

Towards Monolithic 3D Integration: A Design Flow

Panagiotis Chaourani\*, Ana Rusu\*, and Saul Rodriguez\*

\* KTH Royal Institute of Technology, Kista, Sweden

pancha@kth.se

Abstract

Monolithic 3D (M3D) integration technology is a key enabling technology for the implementation of 3D Integrated Circuits (3DICs). 3DICs offer an alternative way for the continuation of Moore’s Law and it comprises of stacking device layers one on top the other. To facilitate the study of M3D circuit topologies a design flow is clearly needed. Towards this, in this work the main potentials and challenges of M3D integration technology are briefly described as well as a design flow is presented for M3D circuits in the form of a Process Design Kit (PDK).

**Keywords:** monolithic (sequential) 3D integration, design flow.

# Introduction and Motivation of Work

The continuous device scaling has reached a dead end as the scaled devices usually fail to meet some critical performance standards like low leakage or high output resistance. To increase the integration density of the future chips, 3DICs where chips expand in three dimensions are proposed. Arguably, the most popular integration technology to process 3DICs is Parallel 3D (P3D) integration which has drown a lot of scientific research recently. In P3D integration 2 wafers can be fabricated separately and then stacked together using Through-Silicon-Vias (TSVs) and micro Bumps. The biggest bottleneck of P3D integration is the large size of TSVs which originates from the poor alignment between stacked wafers. The effects of the large TSVs can become extremely pronounced and deterious as the operating frequency increases. There has been a great effort in literature () to estimate the TSV parasitics and their impact on the performance of a circuit. Novel place and route algorithms have been also proposed for the implementation of P3D chips.

Monolithic 3D integration is an alternative process for the fabrication of 3DICs. In M3D integration transistors can be sequentially processed on top of others. Devices in adjacent layers can be connected through Monolithic Inter-layer Vias (MIVs) that have similar dimensions to the inter-metal vias. Hence, M3D integration offers an unprecedented density of inter-layer connection paths, even at transistor level. One of the biggest impediments of M3D integration is the possible damage of the bottom tier transistors during the processing of the top tier ones. To this end, some low temperature processing techniques for the top tier devices have been proposed. As far as the M3D design techniques are concerned, two main ideas have been proposed () : (1) placing the nmos transistors on top of the pmos ones and (2) stacking digital cells.

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Fig. 1: CDNLive EMEA 2015 Best Paper Awards Ceremony

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# Acknowledgements

Acknowledgements can be placed, if necessary, after conclusions and before the references list.

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