VHDL Design Labs

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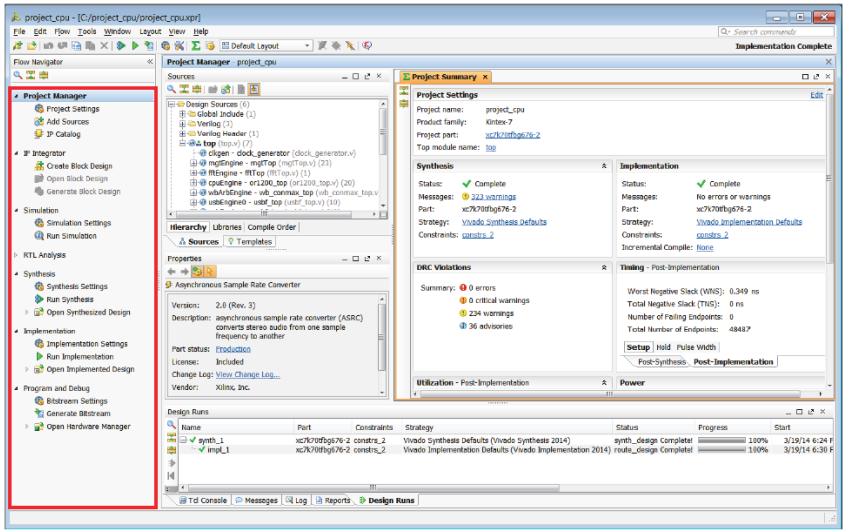
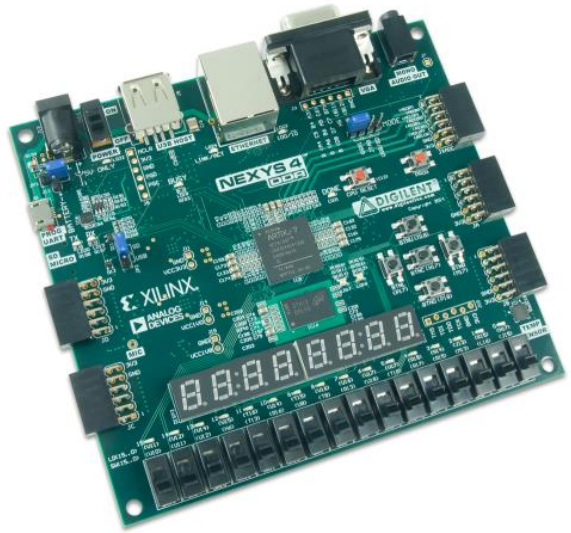
Digital circuit design examples using Xilinx Vivado

Tools



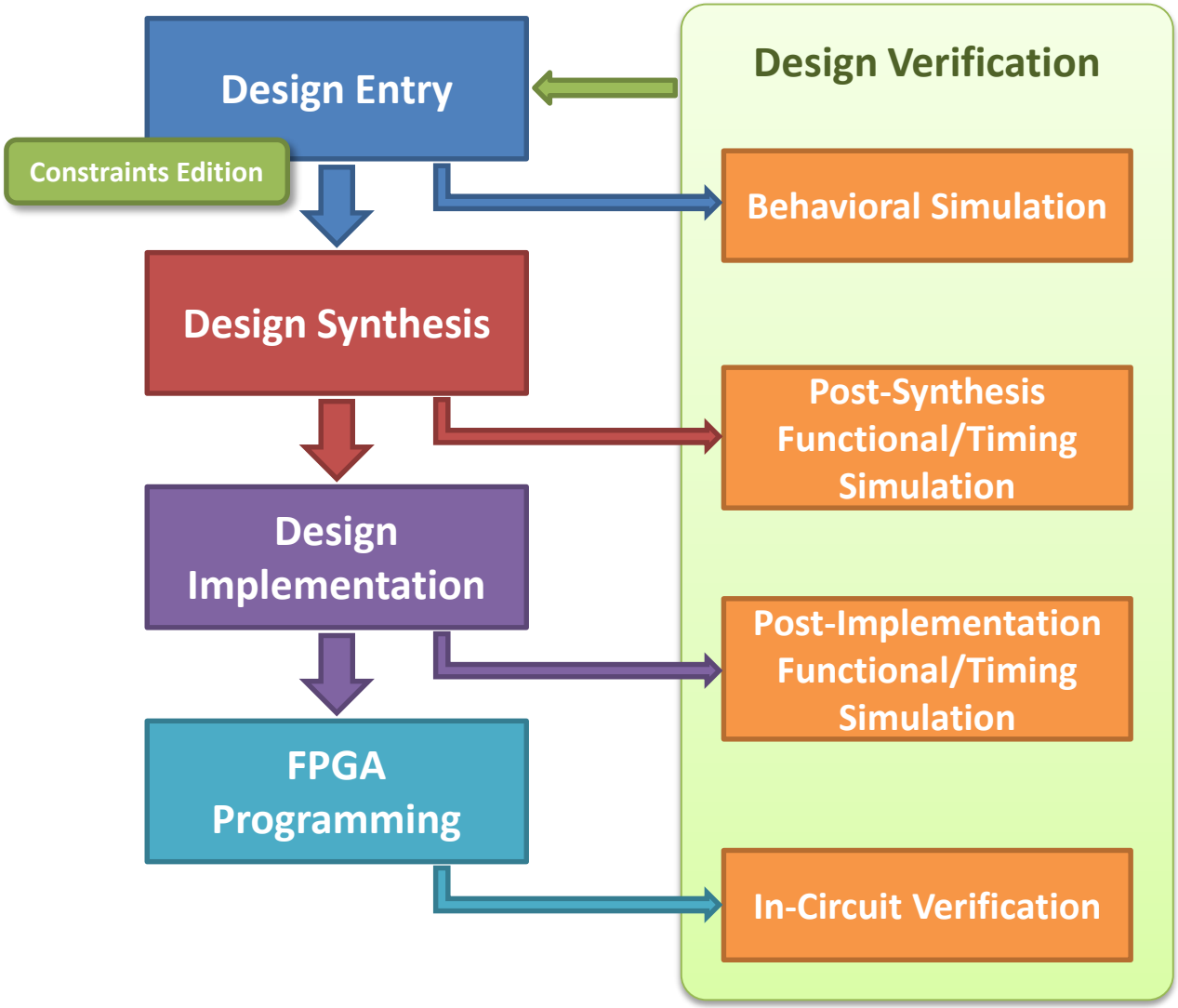
Xilinx Vivado



Nexys 4 DDR Board

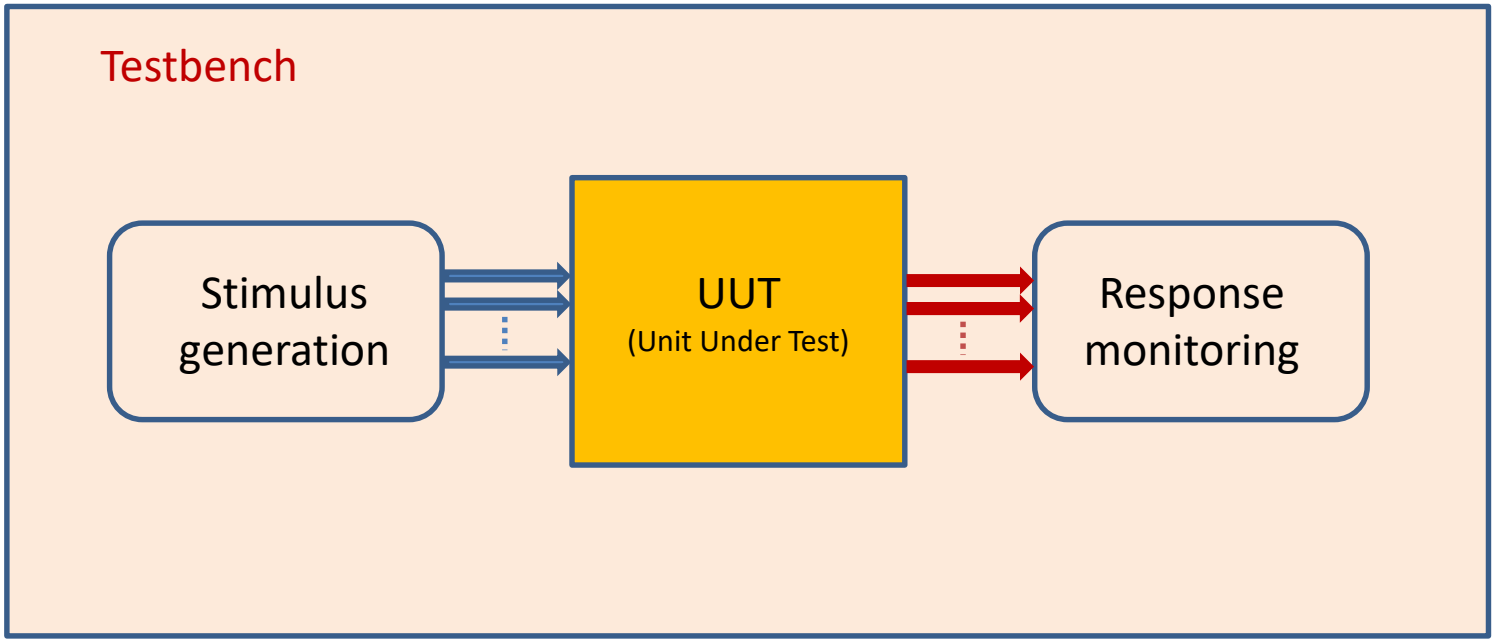
- https://www.amd.com/en/products/software/adaptive-socs-and-fpgas/vivado.html
- https://reference.digilentinc.com/_media/nexys4-ddr:nexys4ddr_rm.pdf

FPGA Based Design Flow



Simulation

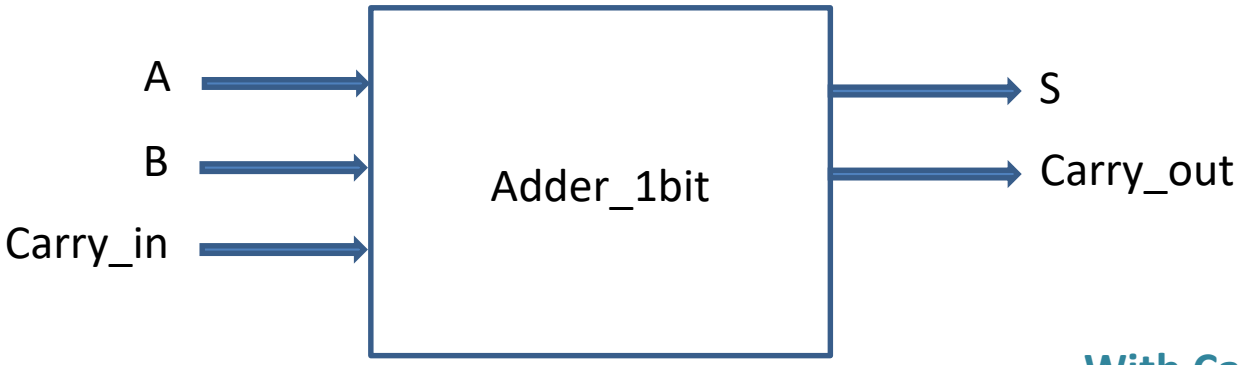
Testbench



Digital circuit design examples using Xilinx Vivado

Design 0

Adder 1 bit



Without Carry_in

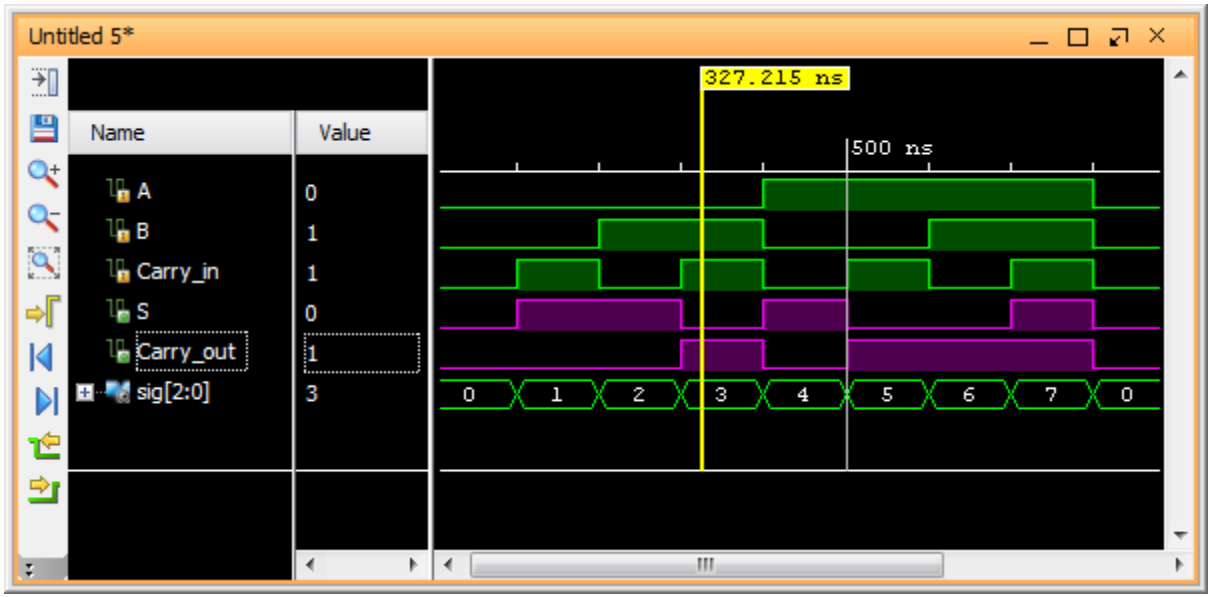
A	B	S	Carry_out
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

With Carry_in

A	B	Carry_in	S	Carry_out
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Design 0

Adder 1 bit

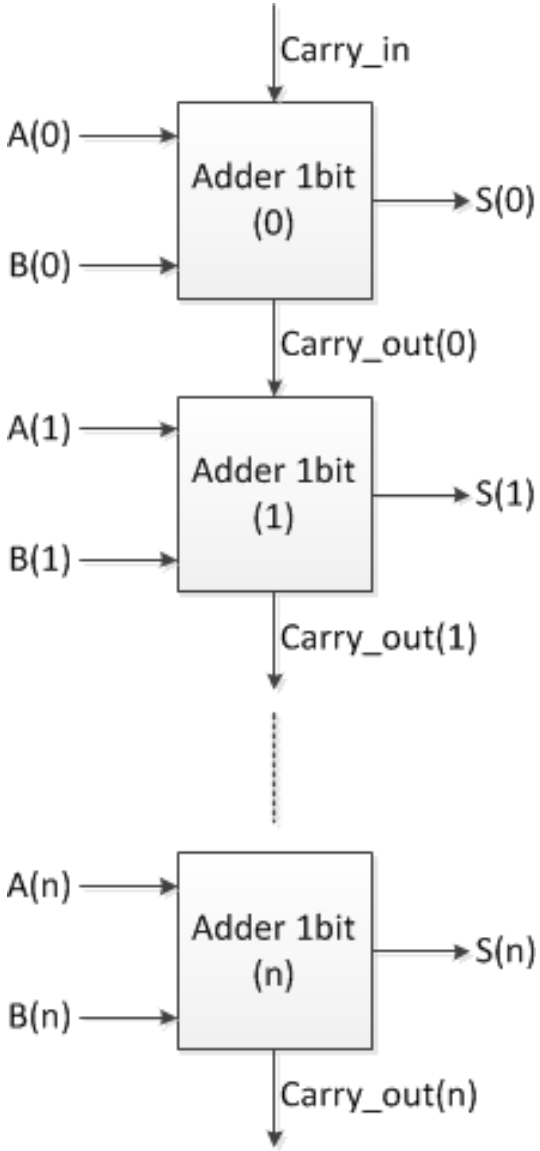


Simulation

Digital circuit design examples using Xilinx Vivado

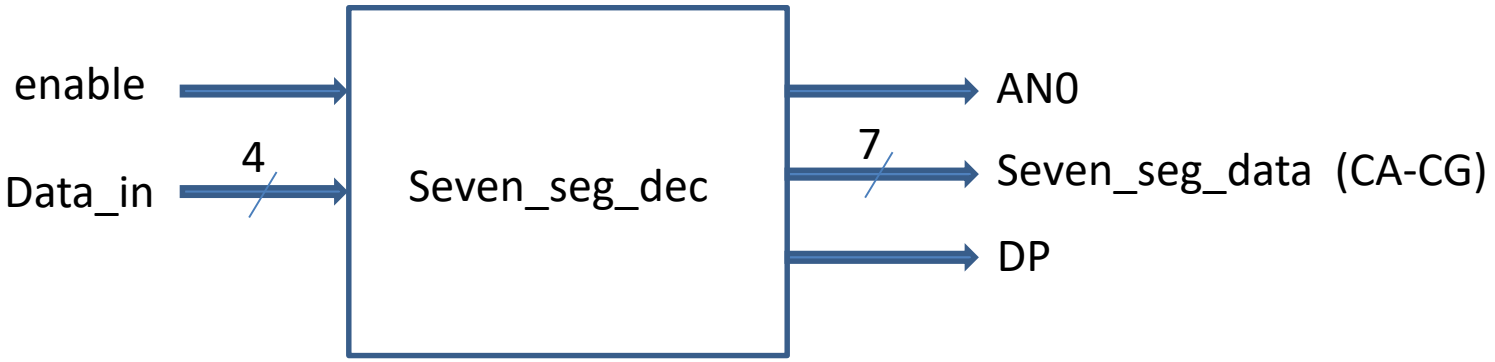
Design 0

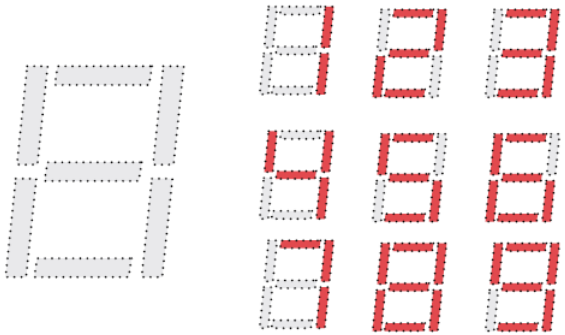
Adder *n* bit

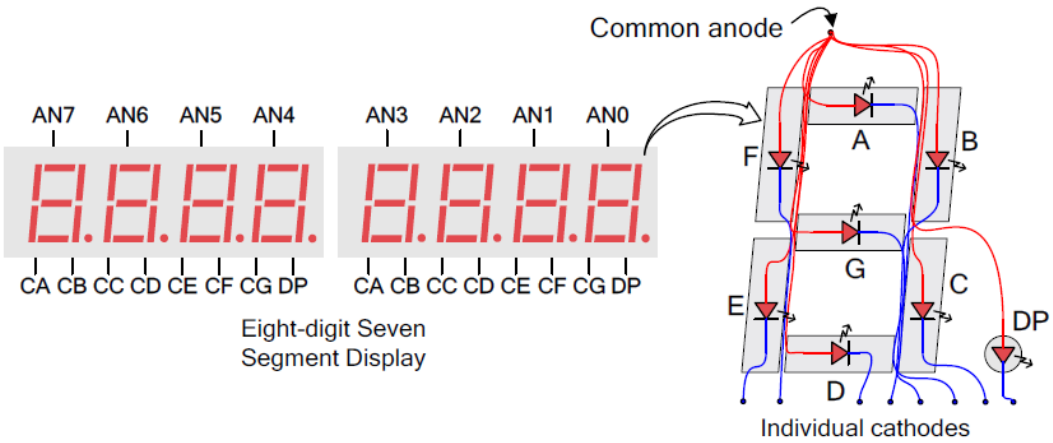


Design 1

Seven Segment Display (One digit)

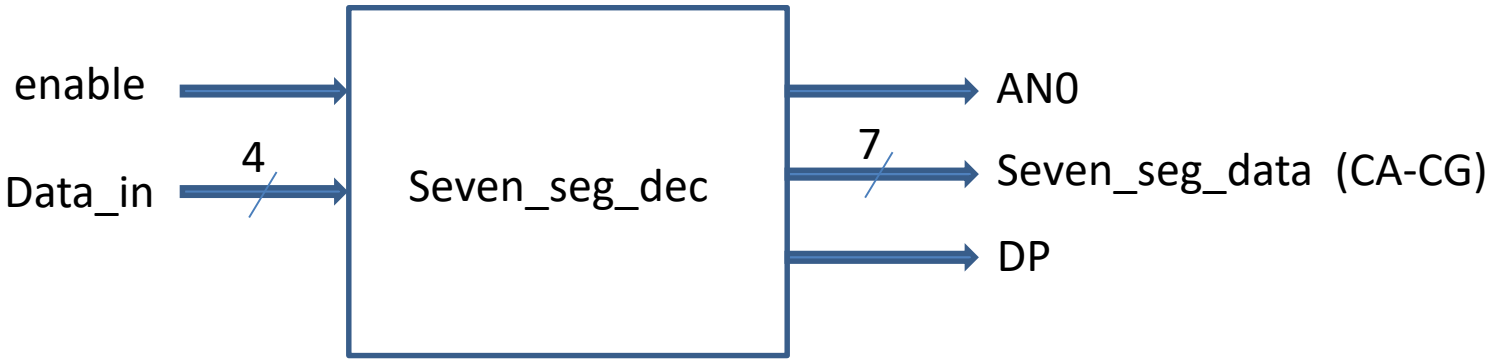






Design 1

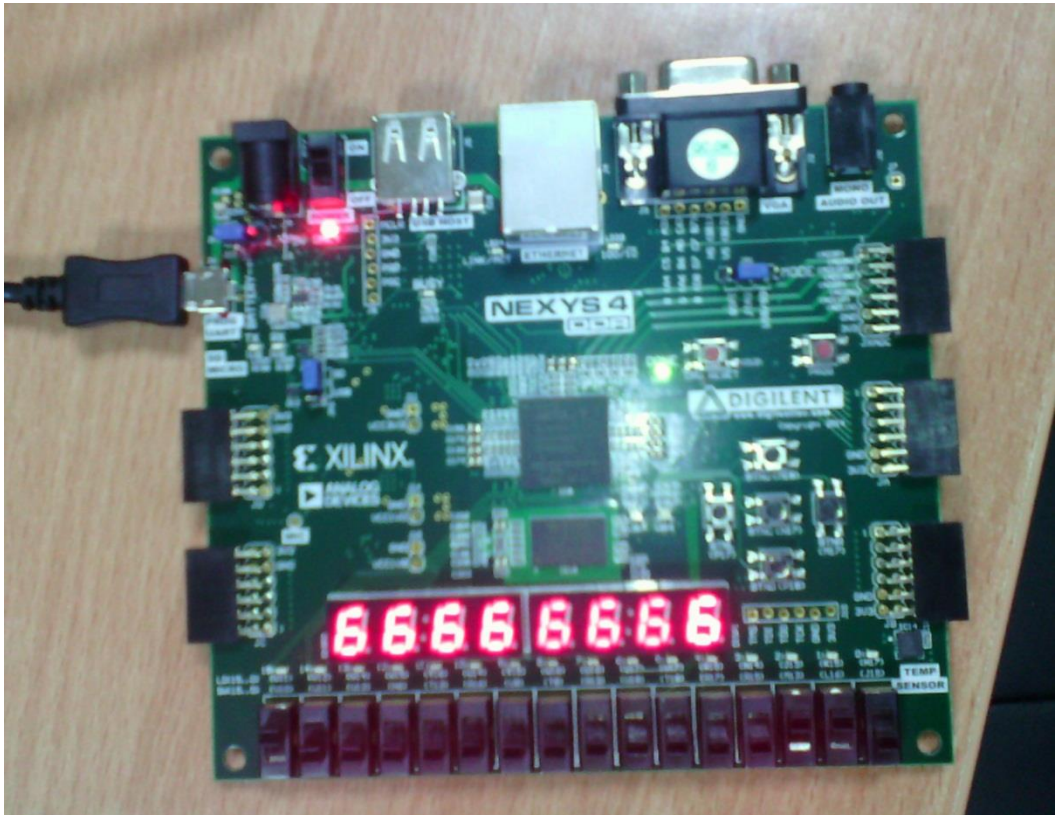
Seven Segment Display (One digit)




```
with BCD_IN select
   SSEG <= "0000001" when "0000",   -- 0
           "1001111" when "0001",   -- 1
           "0010010" when "0010",   -- 2
           "0000110" when "0011",   -- 3
           "1001100" when "0100",   -- 4
           "0100100" when "0101",   -- 5
           "0100000" when "0110",   -- 6
           "0001111" when "0111",   -- 7
           "0000000" when "1000",   -- 8
           "0000100" when "1001",   -- 9
           "0001000" when "1010",   -- A
           "1100000" when "1011",   -- b
           "0110001" when "1100",   -- C
           "1000010" when "1101",   -- d
           "0110000" when "1110",   -- E
           "0111000" when "1111",   -- F
           "1111111" when others;   -- turn off all LEDs
```

Design 1

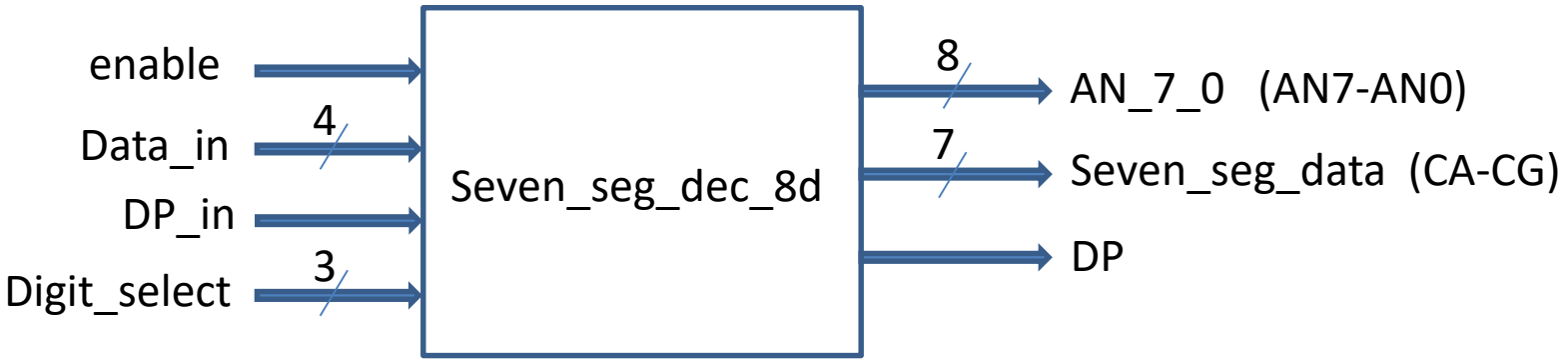
Seven Segment Display (One digit)



Design 1 implementation

Design 2

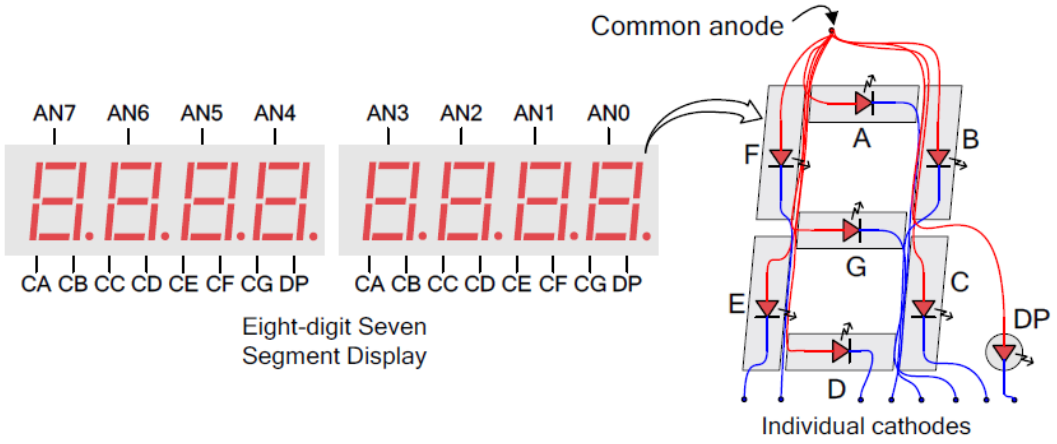
Seven Segment Display (One selected digit)



Digit_select = 0 --> select digit 0
Digit_select = 1 --> select digit 1

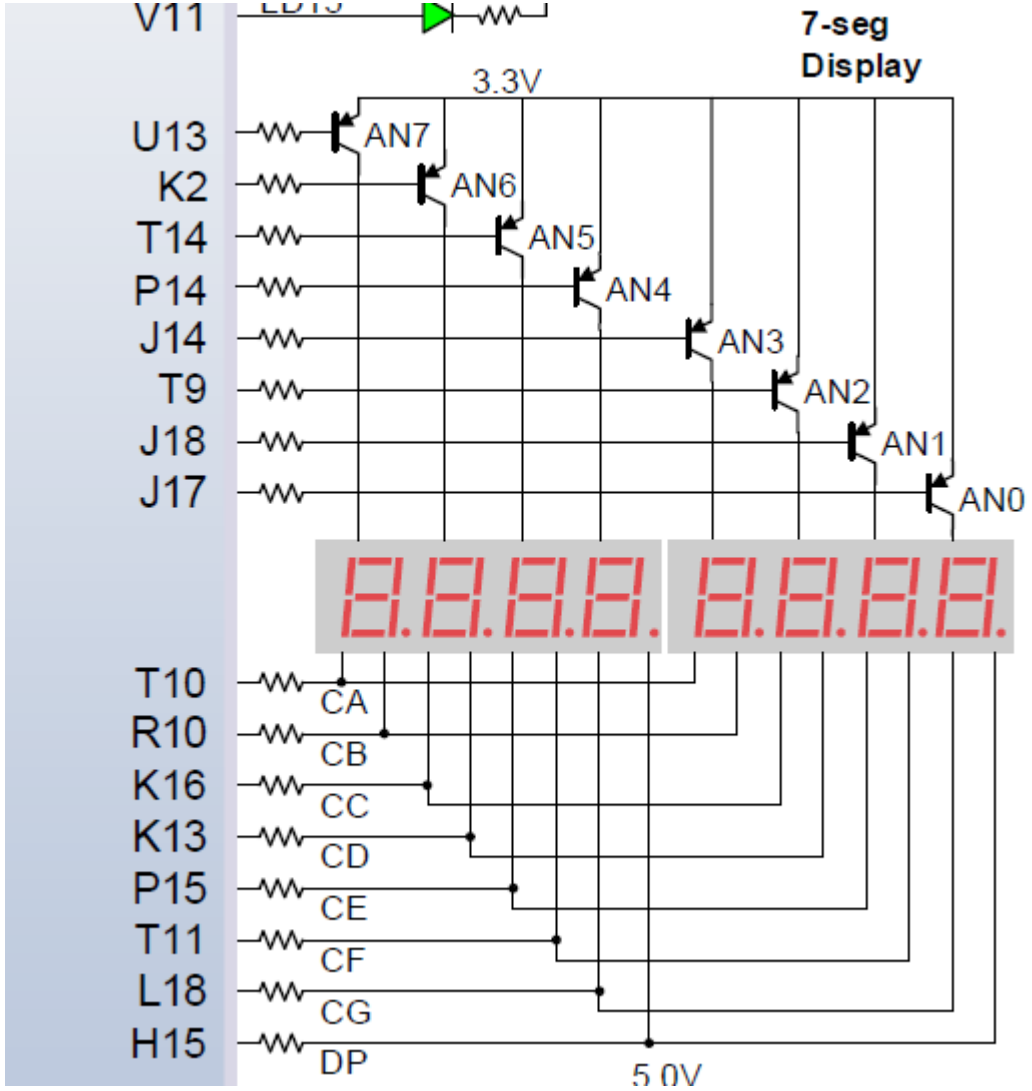
⋮

Digit_select = 7 --> select digit 7



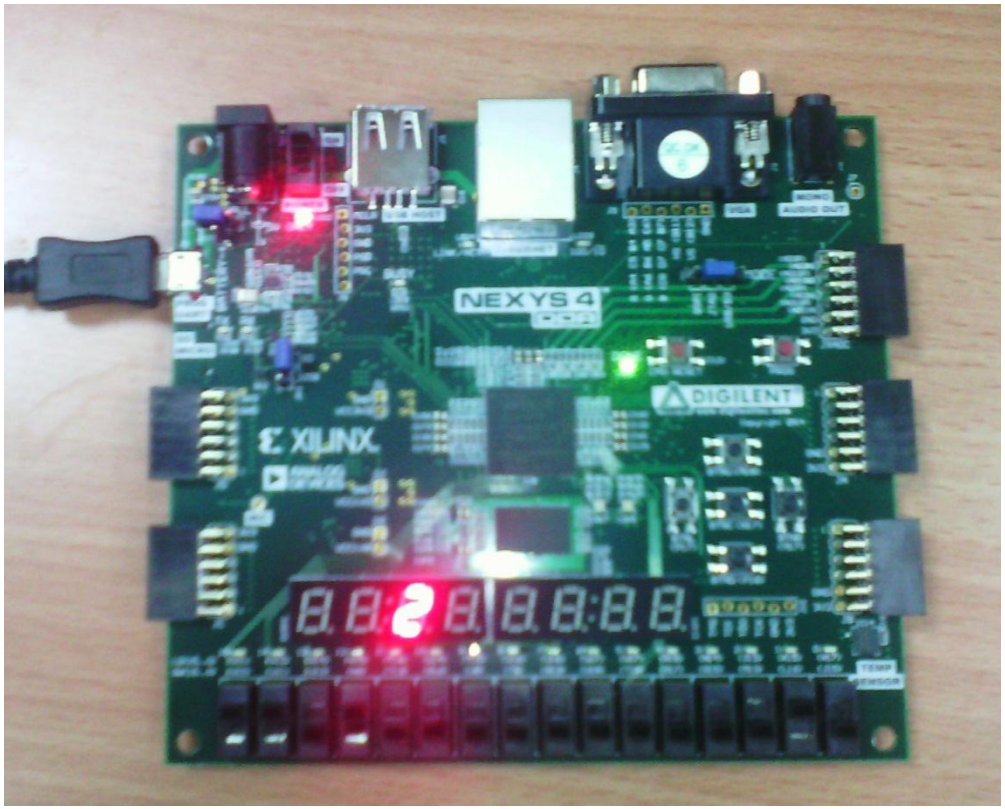
Design 2

Seven Segment Display (One selected digit)



Design 2

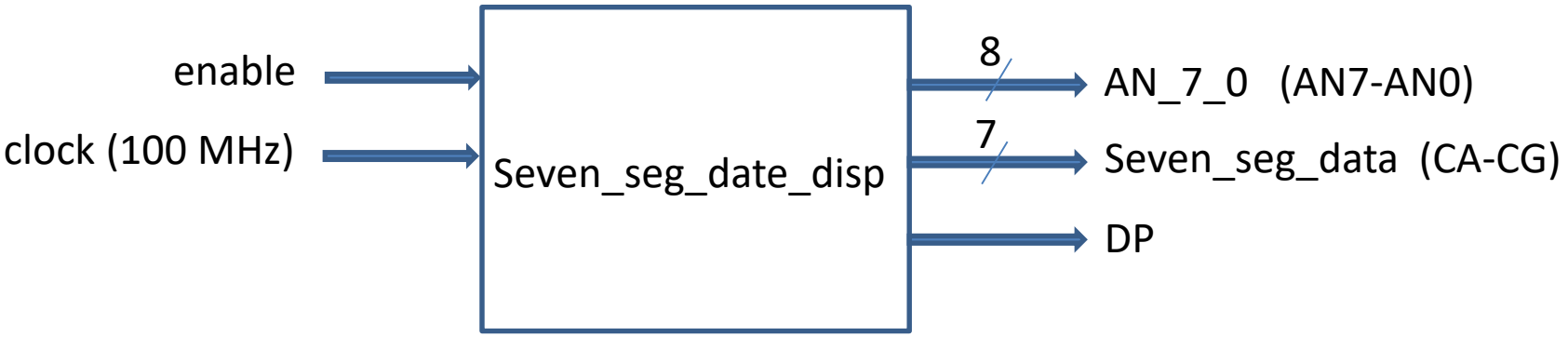
Seven Segment Display (One selected digit)

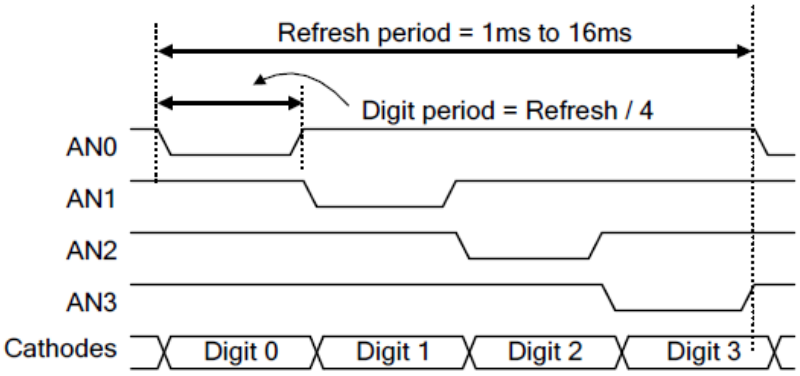


Design 2 implementation

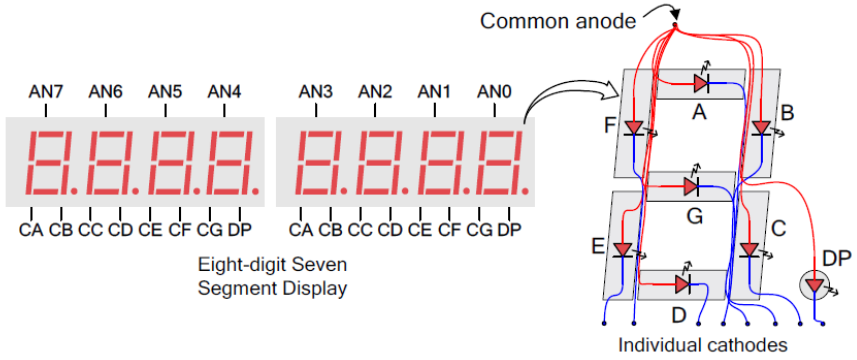
Design 3

Seven Segment Display (Date display)





Four digit scanning display controller timing diagram.

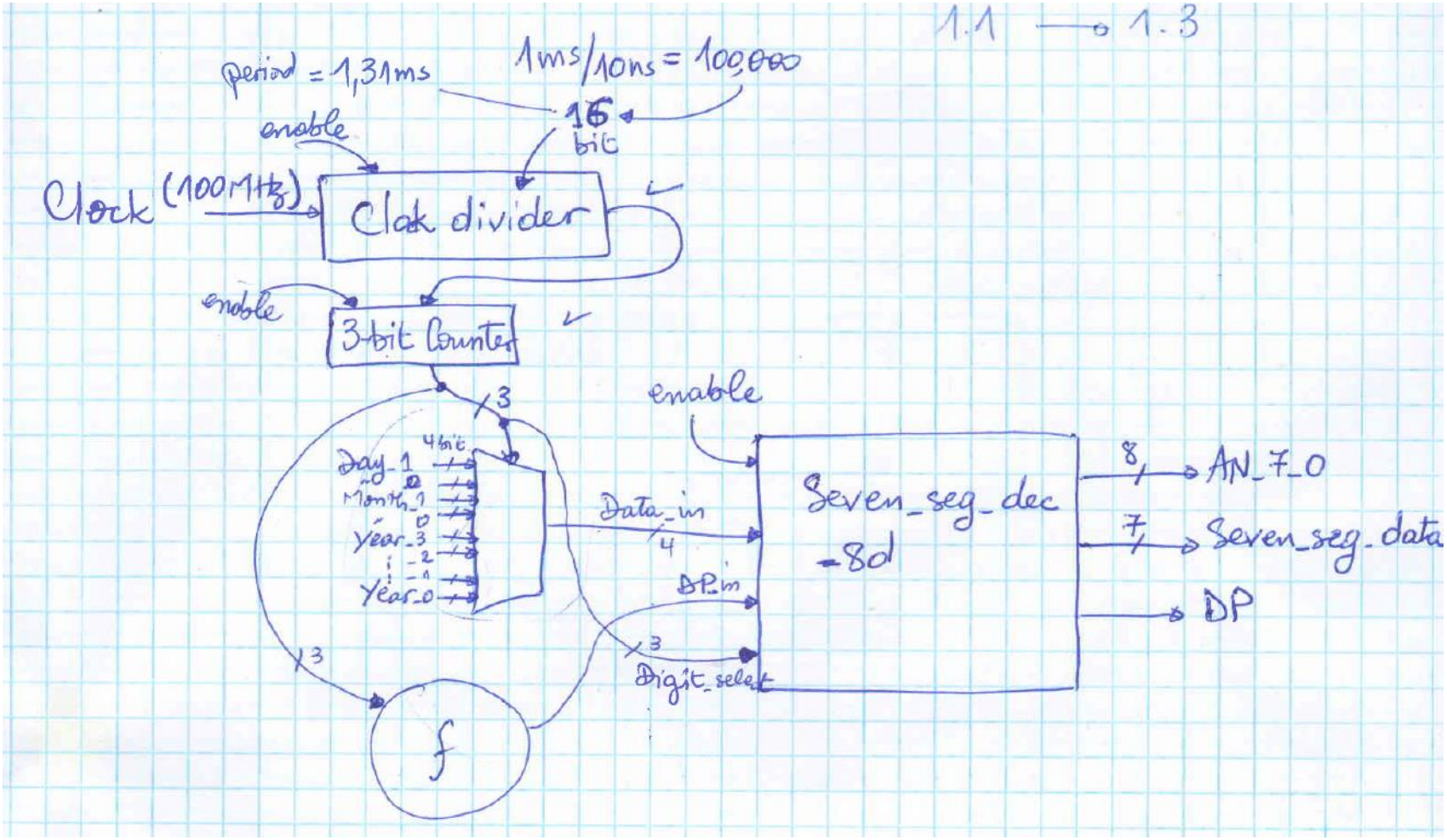


Display example:

16.03.2016

Design 3

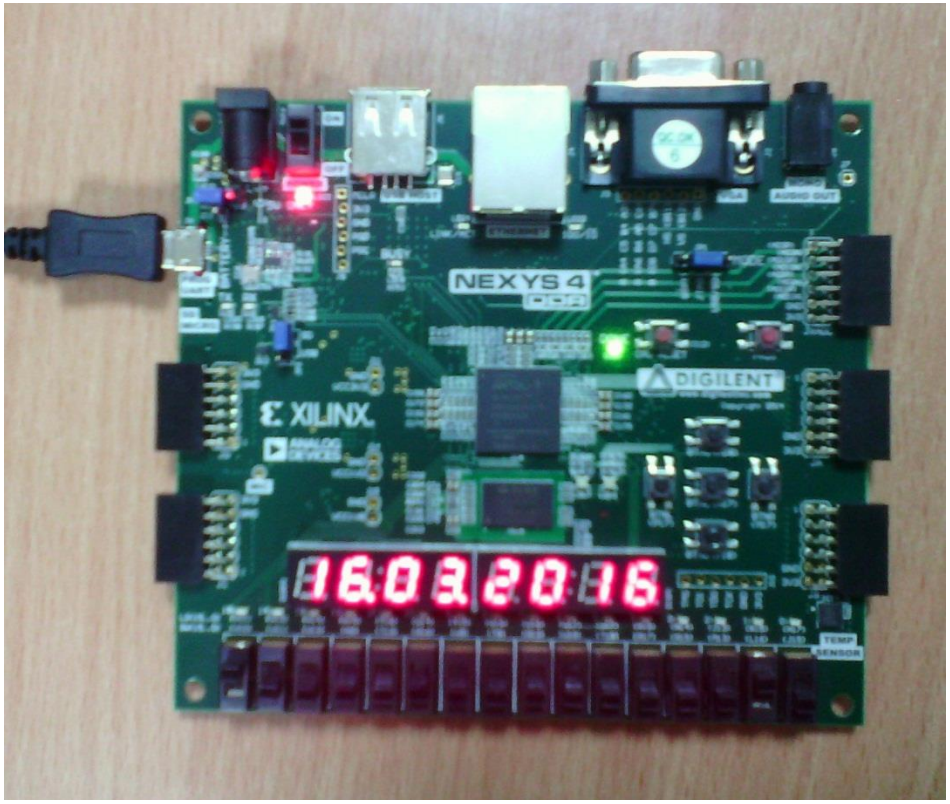
Seven Segment Display (Date display)



Proposed internal architecture

Design 3

Seven Segment Display (Date display)

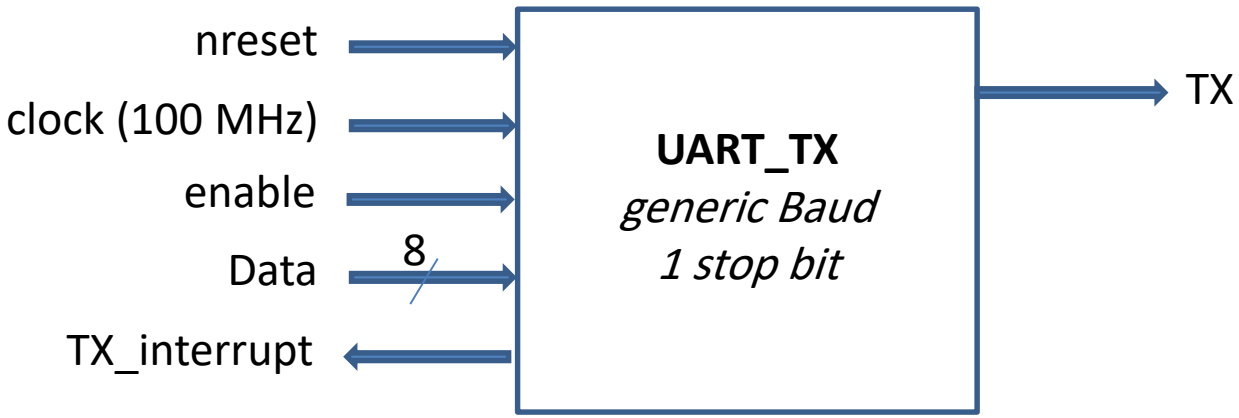


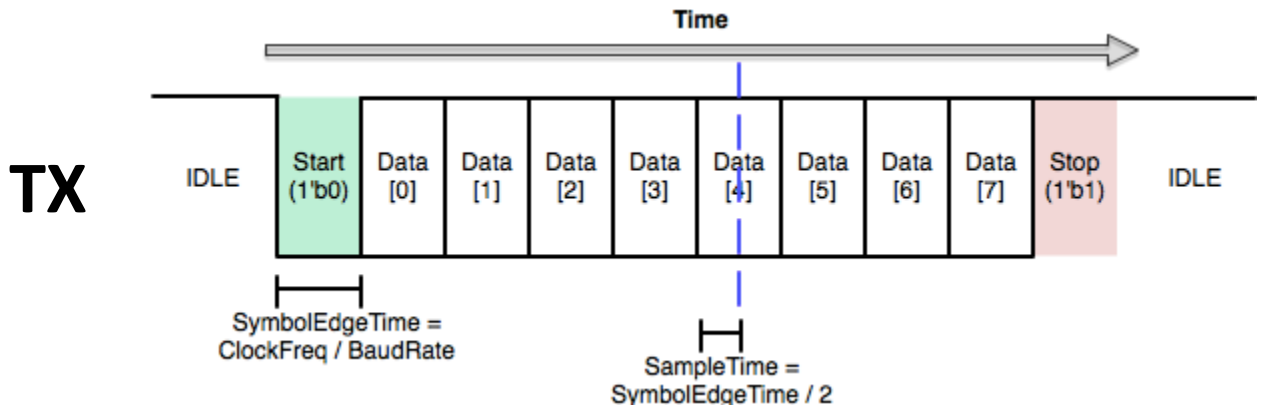
Design 3 implementation

Design 4

Universal Asynchronous Receiver Transmitter (UART)

Transmission part



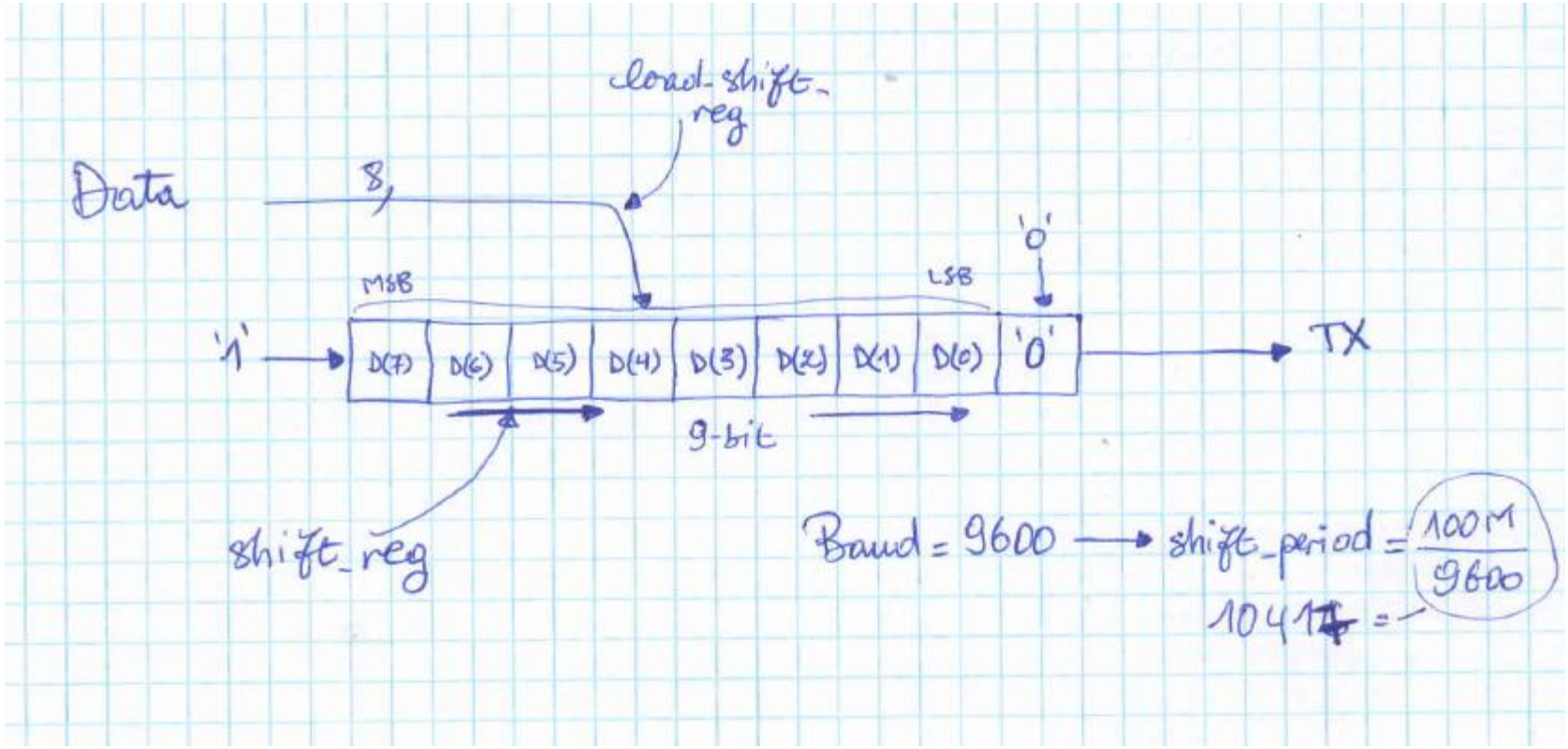


110 baud
300 baud
1 200 baud
2 400 baud
4 800 baud
9 600 baud
19 200 baud
38 400 baud
57 600 baud
115 200 baud
230 400 baud
460 800 baud
921 600 baud
1 843 200 baud
3 686 400 baud
1 baud = 1 bit/s

Design 4

Universal Asynchronous Receiver Transmitter (UART)

Transmission part

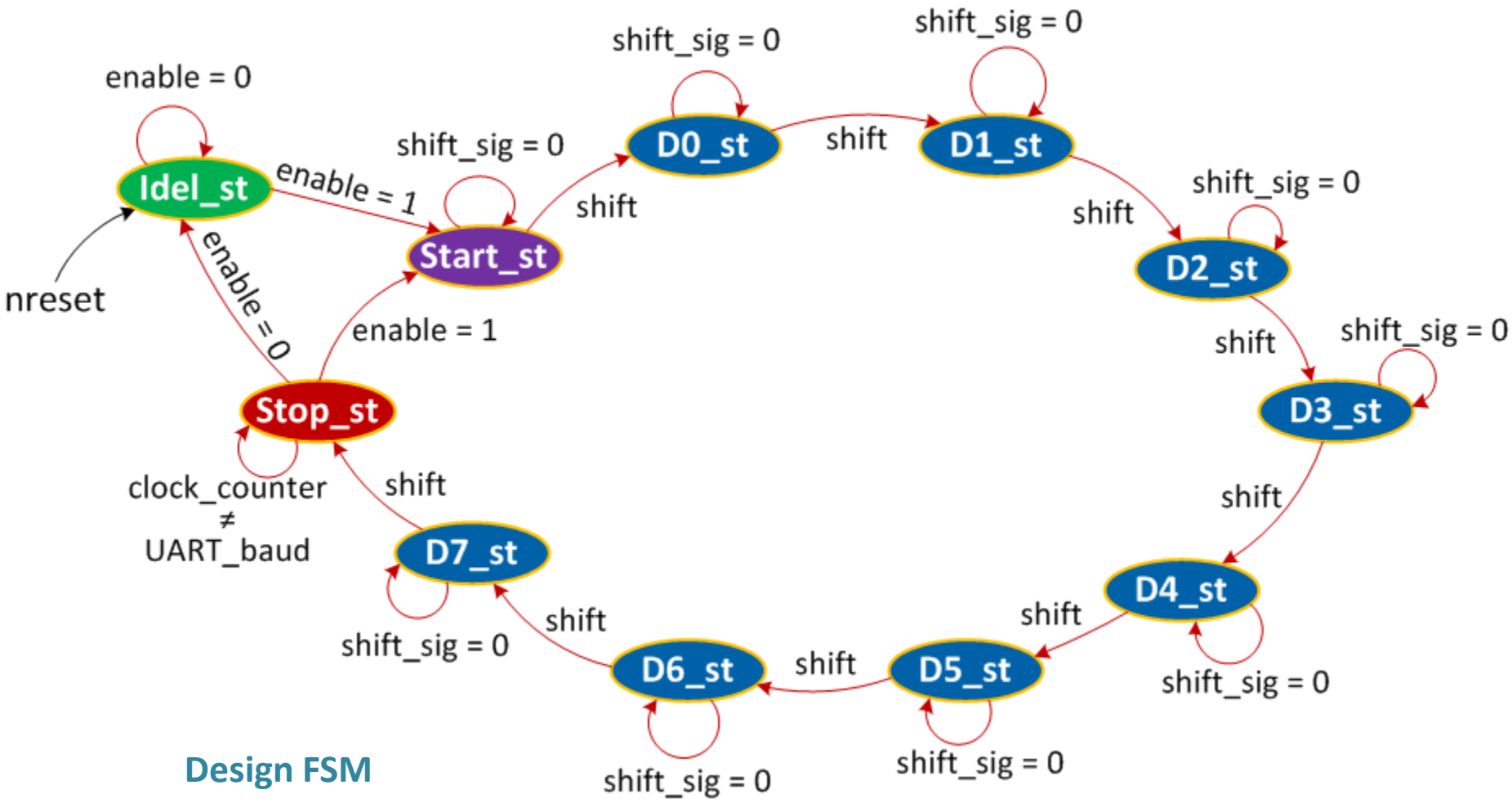


Shift register functioning

Design 4

Universal Asynchronous Receiver Transmitter (UART)

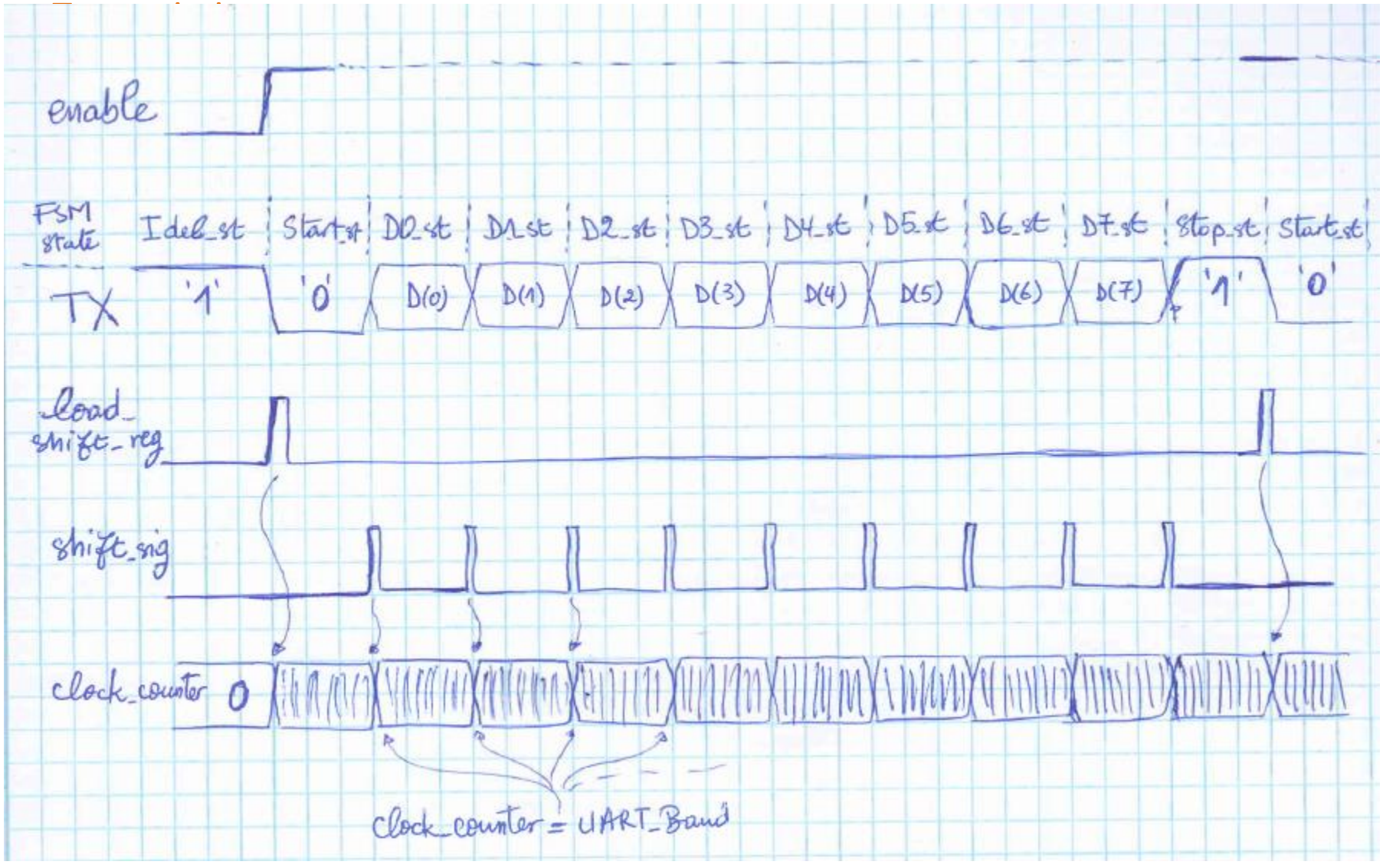
Transmission part



Design FSM

Design 4

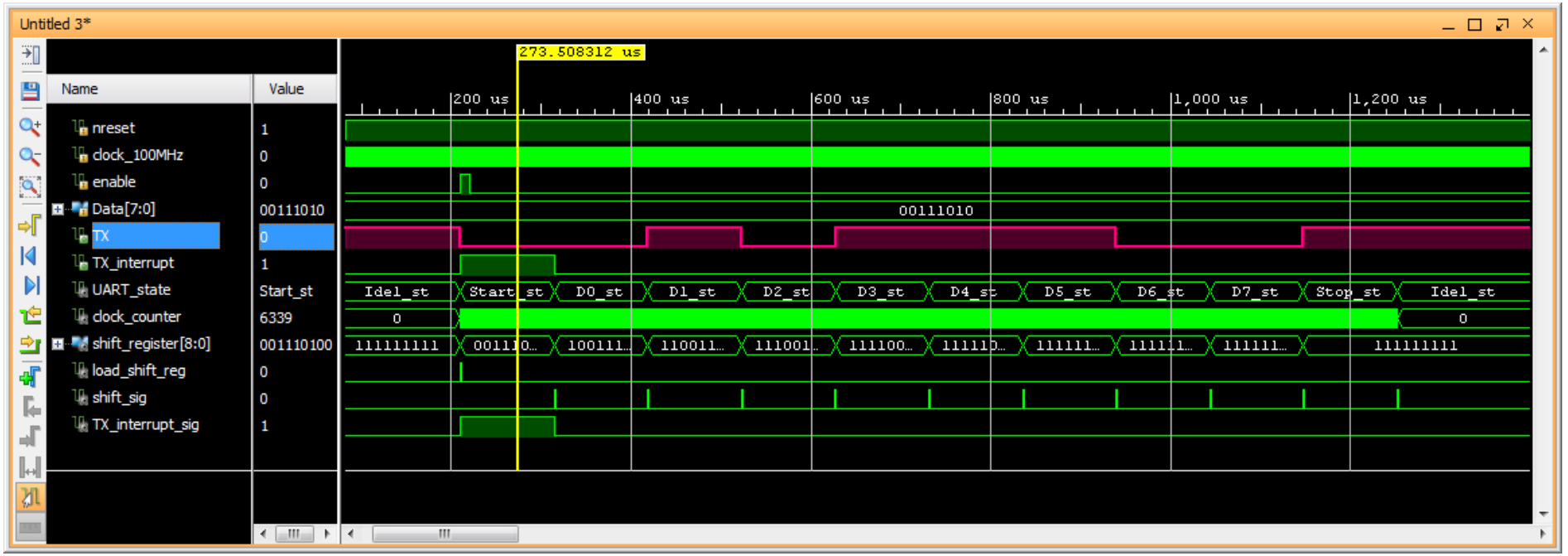
Universal Asynchronous Receiver Transmitter (UART)



Design 4

Universal Asynchronous Receiver Transmitter (UART)

Transmission part

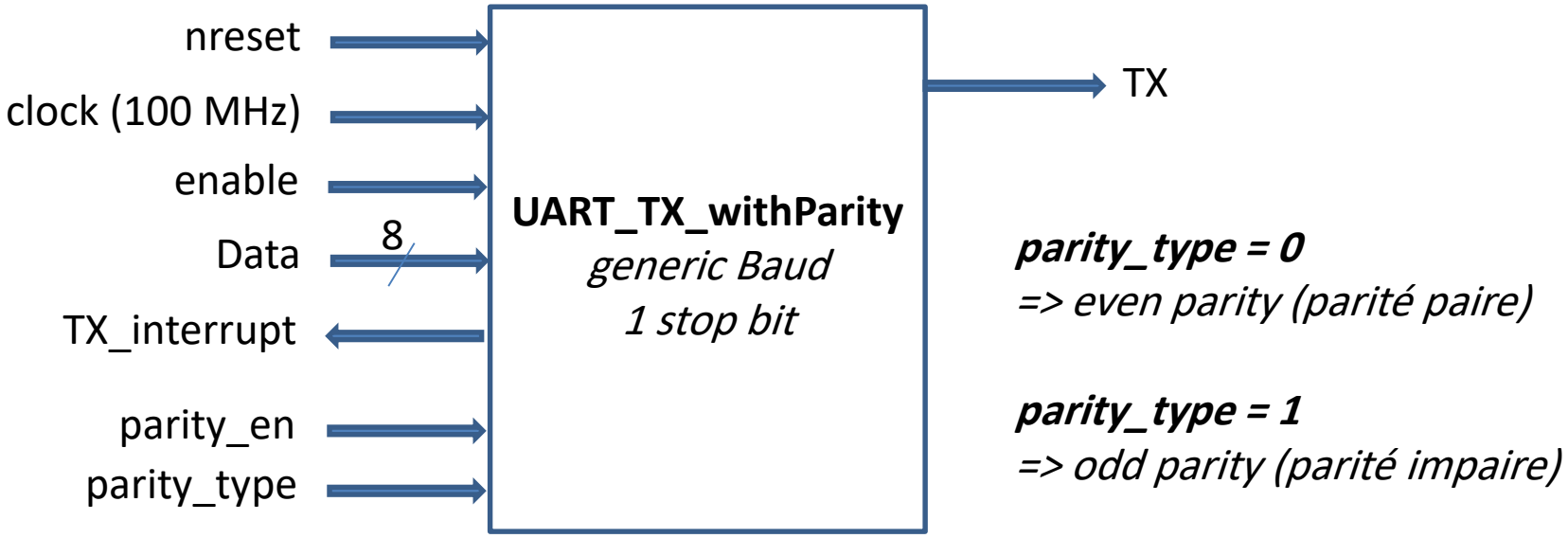


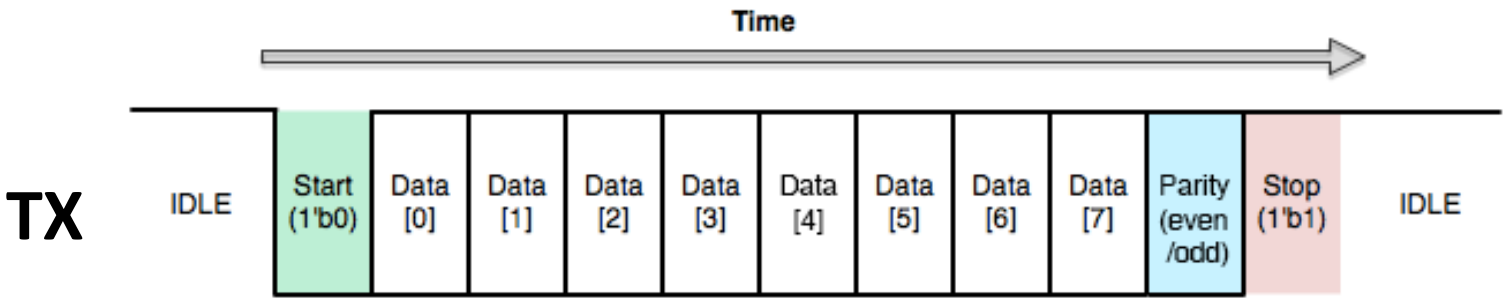
Simulation

Design 5

Universal Asynchronous Receiver Transmitter (UART)

Transmission part (with parity bit)



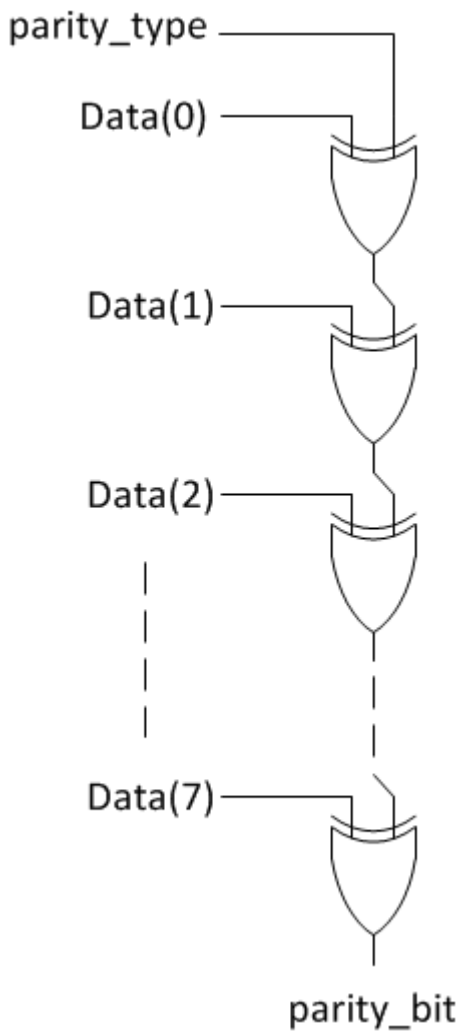


Design 5

Universal Asynchronous Receiver Transmitter (UART)

Transmission part (with parity bit)

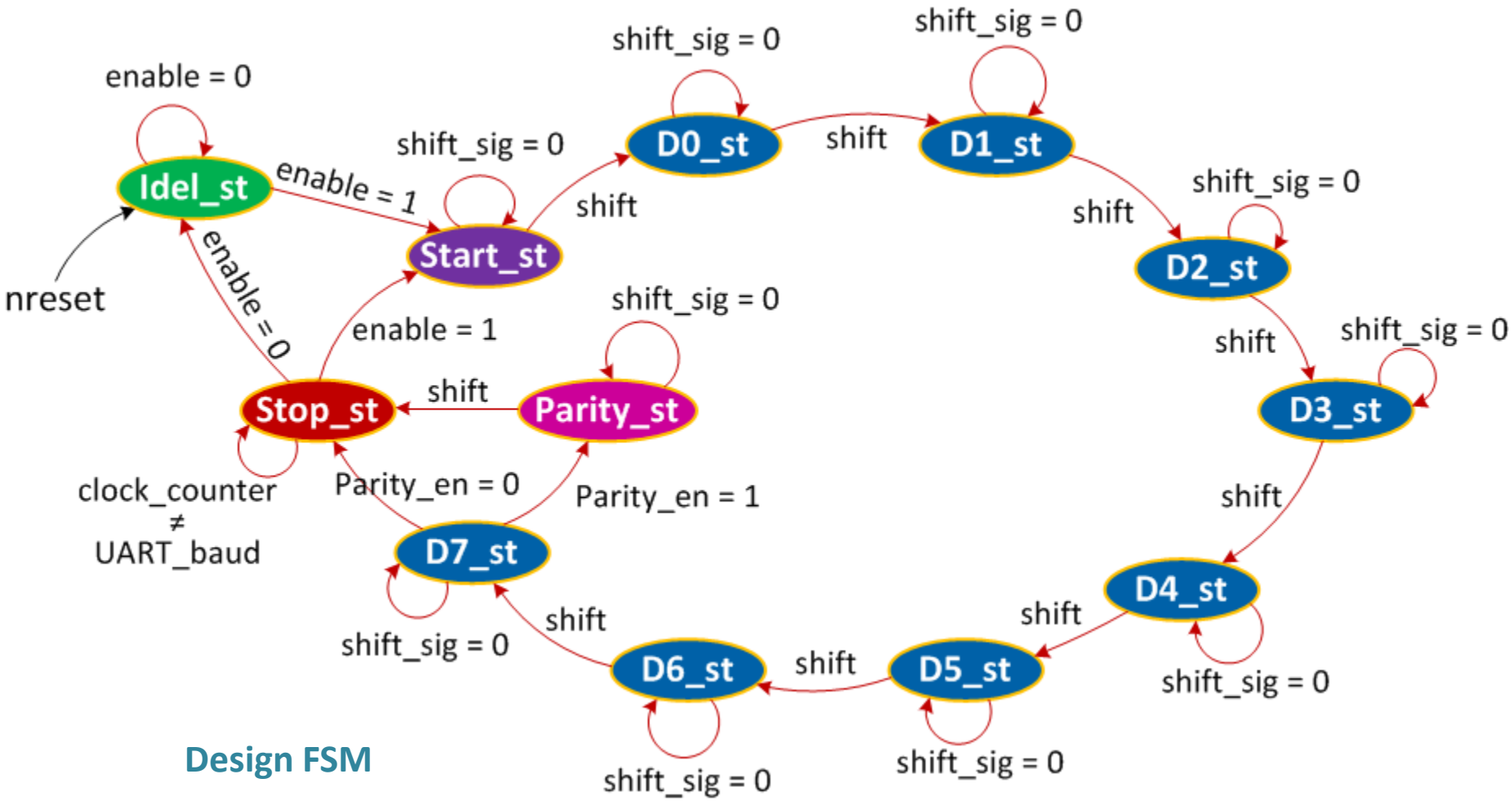
7 bits of data	(count of 1 bits)	8 bits including parity	
		even	odd
0000000	0	00000000	00000001
1010001	3	10100011	10100010
1101001	4	11010010	11010011
1111111	7	11111111	11111110



Design 5

Universal Asynchronous Receiver Transmitter (UART)

Transmission part (with parity bit)

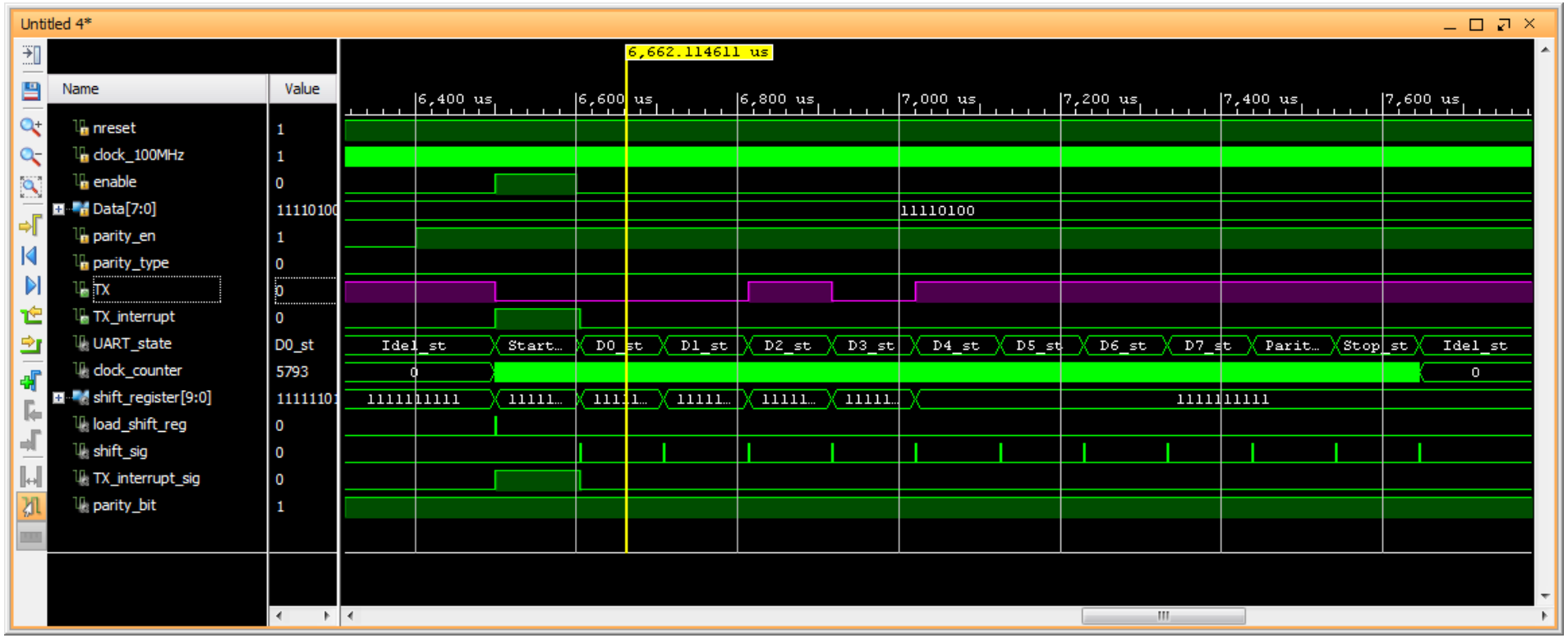


Design FSM

Design 5

Universal Asynchronous Receiver Transmitter (UART)

Transmission part (with parity bit)



Simulation