**Michael T. Fallon**

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**SUMMARY**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Motivated student veteran seeking to leverage internship and military experience by contributing to a dynamic and collaborative team. I aim to demonstrate leadership, teamwork, and a willingness to learn as I prove myself an asset to your organization and explore opportunities to grow as an engineer and a person.

**TECHNICAL SKILLS**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

* RTL development, Static Timing Analysis, verification, CDC, hardware bring-up
* VHDL, Verilog, Vivado, Vitis, Libero, Riviera PRO, Zynq UltraScale+ MPSoC, SmartFusion 2 SoC
* C, MIPS, TCL, MATLAB, Python, O-scopes, Logic analyzers, Spectrum Analyzers

**EDUCATION/PROJECTS**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**San Diego State University (GPA: 3.93 / 4.00) B.S. Electrical Engineering (Exp Grad: May 2023)**

* Created FPGA-based Ethernet MAC with MII interface, compatible with 10/100 Mb/s data rates
  + MDIO driver written in HDL, controlled via AXI-Lite C&S registers to configure PHY from MicroBlaze (C, Verilog)
  + CDC between rx/tx/sys domains using custom async FIFOs, pointers passed using sync pulses (Verilog)
  + Implemented on Artix-7 FPGA dev board and verified with Scapy, Wireshark, and Logic Analyzer (Python)
* Leveraged Time-Multiplexing to implement 16 channel FM synthesizer on Xilinx MiniZed SoC dev board
  + RTL synthesized with Vivado, functional verification achieved using Python based CoCoTB (Verilog, Python)
  + interrupt driven embedded program in Vitis, interfacing with C&S registers in PL fabric via AXI-Lite (C/C++)
  + Mod-Index verified using Bessel Null method with Spec-An, mod amplitude and frequency set dynamically
  + Fixed-point arithmetic DSP, optimal bit-width calculated and verified using MATLAB scripts (Verilog, MATLAB)
* Developed 32-bit pipelined MIPS processor for use on Basys 3 FPGA dev board configured from Quad SPI Flash (Verilog)
* Designed Multi-Layer Neural Network to solve basic non-linearly separable problems (MIPS, C)

**EMPLOYMENT HISTORY**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Innoflight (San Diego, CA) FPGA Engineering Intern (Jan 2022 – Nov 2022)**

* Developed RTL buffer for pipelining data path, with handshaking intact, ensuring design met timing closure (VHDL)
* Spearheaded company-wide adoption of OSVVM, standardizing and improving scope of verification
* Designed SpaceWire Verification Component conforming to ESA standards, enabling system level verification (VHDL)
* Implemented custom RTL to dynamically bias LO driver amplifier using telemetry data feedback loop (VHDL)
* Improved efficiency of FPGA design by writing TCL script to automate simulation environment across projects (TCL)

**San Diego State University (San Diego, CA) Teaching Assistant (Jun 2022 – Present)**

* Created and graded coursework for 50+ students in Microprocessors (CompE 475) and Digital Systems (CompE 470)
* Held office hours covering Verilog, microprocessor architecture, ISA, hazard and exception handling, and memory hierarchy

**Northrop Grumman (Redondo Beach, CA) Electrical Engineering Intern (Jun 2021 – Aug 2021)**

* Assisted with analysis of RF power level control circuit, measuring S-parameters, VSWR, P1dB, and IMD
* Successfully determined passband characteristics of Keysight Digitizer using AWG, O-scope, and Spectrum analyzer

**US Navy (Sasebo, JPN) Electrician’s Mate First Class (Jul 2014 – Jul 2019)**

* Led 12 technicians in maintenance of motors, generators, circuit breakers, and auxiliary electrical equipment
* Supervised operation of electrical generation and transmission equipment onboard USS Bonhomme Richard LHD-6

**CERTIFICATIONS/INVOLVEMENT**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

* Security Clearance – Furnished upon request
* Awarded Navy and Marine Corp Achievement Medal – x2
* Tau Beta Pi Member – California Xi Chapter