Typically, the Zynq will be the master and will send control signals and data to its various slaves. It does this using Control registers via the AXI lite interface. When the Zynq requires an update regarding the current conditions of the PL fabric, it will read from Status registers, which are written to from the FPGA. This is an important distinction, the Zynq CANNOT write to the Status registers, but can only read from them. The combination of these two sets of registers make up the most common use case for an AXI slave interface; the Control and Status Register File (C&S Registers).

For this assignment, review the AXI documentation and describe a register file with an AXI slave interface. Your register file should be 8 registers deep and should contain 4 read/write registers and 4 read only registers. This will be a simple C&S register file where the 4 RW registers are your Control registers and the RO registers are the Status registers. Use the following configuration for your design.



The Data Width of your design should be 32 bits. You will need to write an embedded c program to write to the first four registers from Vitis, and you should be able to read their inverted value from the next four registers.