Instruction	Opcode	Opcode Hex	Reg_Dst	Write_Enb	ALU_OP0	ALU_OP1	ALU_OP2	ALU_Src	Store_Enb	Load_Enb	RAM_to_Reg	BEQ_Control	JU
ADD	"000"	0	0	1	1	0	0	0	0	0	0	0	
SUB	"001"	1	0	1	1	0	1	0	0	0	0	0	
MULi	"010"	2	1	1	1	1	0	1	0	0	0	0	
DIVi	"011"	3	1	1	1	1	1	1	0	0	0	0	
	"100"	4	1	1	1	0	0	1	0	1	1	0	
SW	"101"	5	1	0	1	0	0	1	1	0	0	0	
BEQ	"110"	6	0	0	1	0	1	0	0	0	0	1	
	"111"	7	0	0	0	0	0	0	0	0	0	0	