Department of

Electrical & Electronics Engineering

Abdullah Gul University

Electronics 1

Uneven Seven-Sided Dice Roller Project

Task 2

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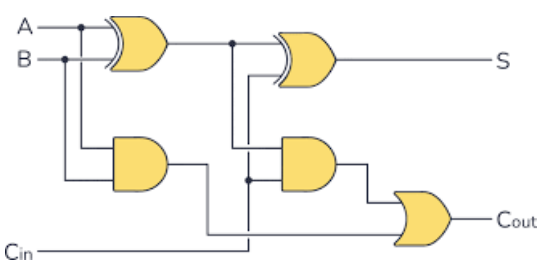
Full Adder



Full adders play an important role in the uneven seven-sided dice roller system by facilitating binary additional operations. They are responsible for the addition of two double steps with a carry input (CIN). This addition process is the basis for creating the result by contributing to the randomness of the system.

(Figure 1.1 | General Full Adder)

In this step, Cin is asked to always be set to '1'. When Cin is set to '1', the circuit and the truth table is summarized because the possibilities that can happen when Cin is 0 are eliminated. Therefore the operations are made with boolean expressions by taking Cin as '1' and then the sum and carry boolean expressions are found. By looking at these expressions, the circuit is reduced if necessary.

When A and B pass through XOR gate then the ouput of the first XOR gate and Cin go through the second XOR gate, the sum is gotten:

$$the\ output\ of\ the\ first\ XOR\ gate = A'.B + B'.A \qquad (1.1)$$

$$the\ output\ of\ the\ second\ XOR\ gate = (A \oplus B)'.Cin + (A \oplus B).Cin' \qquad (1.2)$$

Note: Cin is set to '1'. Therefore some simplifications are made in further operations based on the information.

$$the\ simplified\ version = A.B + A'.B' \qquad (1.3)$$

The simplified version, 1.3, shows that it is sufficient to use XNOR in this diagram to be able to get sum when Cin is set to '1'. Thus the circuit diagram with logic gates for the sum is know anymore.

When A and B pass through the first AND gate and the output of the first XOR gate and Cin pass through the second AND gate. Then the ouput of the first AND gate and the output of the second AND gate go through the OR gate, the carry is gotten:

$$the\ output\ of\ the\ first\ AND\ gate = \mathrm{A.B} \qquad (2.1)$$

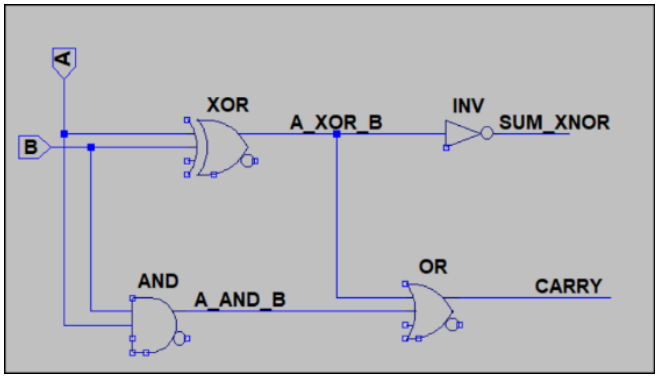
$$the\ output\ of\ the\ second\ AND\ gate = (A \oplus B).Cin \qquad (2.2)$$

$$the\ output\ of\ the\ OR\ gate = AB + (A \oplus B).Cin \qquad (2.3)$$

Note: Cin is set to '1'. Therefore some simplifications are made in further operations based on the information.

$$the\ simplified\ version = A'.B + A.B' + A.B \qquad (2.4)$$

Based on this boolean expression, 2.4, it is seen that using one AND gate and one OR gate is enough to be able to get the carry.



(Figure 1.2 |Simplfied Full Adder)

According to these expressions the simplfied version of the full adder is as in Figure 1.2.

The specific full adder circuit with a fixed carry input (C0) with two double inputs (A and B) and produces two outputs: Sum (s) and one carry output (cout). The circuit uses the CMOS configuration to process the dual addition efficiently while maintaining the constant carry input. It works according to the principle of combining binary numbers and carry input to create the sum and spread a carry output if necessary.

A	B	Cin	Sum (S)	Cout
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

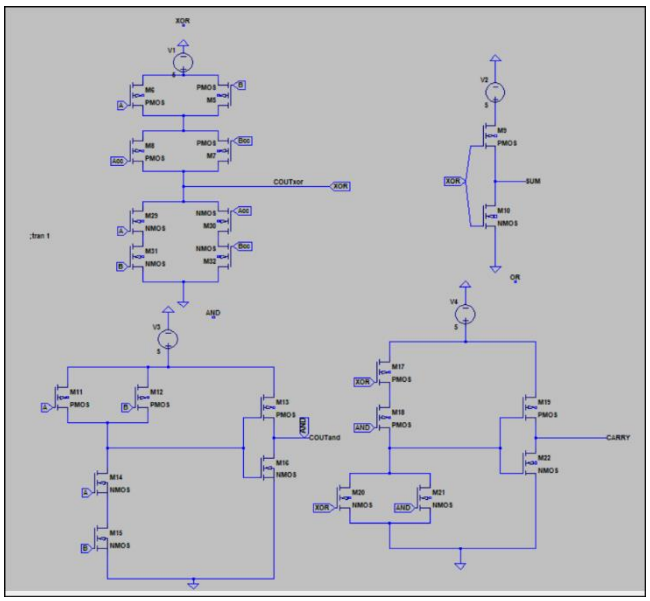
(Figure 1.3 | Truth Table of The Selected Full Adder)

The selected full adder circuit is fixed, especially at CIN 1, due to the suitability of the dual addition within the restrictions of the system. It provides efficient work while contributing to the general functionality of the uneven seven-sided dice roller system.

When CIN (C0) is '1', the theoretical truth for the full adder can be summarized as in Figure 1.3.

This truth table outlines the expected outputs of the full adder circuit when provided with different combinations of inputs, with Cin fixed at '1'.

A. Circuit Diagram

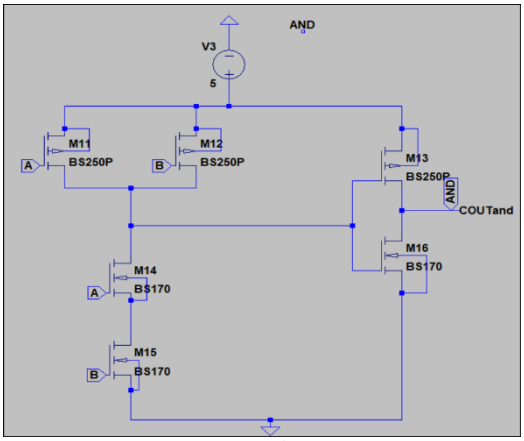


(Figure 2.1 | Circuit Diagram of The Selected Full Adder)

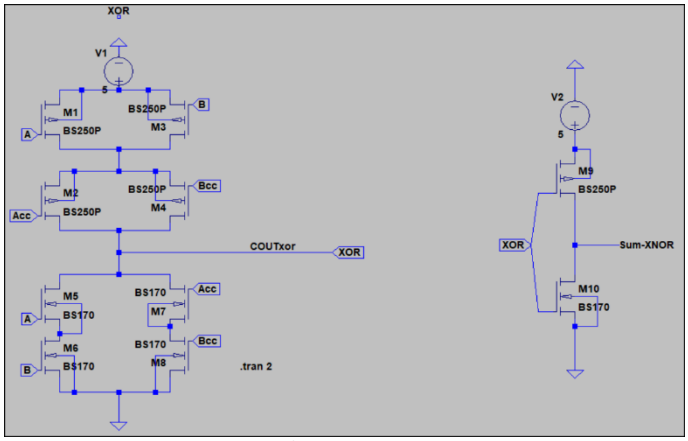
The CMOS full adder circuit was purposefully designed to execute binary addition tasks efficiently within the uneven seven-sided dice roller system. Its integration of PMOS and NMOS transistors in a CMOS configuration ensures robust performance while maintaining low power consumption.

The circuit includes XNOR gate, AND gate and OR gate and they are designed and built in CMOS configuration. The sum is output of cmos XOR gate circuit while the carry is output of CMOS OR gate circuit.

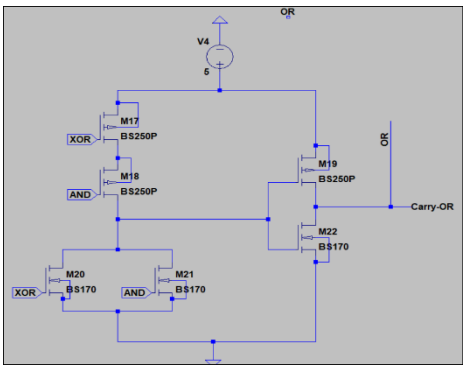
As know Cin is set to ‘1’. A and B are inputs for the full adder İN Figure 2.1. The complements of A and B are also used in this configuration.



(Figure 2.2 | Circuit Diagram of CMOS AND Gate Circuit)



(Figure 2.3 | Circuit Diagram of CMOS XOR Gate and SUM-XNOR Circuit)



(Figure 2.4 | Circuit Diagram of CMOS OR Gate Circuit)

Labels are used to connect the circuits to each other as seen in Figure 2.1 – 2.2 – 2.3 – 2.4.

For the sum part, A and B pass through XOR gate and then the ouput is inverted. At the end of this proccess, the sum is gotten.

For the carry, A and B pass through AND gate and then the output go through OR gate. At the end of this proccess, the carryout is gotten.

Mosfet's parameters can be easily adjusted.. BS170, NMOS, and BS250P, PMOS, mosfet models are used to design and build this circuit. Mosfet's VTO and KP values:

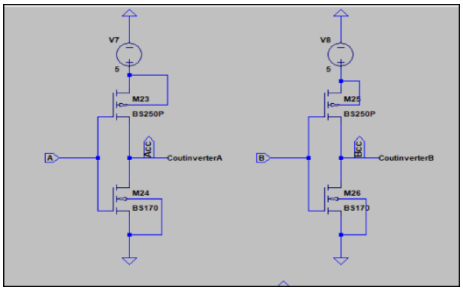
```
.MODEL BS250P PMOS Rg=160 VTO=-3.193 RS=2.041 RD=0.697 IS=2E-13 KP=0.277  PB=1n RB=0.309 Rds=1.2E8

.model BS170 NMOS VTO=1.824 RG=270 RS=1.572 RD=1.436 RB=.768 KP=.1233 Rds=1.2E8 IS=5p Tt=161.6n
```

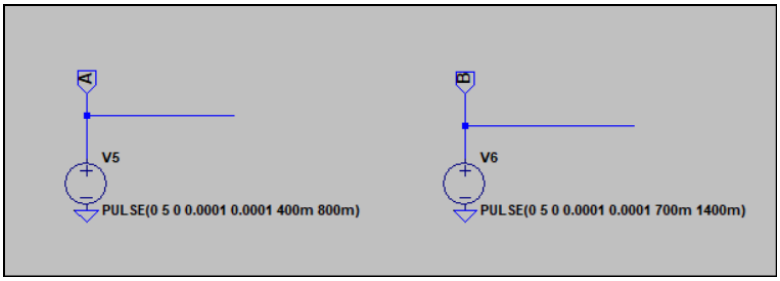
(Figure 2.5 | model mosfet's, BS170 and BS250P, parameteres)

As shown in Figure 2.5:

VTO= -3. 193 and KP=0.277 for BS250P, VTO= 1.824 and KP=.1233 for BS170



(Figure 2.6 | Inverters for A and B Pulses)



(Figure 2.7 | A and B Pulses)

As seen in Figure 2.7:

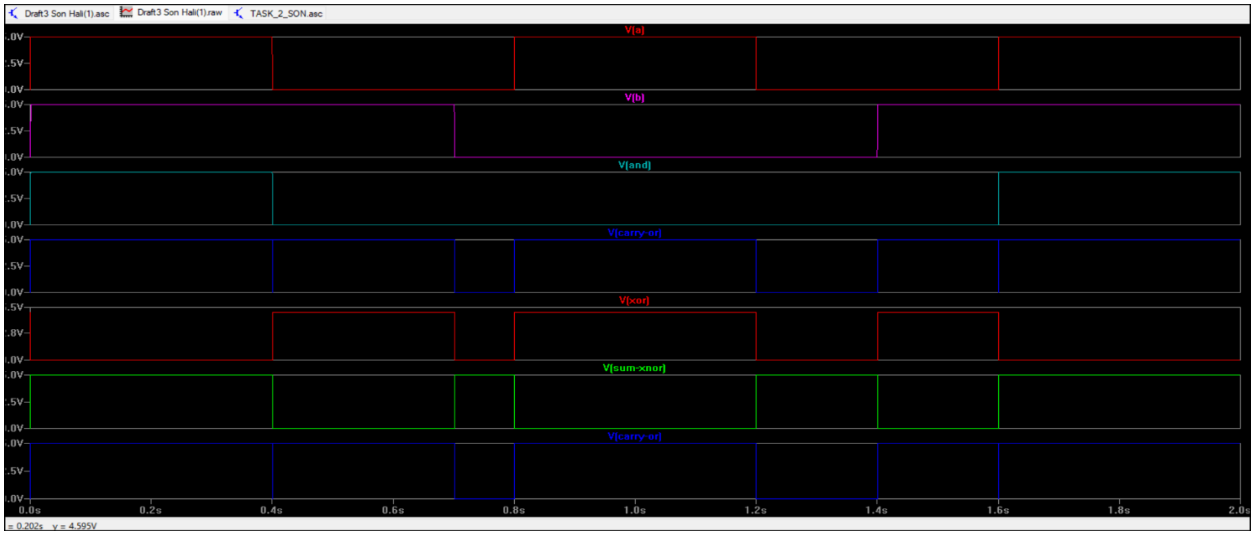
A pulse parameters: Von= 5V, Delay=0s, Trise=0.0001s, Tfall= 0.0001s, Ton= 400ms, Tperiod= 800ms

B pulse parameters: Von= 5V, Delay=0s, Trise=0.0001s, Tfall= 0.0001s, Ton= 700ms, Tperiod= 1400ms

B. Simulation Results

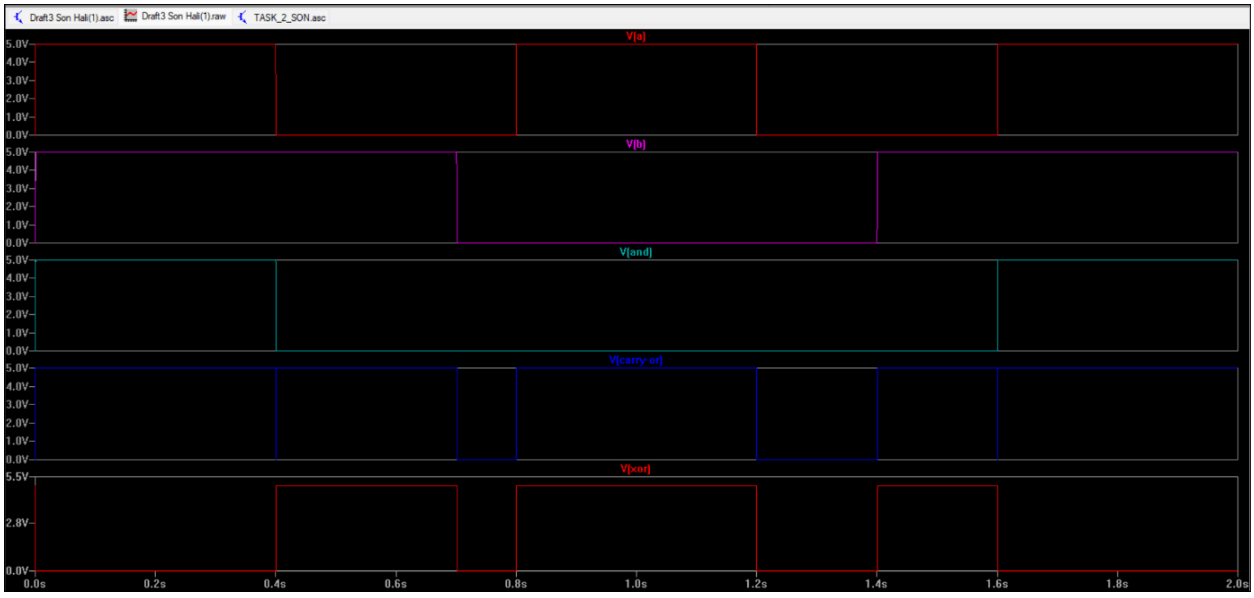
Representation are as below:

A: A Pulse, **B:** B Pulse, **AND**: AND gate output, **Carry-OR**: Both OR gate and Carry output, **XOR:** XOR gate output, **SUM-XNOR:** Both XNOR gate and SUM output.



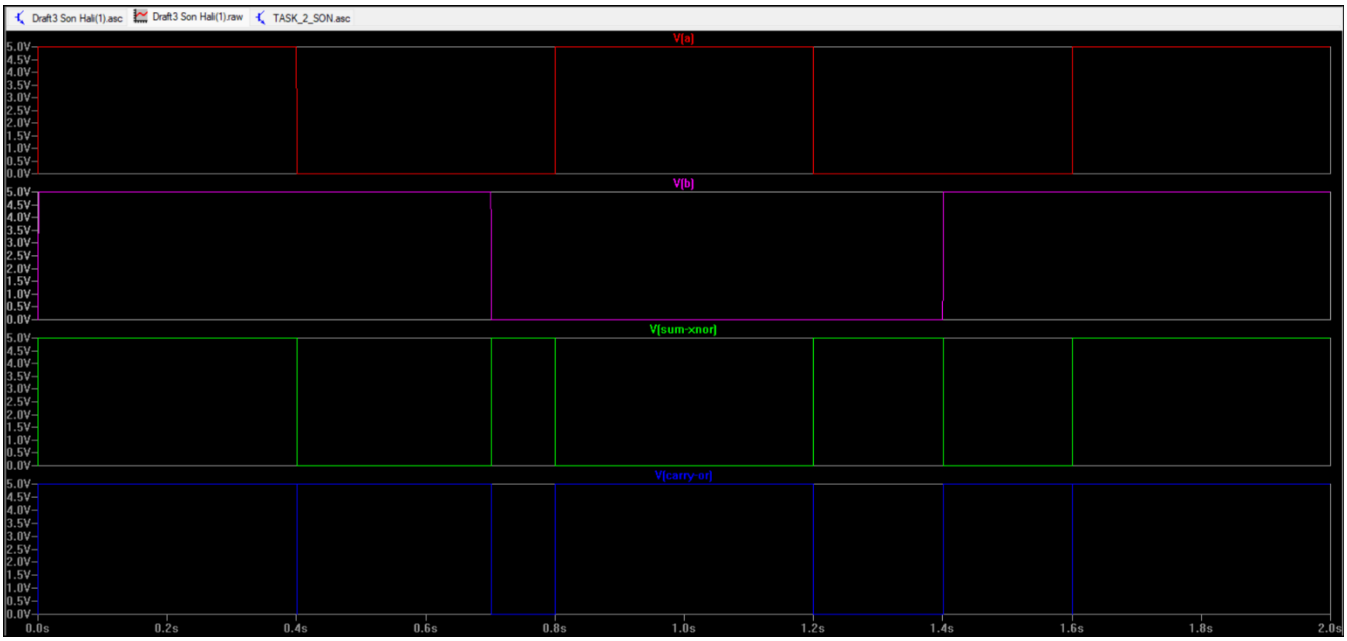
(Figure 3.1 | The output graph of the gates)

As seen in Figure 3.1, the graph window shows us graphs of the outputs of cmos gates in the circuit. Accorcing to Figure 1.2 Turuth Table, the outputs of the gates are as what they should be. In the graph, the outputs from XOR, AND, OR, AND gates and Sum and Carry outputs are shown seperately. It is obvious that the low voltage level is 0V while the high voltage level is 5V as they should be.



(Figure 3.2 | The outputs of cmos logic gates)

As seen in Figure 3.2, the graph window shows us graphs of the outputs of cmos logic gates in the circuit. Accorcing to Figure 1.2 Turuth Table, the outputs of the gates are as what they should be. In the graph, the outputs from XOR, AND, OR, AND gates are shown seperately. It is obvious that the low voltage level is 0V while the high voltage level is 5V as they should be. Because of falling and rising edges in the graphs, some unwanted lines can come out as seen in the OR gate graph.



(Figure 3.3 | The outputs of the sum and carry)

As seen in Figure 3.3, the graph window shows us graphs of the outputs of cmos logic gates in the circuit. Accorcing to Figure 1.2 Turuth Table, the outputs of the gates are as what they should be. In the graph, the outputs of the sum and carry are shown seperately. It is obvious that the low voltage level is 0V while the high voltage level is 5V as they should be.

C. RESULTS AND DISCUSSION

A	B	Cin	Sum (S)	Cout
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

(Figure 4.1 | Truth Table of Selected Full Adder)

The CMOS complete adder circuit's functionality in carrying out binary addition operations was confirmed by the positive findings of the SPICE simulation. With Cin fixed at '1', the simulation showed that the circuit accurately produced the sum and carry outputs in accordance with the given inputs. The output waveforms showed the anticipated behavior, which suggested that the complete adder was operating correctly within the settings that were intended.

As seen in the graphs above, the outputs of the gates are what they should be as in the truth table in Figure 4.1.

The CMOS full adder circuit's applicability for the uneven seven-sided dice roller system is validated by the successful simulation results. The circuit performs binary addition jobs well because it uses a CMOS architecture that combines both PMOS and NMOS transistors.

Overall, the simulation results demonstrate the CMOS complete adder circuit's dependability and durability, emphasizing its critical function in permitting binary addition in the uneven seven-sided dice roller system. The system's computational capabilities can now be developed and optimized with a strong basis thanks to this effective implementation.