CSGE602055 Operating Systems
CSF2600505 Sistem Operasi
Week 05

Rahmat M. Samik-Ibrahim

University of Indonesia at Lenteng Agung

http://rahmatm.samik-ibrahim.vlsm.org/

REV03 04-Oct-2016

Week 05: Memory

Memory

- Reference: (OSCE2e ch7/8) (UCB 11 12 13) (UDA P3L2) (OLD 06)
- Binding & Linking
  - Address Binding
  - Address Space: Logical & Physical
  - Dynamic & Static Linking
  - MMU: Memory Management Unit
  - Base and Limit Registers
  - Swapping
  - Mobile Systems Problem: no swap
- Memory Allocation
  - Contiguous Allocation
  - Multiple-variable-partition Allocation
  - First, Best, Worst Fit Allocation Strategy
- Fragmentation
  - External
  - Internal
  - Compaction

Paging

- Address Space
- Logical/Virtual Address
- Pages
- Page Number
- Page Offset
- Page Table
- PTE: Page Table Entry
- Page Flags: Valid/ Invalid
- TLBs: Translation Look-aside Buffers/ Associative Memory
- Physical Address
- Frames

Address Translation Scheme

Example (Address Translation Scheme)

00	00000	0	0000	00	000	000	00	0000	0
01	00001		0001		001		01		1
02	00010		0010		010		10	0001	0
03	00011		0011		011		11		1
04	00100		0100		100	001	00	0010	0
05	00101		0101		101		01		1
06	00110		0110		110		10	0011	0
07	00111		0111		111		11		1
08	01000		1000	01	000	010	00	0100	0
09	01001		1001		001		01		1
0A	01010		1010		010		10	0101	0
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1D	11101	1	1101	11	101	111	01	1110	1
1E	11110		1110		110		10	1111	0
1F	11111		1111		111		11		0

Hierarchical Page Table

- OPT: outer page table (P1)
- PT: page table (P2)
- Offset (D)
- Three-level Paging Scheme
- Hashed Page Tables
- Inverted Page Table

VM

- Demand Paging
- COW
- Page Replacement
- Frame Allocation
- Kernel

Lab

- Lab
  - top
  - malloc()
  - system()

The End

- This is the end of the presentation.