Monday, January 10, 2011

Memory Module with A Memory Controller

##Here is the VHDL code for the Memory Controller
3####3##

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity Controller is
 port( read_write,ready,clock,reset: in std_logic;
       oe,we                 : out std_logic);

end Controller;

architecture Behavioral of Controller is
type Statetype is (idle,decision,read1,write1);
signal presentstate, nextstate : Statetype;
begin

   process(presentstate,read_write,ready)
             begin

       case presentstate is
```

```
            when idle => oe<='0'; we<='0';
                 if ready='1'  then
                   nextstate<=decision;
                 else
                   nextstate<=idle;
                 end if;

            when decision => oe<='0'; we<='0';
                 if(read_write='1')  then
                    nextstate<=read1;
                 else
                    nextstate<=write1;

                 end if;

            when  read1=> oe<='1'; we<='0';

                  if (ready='1') then
                      nextstate<=idle;
                  else
                     nextstate<=read1;
                  end if;

            when  write1 => oe<='0'; we<='1';
          if (ready='1') then
        nextstate <=idle;
      else
                      nextstate<=write1;
                   end if;

            end case;


  end process;



      process(reset,clock)
  begin


    if reset='1' then
     presentstate<=idle;

    elsif(clock'event and clock='1') then
    presentstate<=nextstate;
  end if;


 end process;


end Behavioral;
```

##

Here is the VHDL code for the top module

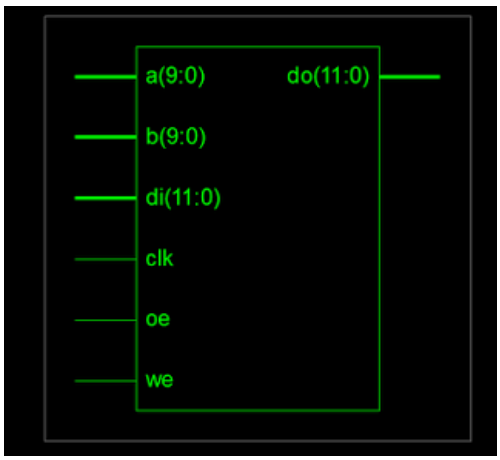
##

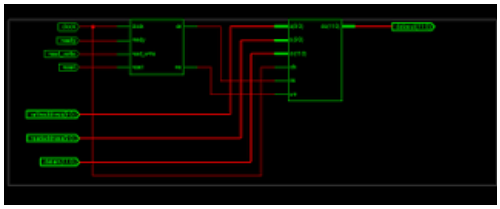
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
```

```
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity ControllingRAM is

port (
      clock : in std_logic;
      datain : in std_logic_vector(11 downto 0);
  dataout : out std_logic_vector(11 downto 0);
      writeaddress : in std_logic_vector(9 downto 0);
      readaddress   : in std_logic_vector(9 downto 0);
      read_write    : in std_logic;
  ready         : in std_logic;
  reset         : in std_logic);

end ControllingRAM;

architecture Behavioral of ControllingRAM is

component Controller is

 port( read_write,ready,clock,reset: in std_logic;
       oe,we                 : out std_logic);

end component;

component RAM1KB is

port (clk : in std_logic;
        oe    : in std_logic;
        we  : in std_logic;
        a   : in std_logic_vector(9 downto 0);
        b   : in std_logic_vector(9 downto 0);
        di  : in std_logic_vector(11 downto 0);
        do  : out std_logic_vector(11 downto 0));


end component;

signal oetemp: std_logic;
signal wetemp: std_logic;

begin


u1: RAM1KB port map (

      clk => clock ,
        oe   => oetemp,
        we  =>  wetemp,
        a   =>  writeaddress,
        b   =>  readaddress,
        di  =>  datain,
        do  =>  dataout

       );

u2: Controller port map
   (

     read_write => read_write,
   ready =>   ready,
   clock =>   clock,
   reset =>    reset,
```

```
    oe =>       oetemp,
  we =>       wetemp


    );

end Behavioral;
```

##





Posted by amr nasr at 1:30 AM
Email ThisBlogThis!Share to TwitterShare to FacebookShare to Pinterest
Labels: Memory Controller, RAM

Newer Post Older Post Home

Your IP and Google Map location

Freelancer Sites

- Embedded Software Blog
- HDfpga
- Mobile Dev & Design
- vhdlguru
- electronics-tech.com
- Virtex-5 Resource
- Xilinx, Inc.
- fpga4fun
- Verilog / VHDL Projects
- OpenCores
- Linux Wiki

VHDL Active Bloggers

- Dangerous Prototypes

- FPGA Developer
- The Digital Electronics Blog
- Reconfigurable Computing
- Final Year Projects by "www.IndianEngineer.in"
- vhdlguru
- IndianEngineer
- Chip Design Magazine
- vlsibank
- OutputLogic.com
- Digital Puzzles and Challenges
- FPGA and DSP from scratch
- FPGA from Scratch
- 第4836页 程序源码搜索引擎 - HackChina.com
- VLSI FORUM
- Digital Design Projects
- Essential VHDL: VHDL Design Examples
- FPGA - -Verilog www.pudn.com

Followers