RTL Design of DDR SDRAM Controller using Verilog

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Abstract

This project work is a working implementation of High Speed DDR (Double Data Rate) SDRAM Controller. The DDR Synchronous Dynamic RAM is an enhancement to the conventional SDRAM running at bus speed over 75MHz. The DDR SDRAM (referred to as DDR) doubles the bandwidth of the memory by transferring data twice per cycle on both the rising and falling edges of the clock signal. The designed DDR Controller supports data width of 64 bits, Burst Length of 4 and CAS (Column Address Strobe) latency of 2. DDR Controller provides a synchronous command interface to the DDR SDRAM Memory along with several control signals. In this paper, the implementation has been done in Verilog HDL by using Xilinx ISE 9.2i and Modelsim 6.4b.

Keywords- Double Data Rate, Column Address Strobe (CAS), Synchronous Dynamic RAM.

1. Introduction

With the rapid development in the processor's family, speed and capacity of a memory device is a major concern. The DDR is an enhancement to the traditional synchronous DRAM. The DDR is able to transfer the data on both the edges of each clock cycle. Thus doubling the data transfer rate of the memory device. The DDR is available in a very low cost that's why it is widely used in personal computers where they are basically used to provide the functions of storage and buffers. The DDR SDRAM supports the data widths of 16, 32 and 64 bits. It automatic refresh during the normal and power down modes. The DDR is a complete synchronous implementation of controller. It increases the throughput using command pipelining and bank management.

This paper is organized as follows. In Section 2, Block diagram of DDR controller will be described. The architecture of DDR controller will be described in Section 3. In Section 4, different functional blocks will be explained. Finally the Result and Conclusion will be given in Section 5 and Section 6 respectively.

2. DDR controller Block Diagram

Figure 1 shows the different blocks in top level reference design. The user interface module contains the I/O registers to latch system signals coming into the FPGA. The DDR controller module contains the DDR SDRAM controller, including the I/Os to interface with the DDR SDRAM.

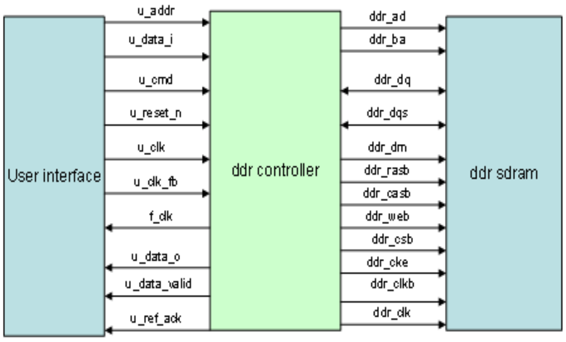

Figure 1: Top Level block diagram

3. DDR Controller Architecture

The DDR Controller mainly consists of four functional blocks:

1. Address Latch
2. Data Path
3. Controller
4. Counter

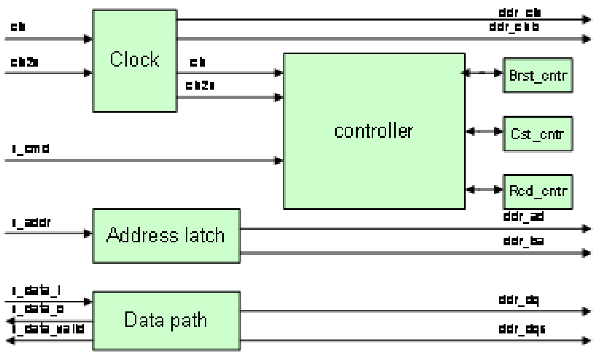

Figure 2: DDR Controller Architecture

4. Different Functional Blocks

A. Address Latch

The basic function of address latch module is to gets its control signals from the controller and generates row, column and bank addresses for the DDR SDRAM. The address latch also generates different control signals like burst_max, cas_lat_max for the burst counter and cas latency counter.

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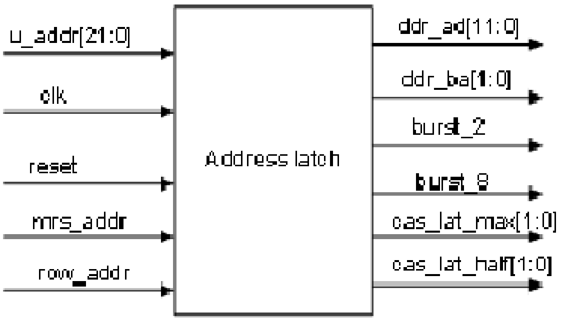

Figure 3: Address Latch Module

B. Data Path

One of the most difficult aspects of DDR SDRAM controller design is to transmit and capture data at double data rate. This module transmits data to the memories. The basic function of data path module is storing the write data and calculates the value for read data path.

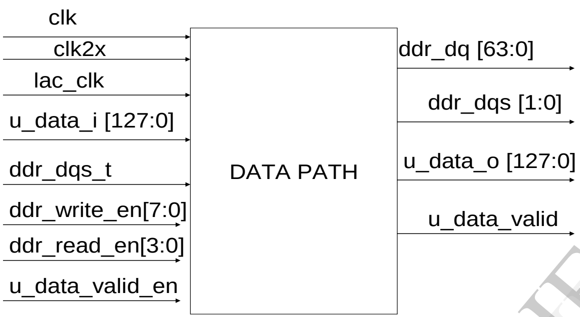

Figure 4: Data Path Module

Data path module handles all the data generation and sampling task of DDR controller. For Read access, data is sampled by data path. Data is then synchronized with the internal clock and transferred to the user interface one-word per clock cycle as normal data rate. For Write access, data is received from the user interface at the normal one word per clock data rate. The DDR controller's data path then resynchronized the data and transfers them using the double data rate.

C. Controller

The controller consists of a state machine which performs DDR SDRAM read and write accesses based on user interface request. The controller consists of a high performance timing & control state machine that observes all timing requirements and issues the commands to the memory devices at the shorted time possible. The pin diagram of controller is shown in figure 5:

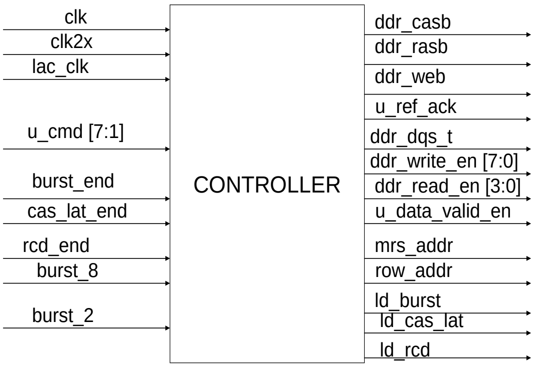

Figure 5: Controller Module

The DDR controller consists of a high performance memory controller for system requiring access to external devices with lowest latency and highest throughput. The controller accepts and decodes user interface commands and generates read, write, refresh commands. It also generates signals for other modules. The memory is initialised and powered up using a defined process. The controller state machine handles the initialization process upon power up.

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D. Controller state machine diagram

Initially the controller is in the IDLE state. That means no operation is performing. A PRECHARGE ALL command is then applied. This command is used to deactivate any open row in a bank or the open bank row in all banks. Once a bank is precharged, it is in idle state and must be activated prior to any READ and WRITE operation. Next a LOAD MODE REGISTER command should be issued for the extended mode register to enable the DLL, then another LOAD MODE REGISTER command to the mode register to reset the DLL and to program the operating parameters. Again a PRECHARGE command should be applied which place the device in all banks in IDLE state. In the IDLE state two AUTO REFRESH cycles must be performed.

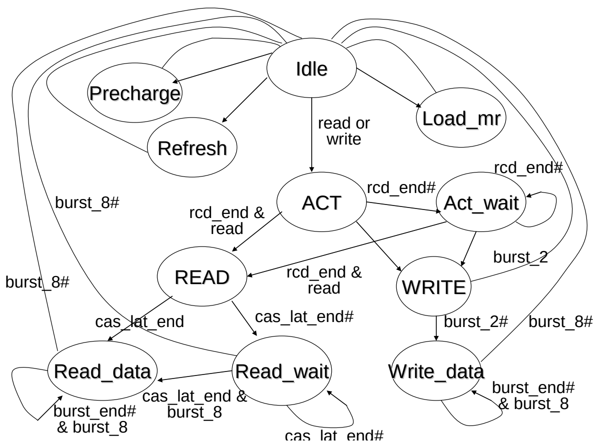

Figure 6: controller state machine diagram

The controller next state could be PRECHARGE, LOAD_MR, REFRESH or ACT, depending upon the required command. The ACT command is used to open a row in a bank before starting any read or write operation. The controller state machine diagram is shown in figure below:

E. Counter

The task of Burst Count is to count when there are consecutive READ and WRITE operations. While doing consecutive READ and WRITE operations, the Burst_count value determines when the next READ and WRITE command should be issued.

5. Result

Figure 7 shows the RTL schematic of designed DDR SDRAM controller.

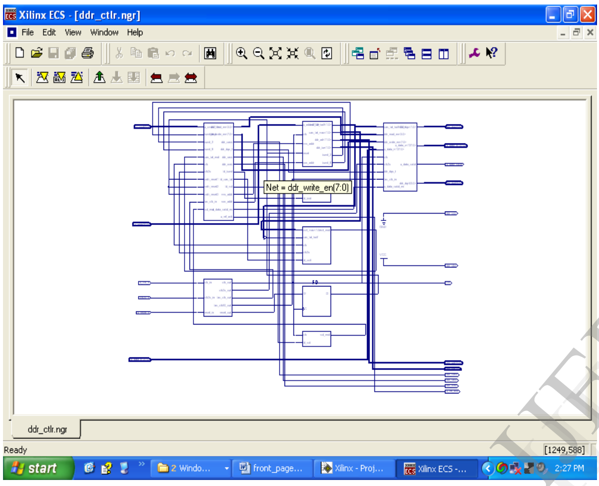

Figure 7: RTL schematic of DDR Controller

The following figures are the simulation result of controller, controller Write cycle and controller Read cycle obtained by using Modelsim 6.4b.

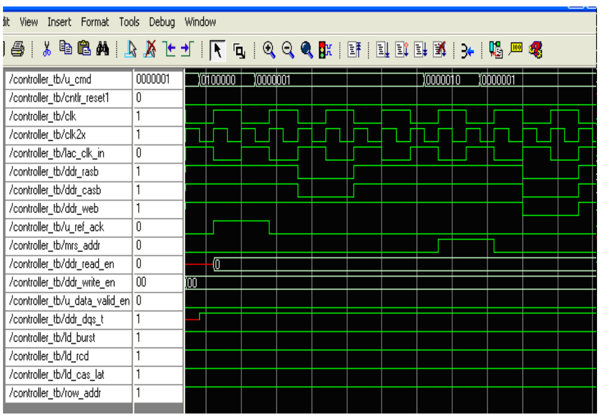

Figure 8: Simulation waveform for Controller

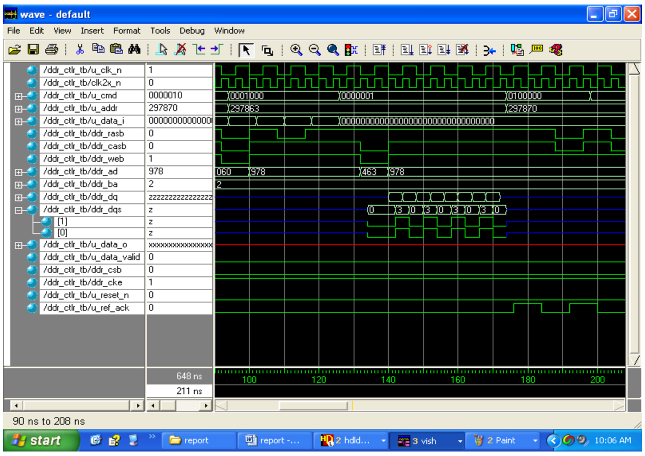

Figure 9: Simulation waveform for Controller Write Cycle

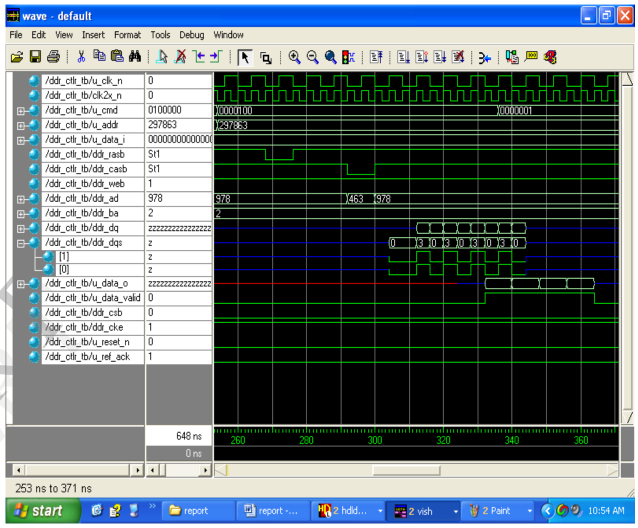

Figure 10: Simulation waveform for Controller Read Cycle

6. Conclusion

In this paper an efficient fully functional DDR SDRAM controller is designed. The controller generates different types of timing and control signals, which synchronises the timing and control the flow of operation. The memory system operates at double the frequency of processor, without affecting the performance. Thus we can reduce the data bus size. The drawback of this controller is complex schematic with large number of buffers in the circuit increases the amount of delay.

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