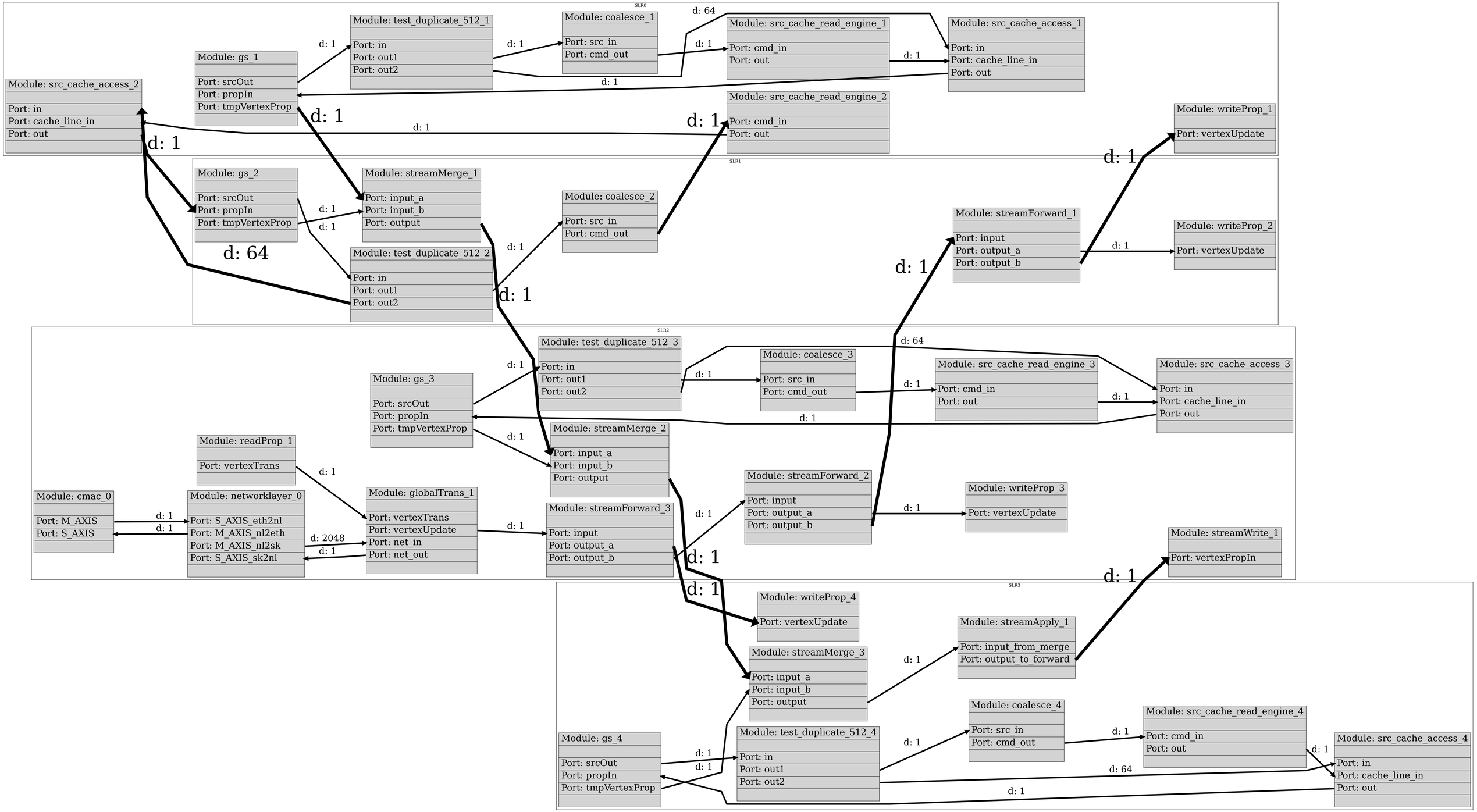
SLR0
Module: test_duplicate_512_1
Port: in
Port: out1
Port: out2
Module: coalesce_1
Port: src_in
Port: cmd_out
Module: src_cache_read_engine_1
Port: cmd_in
Port: out
Module: src_cache_access_1
Port: in
Port: cache_line_in
Port: out
Module: gs_1
Port: srcOut
Port: propIn
Port: tmpVertexProp
Module: src_cache_access_2
Port: in
Port: cache_line_in
Port: out
Module: src_cache_read_engine_2
Port: cmd_in
Port: out
Module: writeProp_1
Port: vertexUpdate
SLR1
Module: gs_2
Port: srcOut
Port: propIn
Port: tmpVertexProp
Module: streamMerge_1
Port: input_a
Port: input_b
Port: output
Module: test_duplicate_512_2
Port: in
Port: out1
Port: out2
Module: coalesce_2
Port: src_in
Port: cmd_out
Module: streamForward_1
Port: input
Port: output_a
Port: output_b
Module: writeProp_2
Port: vertexUpdate
SLR2
Module: test_duplicate_512_3
Port: in
Port: out1
Port: out2
Module: coalesce_3
Port: src_in
Port: cmd_out
Module: src_cache_read_engine_3
Port: cmd_in
Port: out
Module: src_cache_access_3
Port: in
Port: cache_line_in
Port: out
Module: gs_3
Port: srcOut
Port: propIn
Port: tmpVertexProp
Module: streamMerge_2
Port: input_a
Port: input_b
Port: output
Module: readProp_1
Port: vertexTrans
Module: cmac_0
Port: M_AXIS
Port: S_AXIS
Module: networklayer_0
Port: S_AXIS_eth2nl
Port: M_AXIS_nl2eth
Port: M_AXIS_nl2sk
Port: S_AXIS_sk2nl
Module: globalTrans_1
Port: vertexTrans
Port: vertexUpdate
Port: net_in
Port: net_out
Module: streamForward_3
Port: input
Port: output_a
Port: output_b
Module: streamForward_2
Port: input
Port: output_a
Port: output_b
Module: writeProp_3
Port: vertexUpdate
Module: streamWrite_1
Port: vertexPropIn
SLR3
Module: writeProp_4
Port: vertexUpdate
Module: streamApply_1
Port: input_from_merge
Port: output_to_forward
Module: streamMerge_3
Port: input_a
Port: input_b
Port: output
Module: coalesce_4
Port: src_in
Port: cmd_out
Module: src_cache_read_engine_4
Port: cmd_in
Port: out
Module: gs_4
Port: srcOut
Port: propIn
Port: tmpVertexProp
Module: test_duplicate_512_4
Port: in
Port: out1
Port: out2
Module: src_cache_access_4
Port: in
Port: cache_line_in
Port: out
d: 1
d: 64
d: 2048