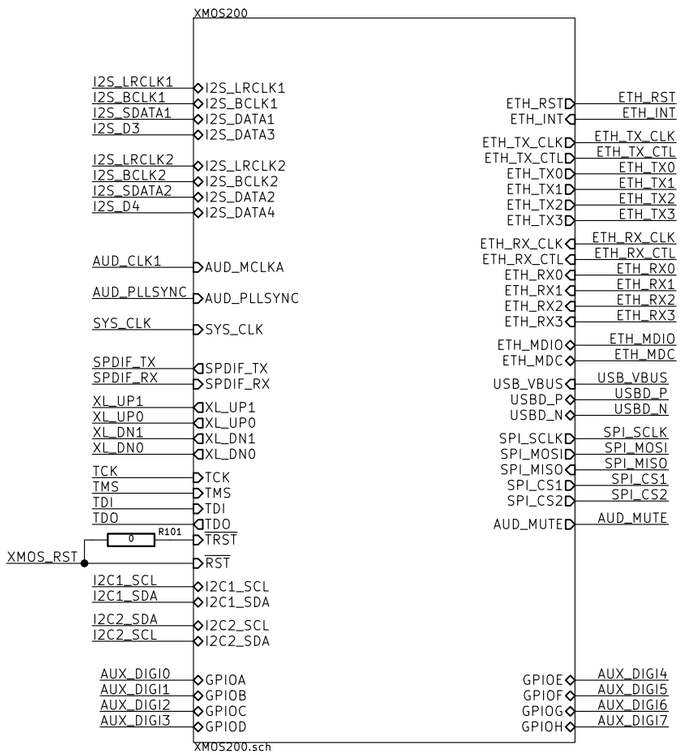
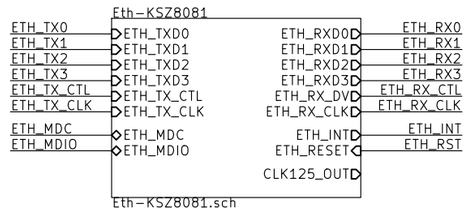
Open Hardware DSP Platform – www.ohdsp.org
CoreOne – xCORE200 Platform
Revision 2.1

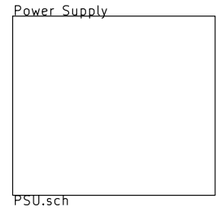
XMOS 200



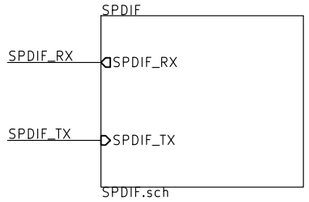
Ethernet



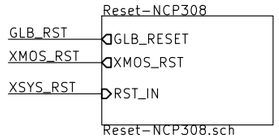
Power supply



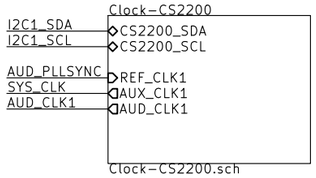
SPDIF



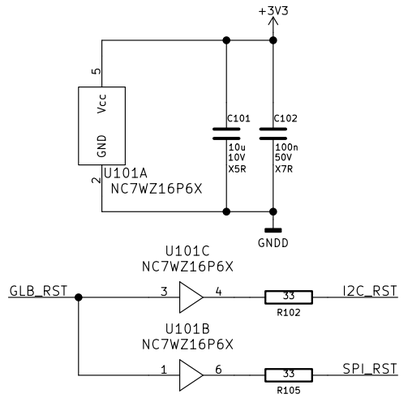
Reset control



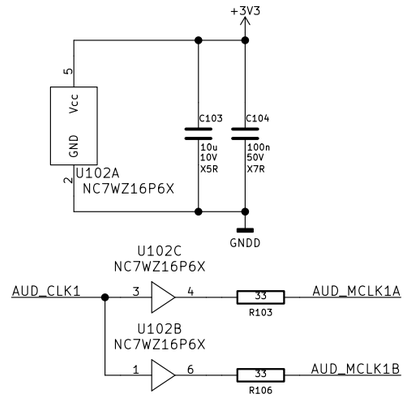
Clock generator



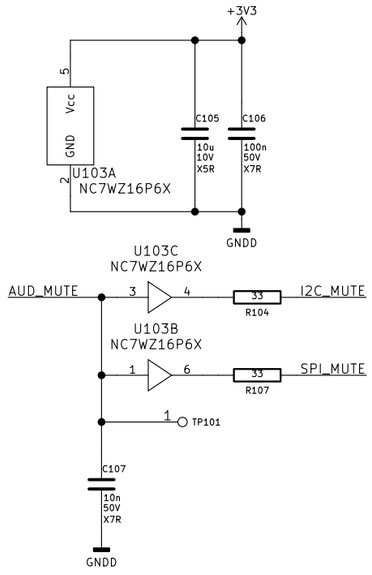
External reset buffer



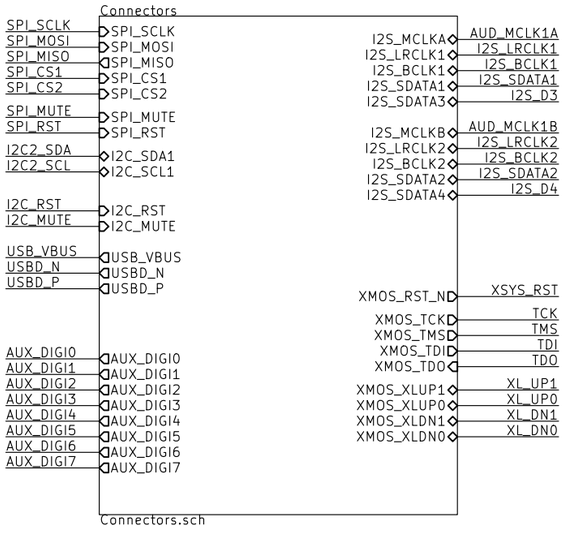
Audio clock buffer



External mute buffer



Connectors



Notes:

All digital I/O is 3V3. Use outside this voltage can cause damage.

See bill of materials for detailed parts information.

Trace impedance on SPI/I2C, MCLK, and I2S is designed for approx 89ohm.
26AWG ribbon cable used with Ground–Signal–Ground is approx 89ohm.

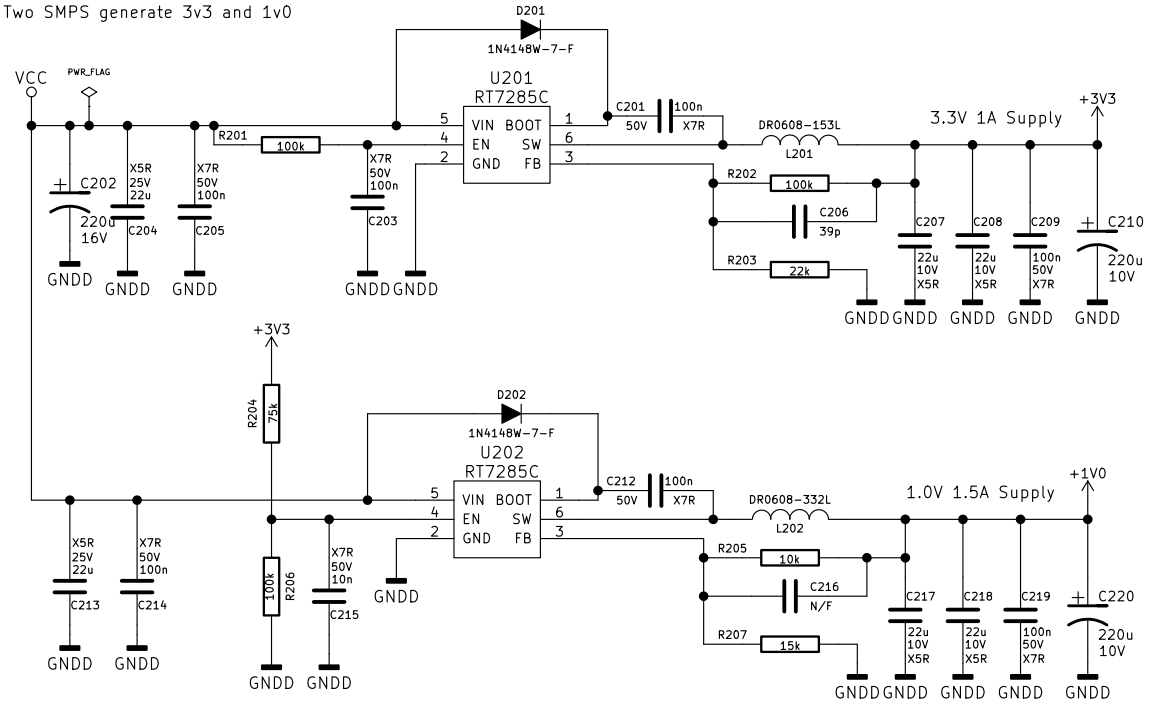
Sheet: /
File: CoreOne–xCORE200–2.1.sch

Title: CoreOne – xCORE200 Platform

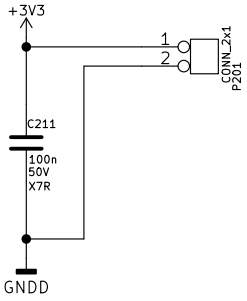
Size: A3	Date: 2019–04–04	**Rev: 2.1**
KiCad E.D.A. kicad (5.1.0)–1		Id: 1/8

Power Supply

Two SMPS generate 3v3 and 1v0

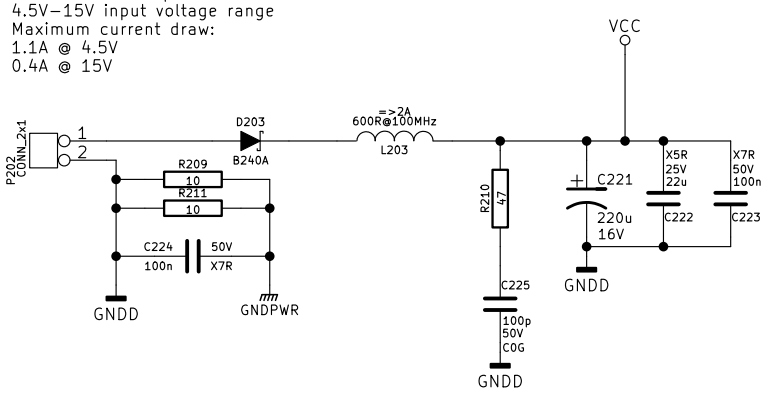


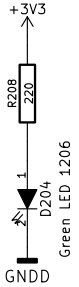
External 3V3 connection
Do not overload!
Recommend 100mA max



Power Input

4.5V–15V input voltage range
Maximum current draw:
1.1A @ 4.5V
0.4A @ 15V





Mounting Holes and Fiducials

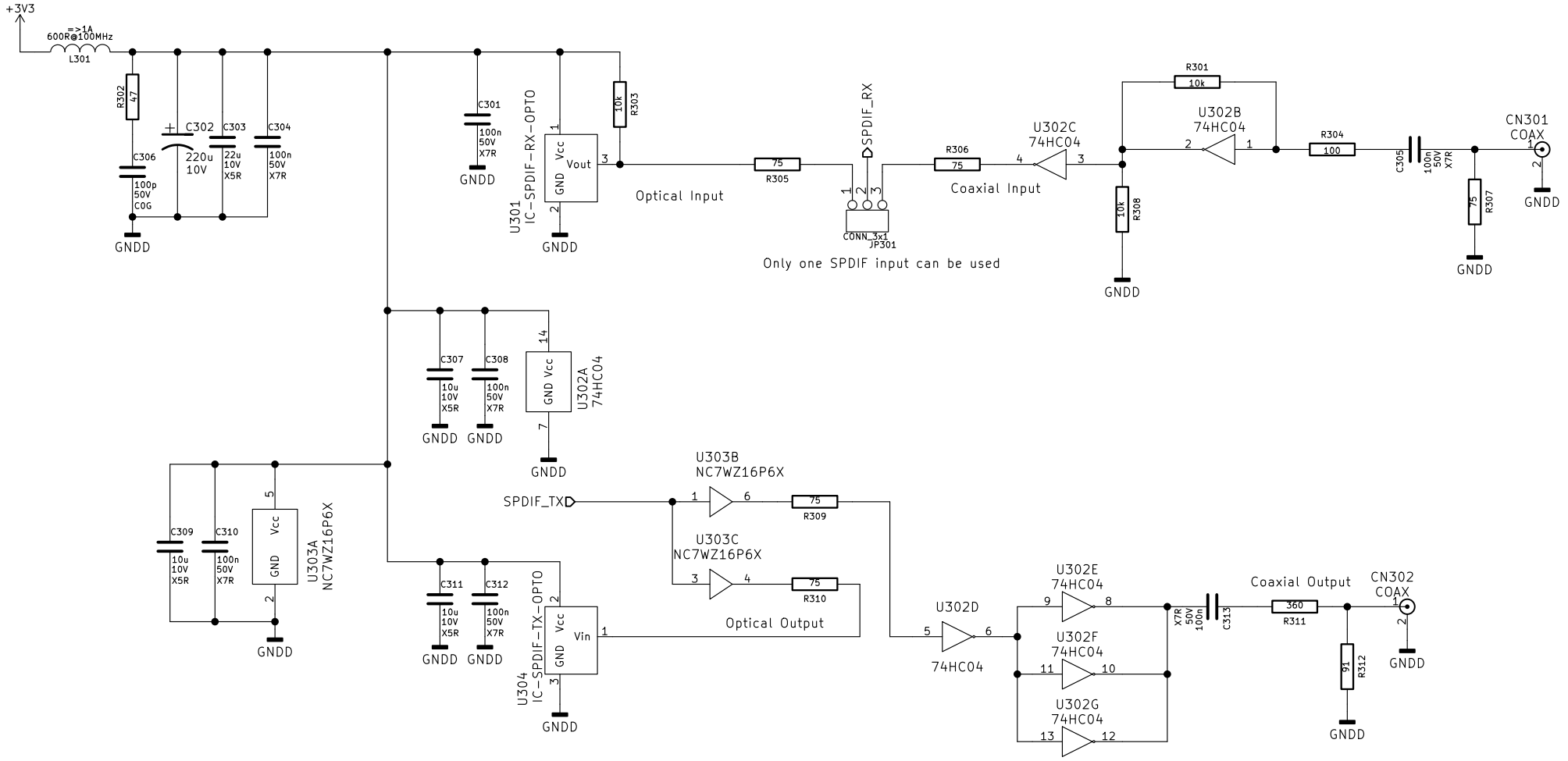
MNT201 MNT202 FID201 FID202 FID204 FID206
MNT203 MNT204 FID203 FID205

Sheet: /Power Supply/
File: PSU.sch

Title: CoreOne – xCORE200 Platform

Size: A4	Date: 2019-04-04	**Rev: 2.1**
KiCad E.D.A. kicad (5.1.0)-1		Id: 2/8

SPDIF Inputs and Outputs – Optical and Coaxial



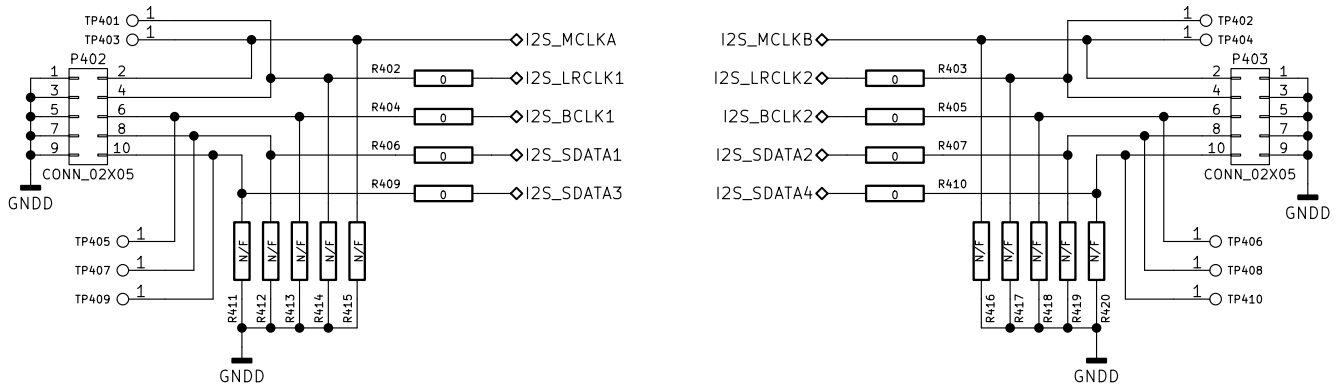
Sheet: /SPDIF/
File: SPDIF.sch

Title: CoreOne – xCORE200 Platform

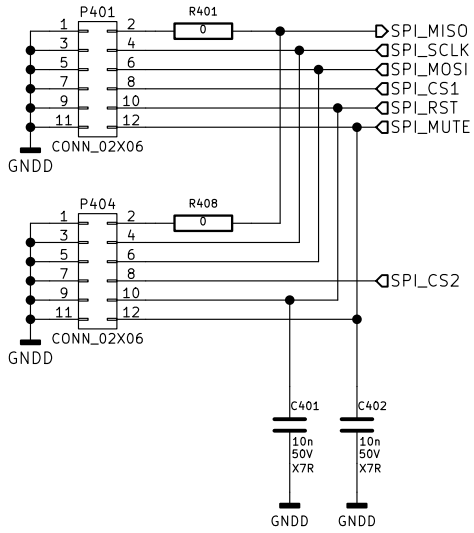
Size: A4	Date: 2019-04-04	**Rev: 2.1**
KiCad E.D.A. kicad (5.1.0)-1		Id: 3/8

Connectors

I2S Connectors

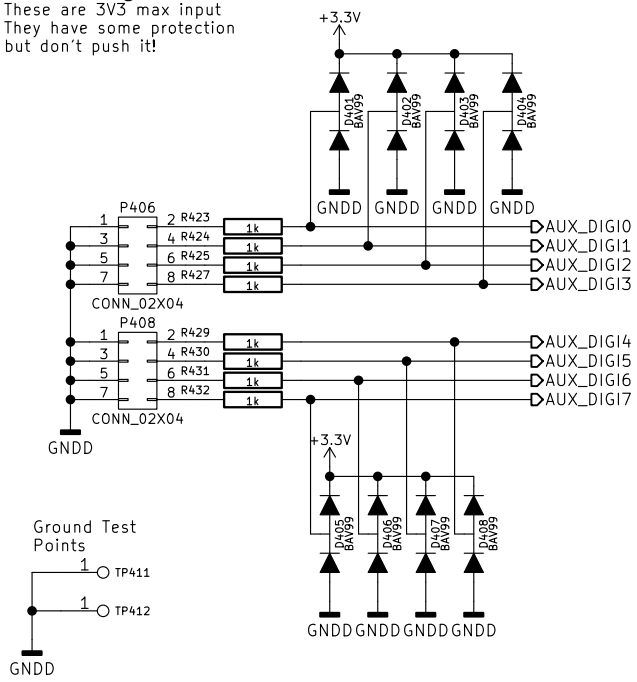


SPI Ports

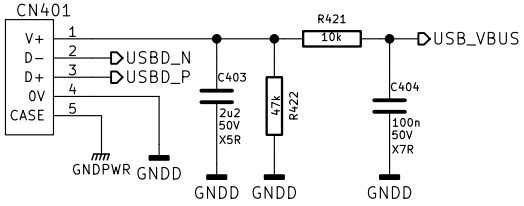


AUX Digital I/O

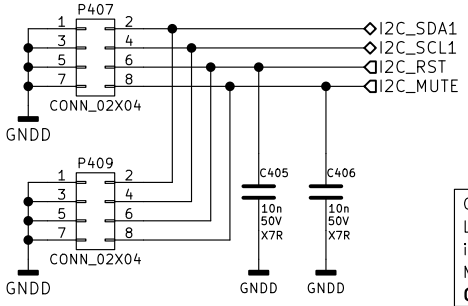
These are 3V3 max input
They have some protection
but don't push it!



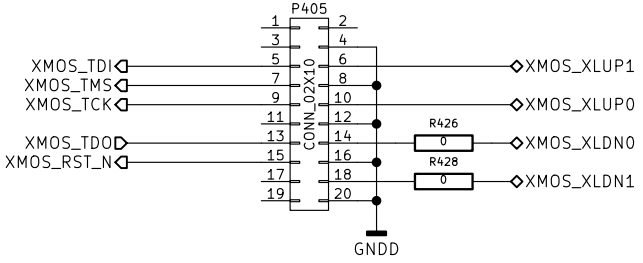
USB Port



I2C Ports



XMOS xSYS Interface Programming/Debug



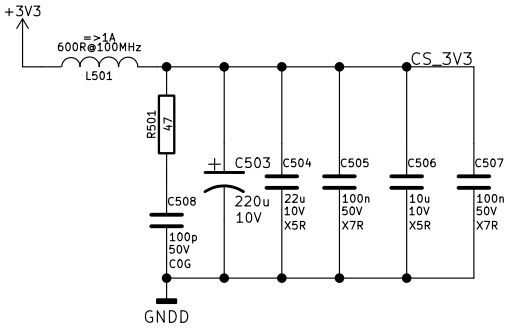
Sheet: /Connectors/
File: Connectors.sch

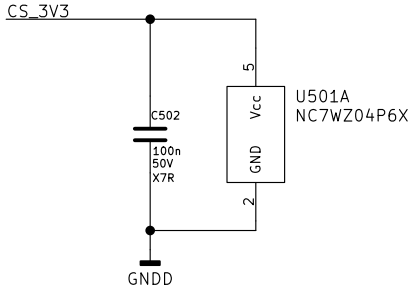
Title: CoreOne – xCORE200 Platform

Size: A4	Date: 2019-04-04	**Rev: 2.1**
KiCad E.D.A. kicad (5.1.0)-1		Id: 4/8

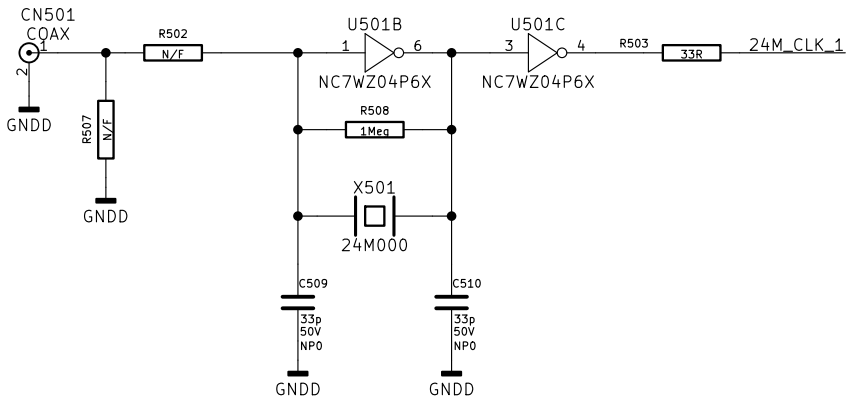
System and Audio Clocks

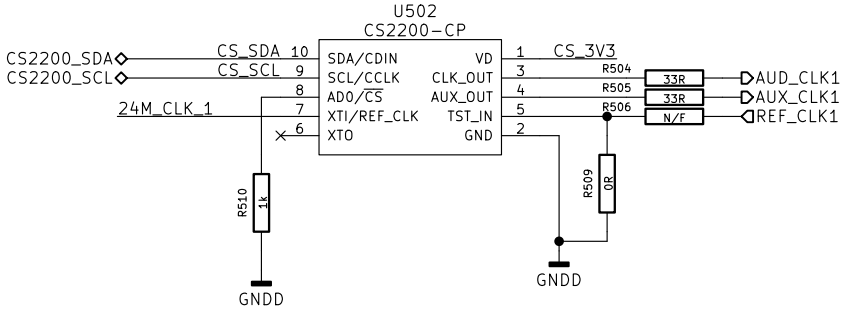
Note: Two controlled clocks are provided to allow two audio clock domains.
Both clocks are fed from the same crystal. If U502 and/or U503 are fitted as
CS2100-CP parts then the clocks can be run from the REF_CLK signals to
synchronise the clocks to the AUD_PLLSYNC signal from U801.





External Clock Input



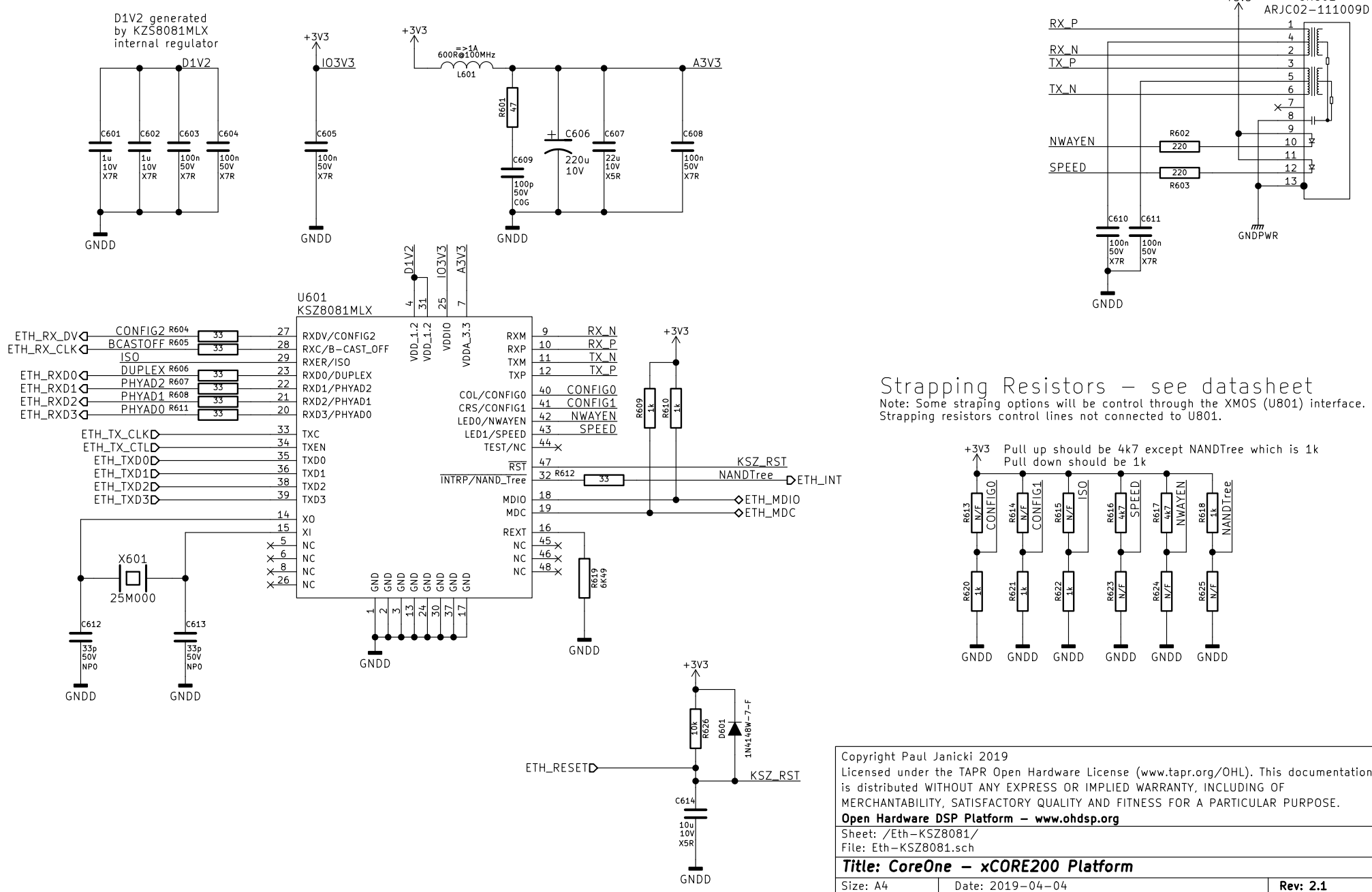


Sheet: /Clock-CS2200/
File: Clock-CS2200.sch

Title: CoreOne – xCORE200 Platform

Size: A4	Date: 2019-04-04	**Rev: 2.1**
KiCad E.D.A. kicad (5.1.0)-1		Id: 5/8

Ethernet – KSZ8081 10/100Meg Base-TX



Strapping Resistors – see datasheet

Note: Some straping options will be control through the XMOS (U801) interface.
Strapping resistors control lines not connected to U801.

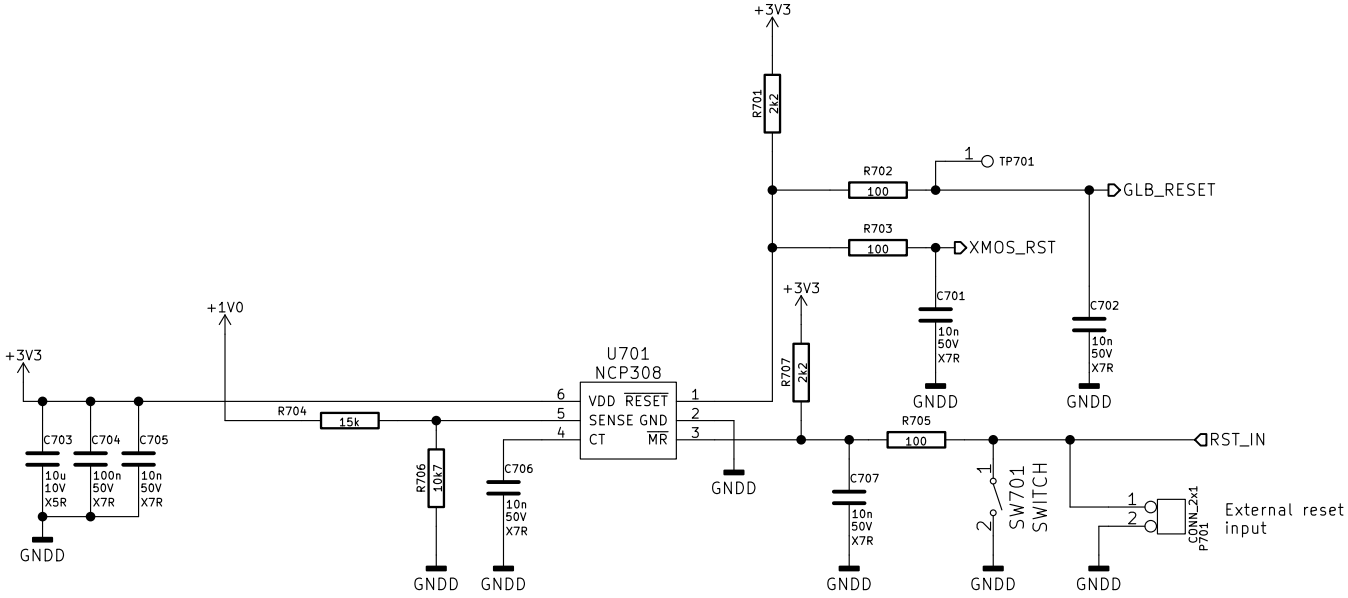
Sheet: /Eth-KSZ8081/
File: Eth-KSZ8081.sch

Title: CoreOne – xCORE200 Platform

Size: A4	Date: 2019-04-04	**Rev: 2.1**
KiCad E.D.A. kicad (5.1.0)-1		Id: 6/8

Voltage Monitor Reset

Generate a global reset based on 1V0 voltage rail.
Use NCP308SNADJT1G adjustable version.
Supports external reset signal.



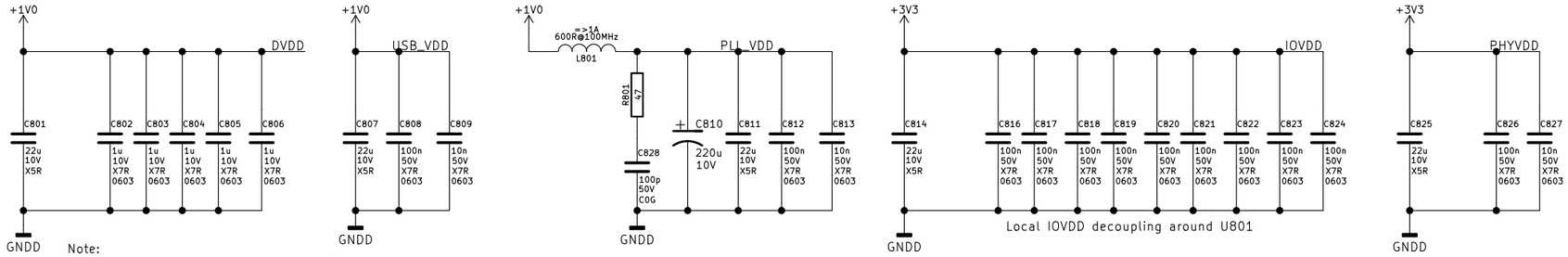
Sheet: /Reset-NCP308/
File: Reset-NCP308.sch

Title: CoreOne – xCORE200 Platform

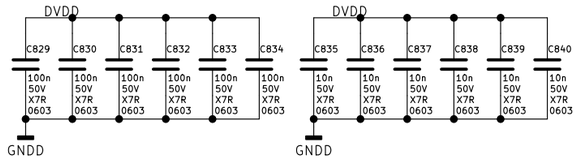
Size: A4	Date: 2019-04-04	**Rev: 2.1**
KiCad E.D.A. kicad (5.1.0)-1		Id: 7/8

XMOS 200 – XE216-512-TQ128 or XEF216-512-TQ128

Note: Can use XE216-512-TQ128 or XEF216-512-TQ128. XEF216-512-TQ128 has internal flash memory so do not fit SPI flash memory U802.

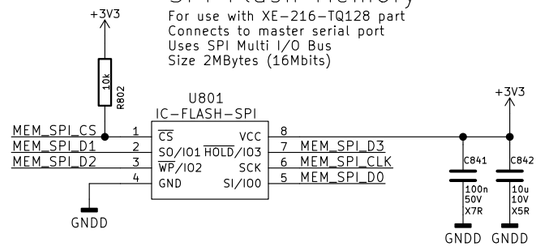


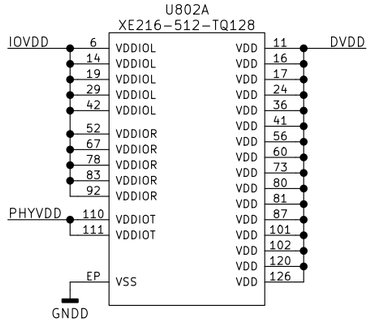
Local DVDD decoupling around U801

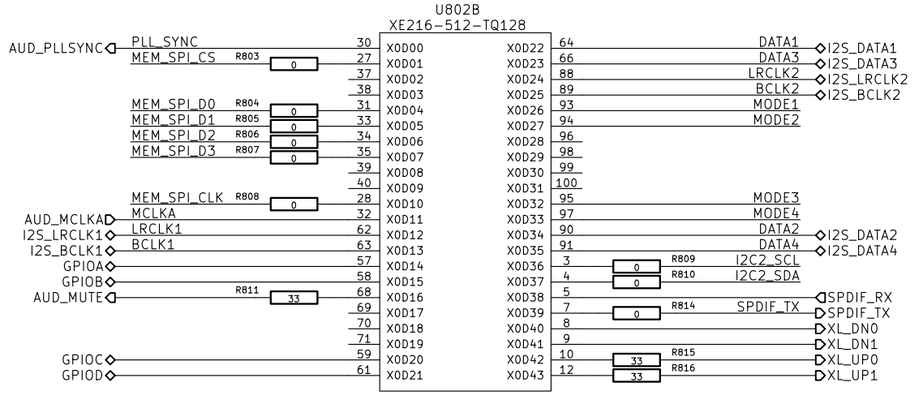


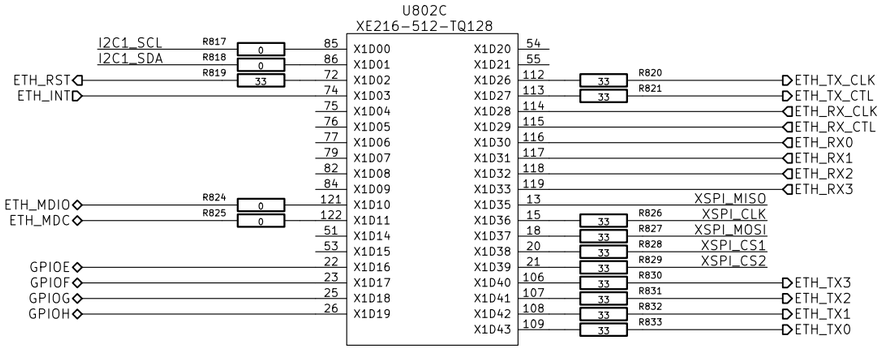
SPI Flash Memory

For use with XE-216-TQ128 part
Connects to master serial port
Uses SPI Multi I/O Bus
Size 2MBytes (16Mbits)



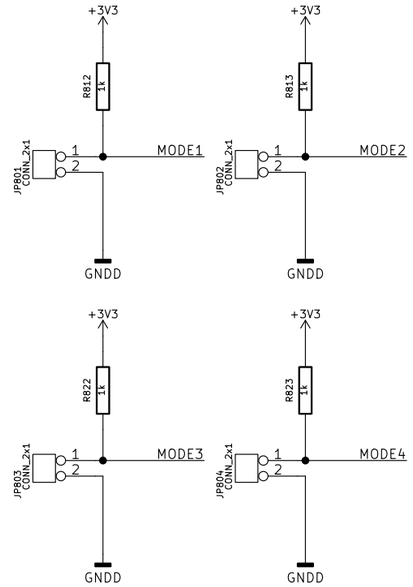






Mode Select Jumpers

To allow configuration options to be hardware selected



Control ports

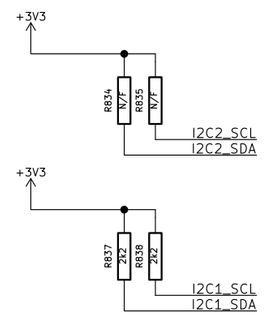
I2C

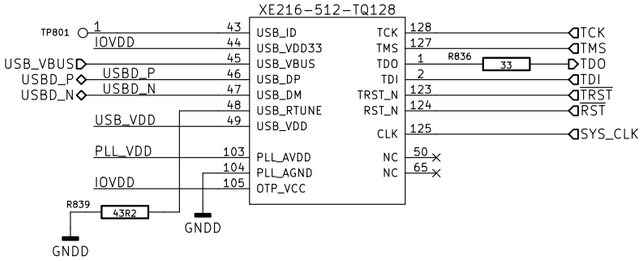
I2C1_SCL ◇ I2C1_SCL
I2C1_SDA ◇ I2C1_SDA
I2C2_SCL ◇ I2C2_SCL
I2C2_SDA ◇ I2C2_SDA

SPI

SPI_MISO ◇ XSPI_MISO
SPI_SCLK ◇ XSPI_CLK
SPI_MOSI ◇ XSPI_MOSI
SPI_CS1 ◇ XSPI_CS1
SPI_CS2 ◇ XSPI_CS2

I2C Pull-ups





Sheet: /XMOS200/
File: XMOS200.sch

Title: CoreOne – xCORE200 Platform

Size: A3	Date: 2019-04-04	**Rev: 2.1**
KiCad E.D.A. kicad (5.1.0)-1		Id: 8/8