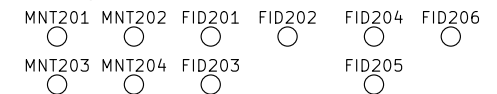
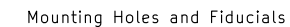
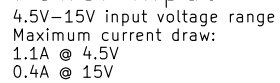
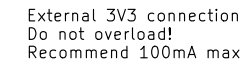


Notes:  
All digital I/O is 3V3. Use outside this voltage can cause damage.

See bill of materials for detailed parts information.

Trace impedance on SPI/I2C, MCLK, and I2S is designed for approx 89ohm. 26AWG ribbon cable used with Ground-Signal-Ground is approx 89ohm.

Two SMPS generate 3v3 and 1v0

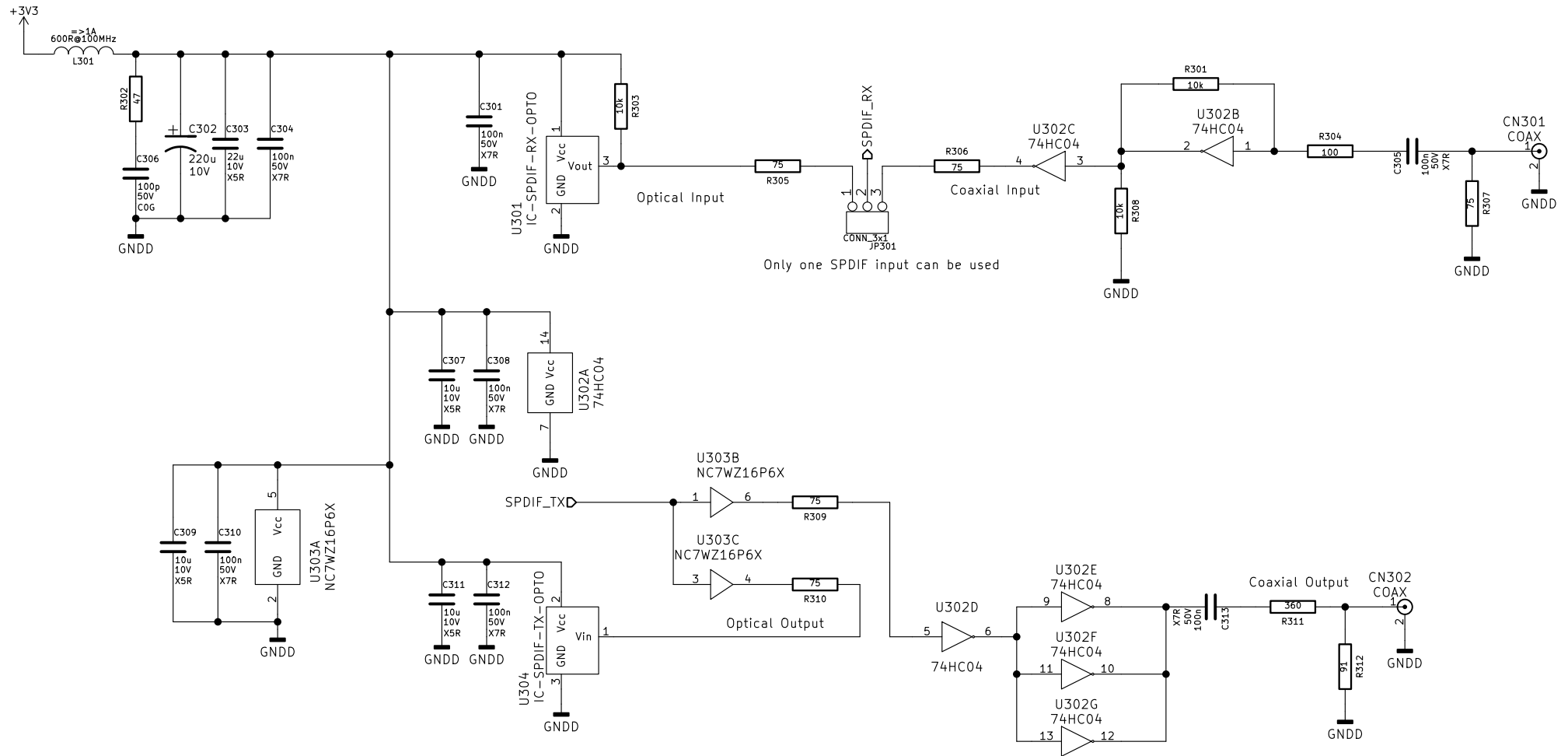


Licensed under the TAPR Open Hardware License ([www.tapr.org/OHL](http://www.tapr.org/OHL)). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.

Size: A4	Date: 2019
KiCad E.D.A.	kicad (5.1.0)-1

Id: 2/8

# SPDIF Inputs and Outputs – Optical and Coaxial



Copyright Paul Janicki 2019  
 Licensed under the TAPR Open Hardware License ([www.tapr.org/OHL](http://www.tapr.org/OHL)). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.  
**Open Hardware DSP Platform – [www.ohdsp.org](http://www.ohdsp.org)**

Sheet: /SPDIF/  
 File: SPDIF.sch

**Title: CoreOne – xCORE200 Platform**

Size: A4 Date: 2019-04-02

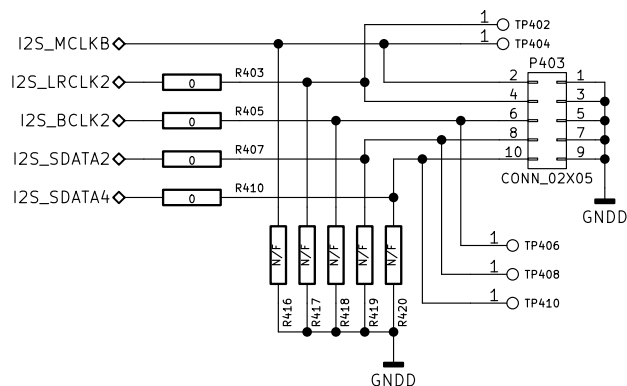
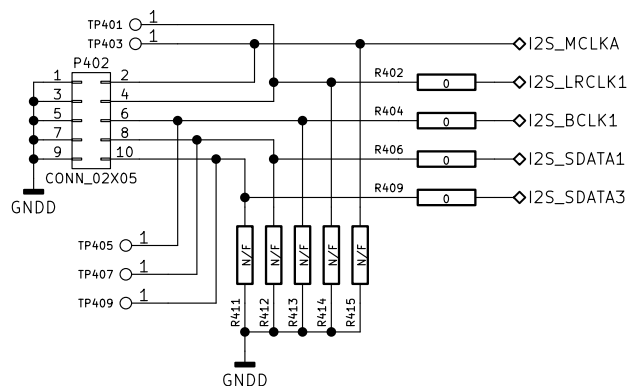
KiCad E.D.A. kicad (5.1.0)-1

**Rev: 2.0**

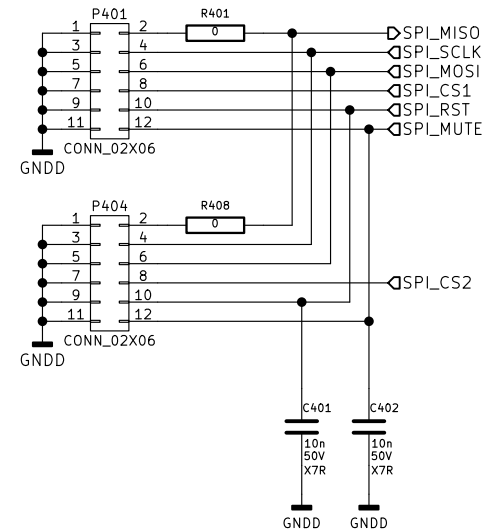
Id: 3/8

# Connectors

## I2S Connectors

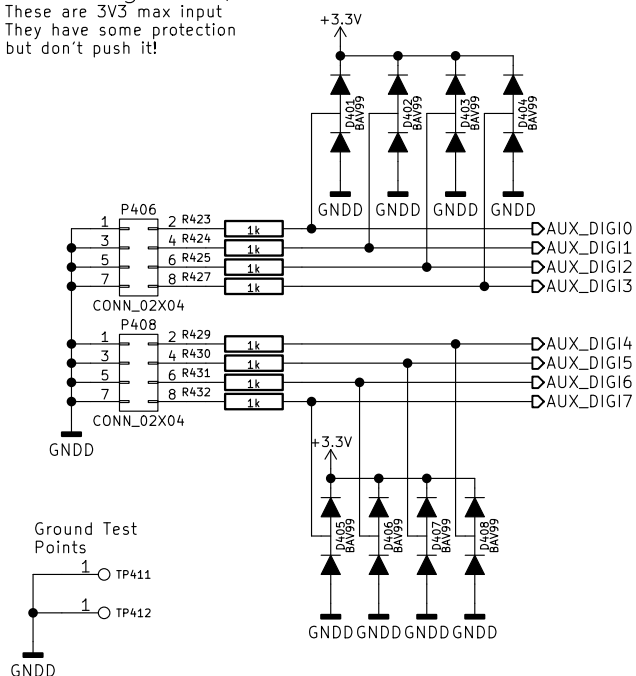


## SPI Ports

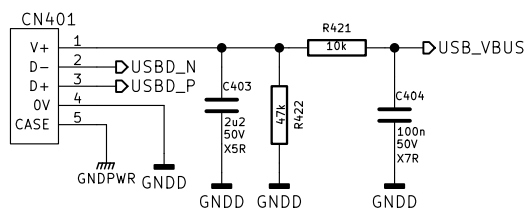


## AUX Digital I/O

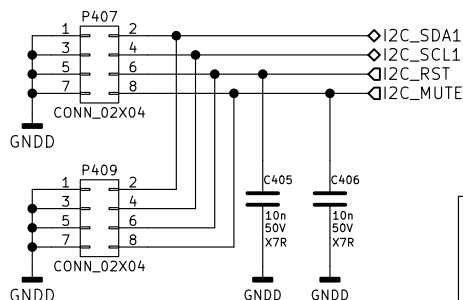
These are 3V3 max input  
They have some protection  
but don't push it!



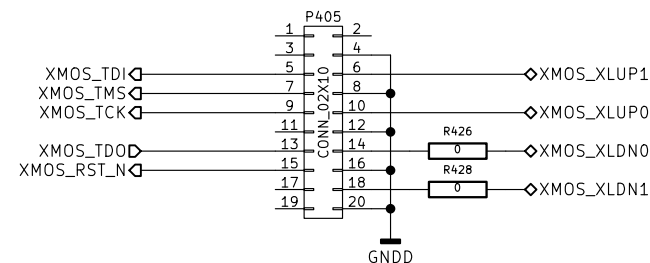
## USB Port



## I2C Ports



## XMOS xSYS Interface Programming/Debug



Copyright Paul Janicki 2019  
Licensed under the TAPR Open Hardware License ([www.tapr.org/OHL](http://www.tapr.org/OHL)). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.

Open Hardware DSP Platform – [www.ohdsp.org](http://www.ohdsp.org)

Sheet: /Connectors/

File: Connectors.sch

**Title: CoreOne – xCORE200 Platform**

Size: A4 Date: 2019-04-02

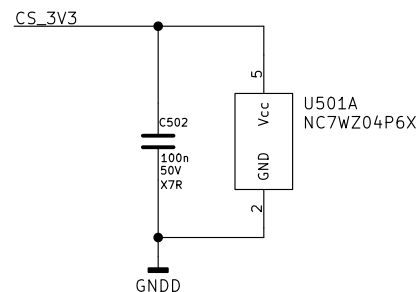
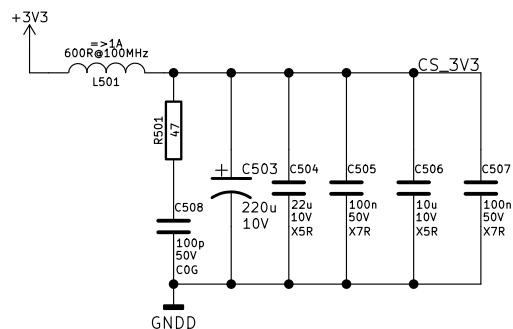
KiCad E.D.A. kicad (5.1.0)–1

Rev: 2.0

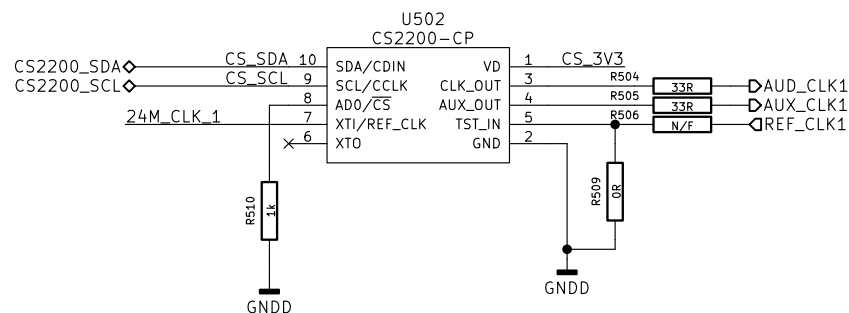
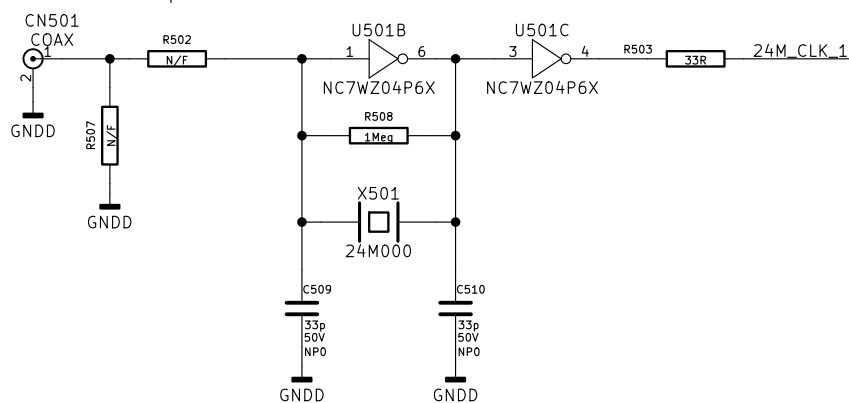
Id: 4/8

## System and Audio Clocks

Note: Two controlled clocks are provided to allow two audio clock domains. Both clocks are fed from the same crystal. If U502 and/or U503 are fitted as CS2100-CP parts then the clocks can be run from the REF\_CLK signals to synchronise the clocks to the AUD\_PLLSYNC signal from U801.



External Clock Input



Copyright Paul Janicki 2019

Licensed under the TAPR Open Hardware License ([www.tapr.org/OHL](http://www.tapr.org/OHL)). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.

Open Hardware DSP Platform – [www.ohdsp.org](http://www.ohdsp.org)

Sheet: /Clock-CS2200/

File: Clock-CS2200.sch

**Title: CoreOne – xCORE200 Platform**

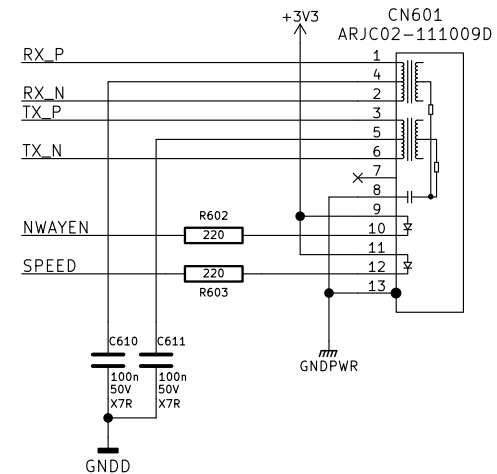
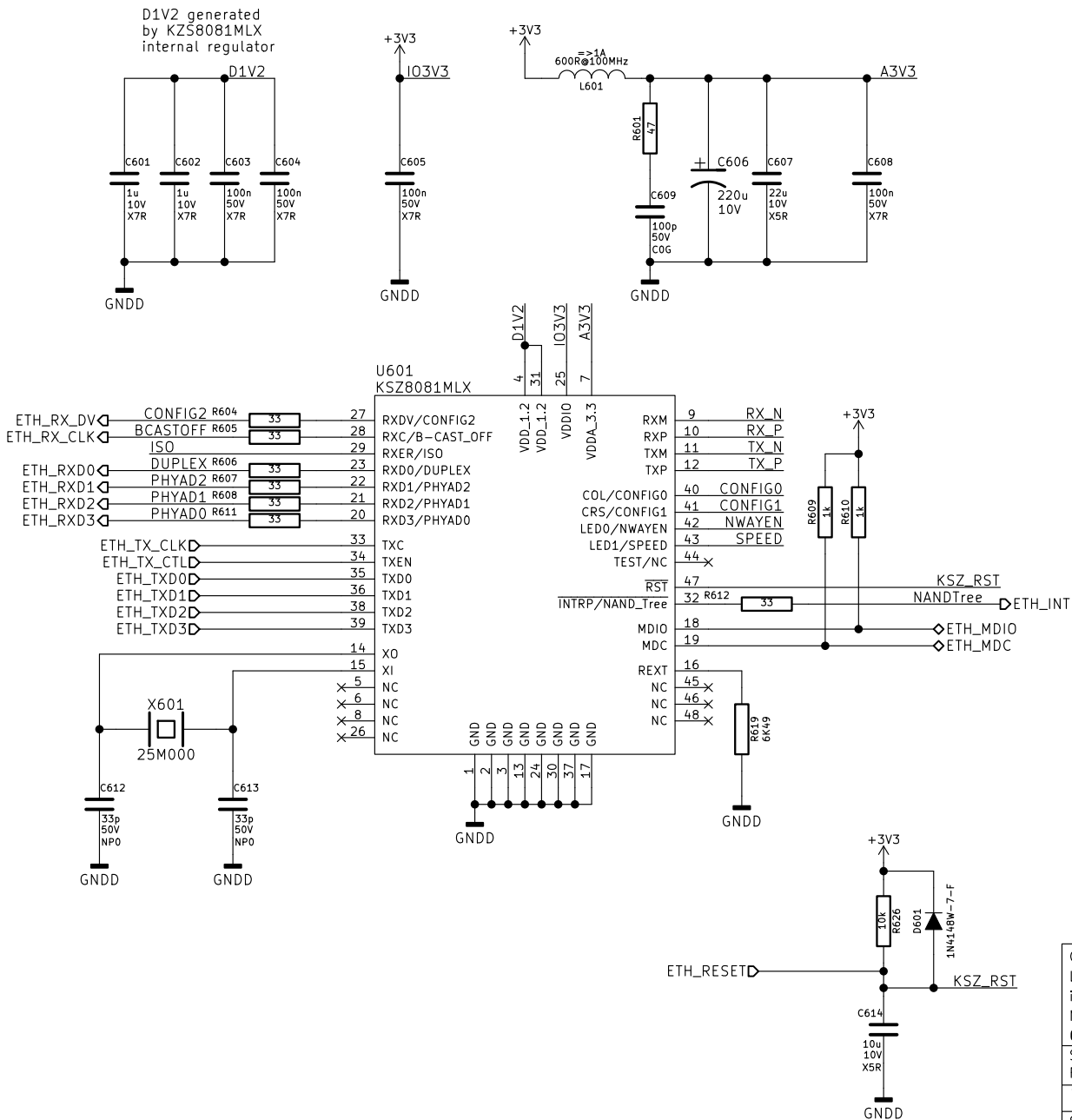
Size: A4 Date: 2019-04-02

KiCad E.D.A. kicad (5.1.0)-1

Rev: 2.0

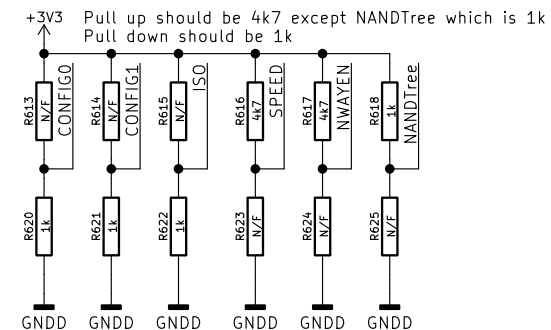
Id: 5/8

Ethernet – KSZ8081 10/100Meg Base-TX



Strapping Resistors – see datasheet

Note: Some strapping options will be control through the XMOS (U801) interface.  
Strapping resistors control lines not connected to U801.



Copyright Paul Janicki 2019

Licensed under the TAPR Open Hardware License ([www.tapr.org/OHL](http://www.tapr.org/OHL)). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.

Open Hardware DSP Platform – [www.ohdsp.org](http://www.ohdsp.org)

Sheet: /Eth-KSZ8081/

File: Eth-KSZ8081.sch

**Title: CoreOne – xCORE200 Platform**

Size: A4	Date: 2019-04-02
----------	------------------

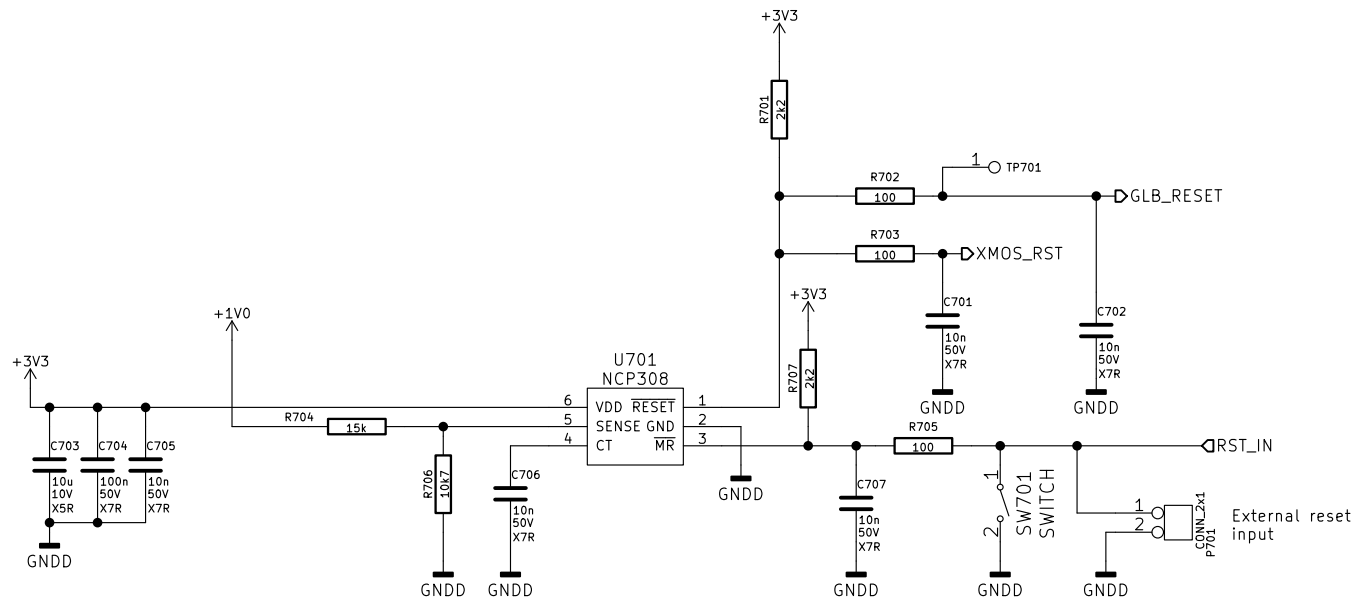
SIZE: A1	Date: 2013
KiCad E.D.A.	kicad (5.1.0)-1

Rev: 2.0

Id: 6/8

## Voltage Monitor Reset

Generate a global reset based on 1V0 voltage rail.  
Use NCP308SNADJT1G adjustable version.  
Supports external reset signal.



Copyright Paul Janicki 2019

Licensed under the TAPR Open Hardware License ([www.tapr.org/OHL](http://www.tapr.org/OHL)). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.

**Open Hardware DSP Platform – [www.ohdsp.org](http://www.ohdsp.org)**

Sheet: /Reset-NCP308/

File: Reset-NCP308.sch

**Title: CoreOne – xCORE200 Platform**

Size: A4 Date: 2019-04-02

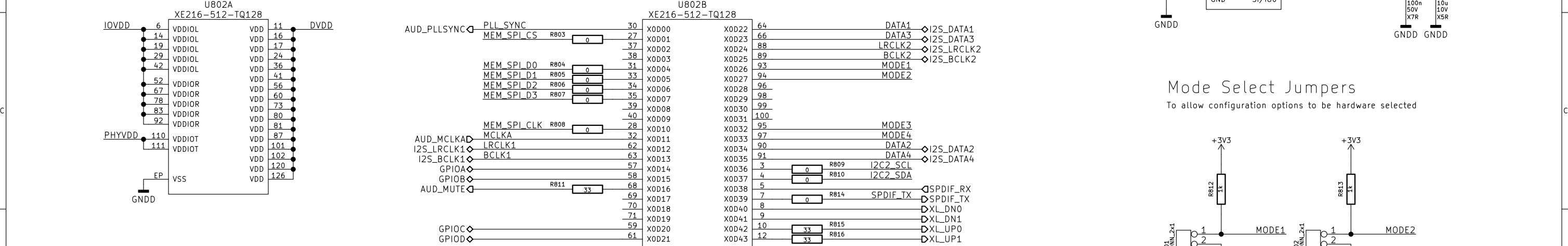
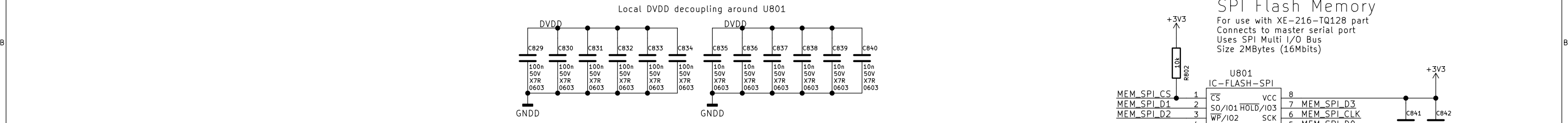
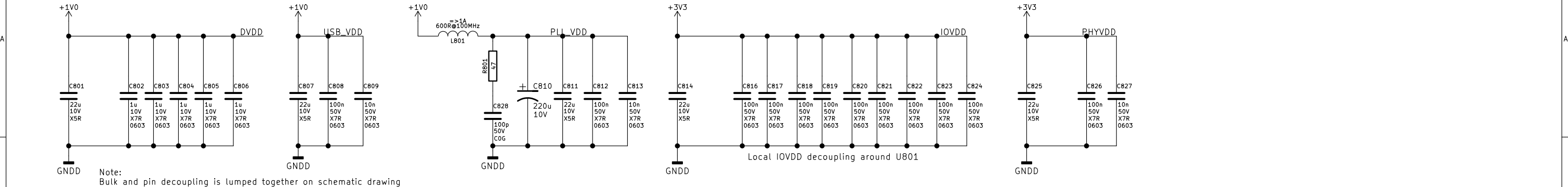
KiCad E.D.A. kicad (5.1.0)-1

**Rev: 2.0**

Id: 7/8

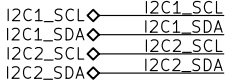
XMOS 200 – XE216-512-TQ128 or XEF216-512-TQ128

Note: Can use XE216-512-TQ128 or XEF216-512-TQ128. XEF216-512-TQ128 has internal flash memory so do not fit SPI flash memory U802.

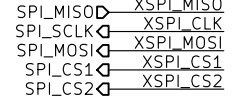


Control ports

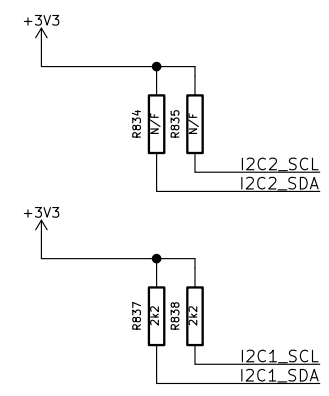
I2C



SPI

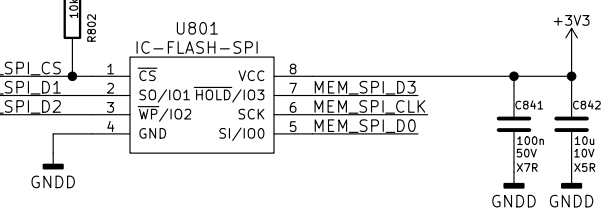


I2C Pull-ups



SPI Flash Memory

For use with XE-216-TQ128 part  
Connects to master serial port  
Uses SPI Multi I/O Bus  
Size 2MBytes (16Mbits)



Mode Select Jumpers

To allow configuration options to be hardware selected

