FT64 Paged Memory Management Unit

# Features

* 512 entry, 8-way associative TLB
* variable page table depth, subset address translation
* address short-cutting for larger page sizes (8MB)
* 8kB page size
* 64-bit address translations
* 64-bit bus mastering for table lookup
* automatic periodic hardware clearing of page accessed bit

# Operation

The PMMU translates virtual to physical addresses by looking up the translation in a TLB (translation lookaside buffer). Address translation takes two clock cycles to perform. During the first clock cycle it is determined if the access is valid. If the access is a valid access then the input address is transferred to output on the second clock cycle, otherwise an error signal is set active.

The PMMU will automatically walk the page tables on a TLB miss and update the TLB with an address translation. If the translation is not available a page fault is generated. Walking the page tables depends on the number of levels selected by the PTA (page table address) register. More levels to traverse take more memory cycles. Address translation may be shortcut at 8MB pages if indicated in the page table entry.

The PMMU will also periodically reset the accessed bits of page table entries during idle access times, to support the clock algorithm. The update is triggered by an externally provided signal. This signal should be connected to an interval timer (PIT) circuit.

Pages are 8kB in size. Each page contains 1024, 64-bit entries.

# Page Table Entry

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 16 | | 15 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Physical Address28..13 | | PL | D | U | S | A | C | R | W | X |
| 63 51 | 50 32 | | | | | | | | | |
| ~13 | Physical Address47..29 | | | | | | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit |  |  | |  |
| 0 | X | 1 = executable | Together these three fields combined indicate if the page is present. It must be at least one of readable, writeable, or executable. | |
| 1 | W | 1 = page writeable |
| 2 | R | 1 = readable |
| 3 | C | 1 = cache disabled | |  |
| 4 | A | 1 = accessed | |  |
| 5 | S | 1 = shortcut translation | | Translation shortcut bit eg (8MiB pages) |
| 6 | U | undefined usage | | available to be used by OS |
| 7 | D | 1=dirty | |  |
| 8 to 15 | PL | Privilege level | |  |
| 16 to 31 | PA | Physical Address bits Physical Address bits 13 to 47 | |  |
| 32 to 50 |  |

# Page Directory Entry

Page directory entries have the same format as page table entries.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 16 | | 15 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Physical Address28..13 | | PL | D | U | S | A | C | R | W | X |
| 63 51 | 50 32 | | | | | | | | | |
| ~13 | Physical Address47..29 | | | | | | | | | |

# Hardware Interface

|  |  |  |  |
| --- | --- | --- | --- |
| Port | Bits | Dir. | Description |
| rst\_i | 1 | I | resets the core |
| clk\_i | 1 | I | clock input |
| clock\_tick\_i | 1 | I | This input is meant to be driven by a timing source and is used for hardware clearing of the accessed bit in page table entries. |
| m\_cyc\_o | 1 | O | bus master cycle valid strobe |
| m\_lock\_o | 1 | O | not used |
| m\_ack\_i | 1 | I | bus master transfer acknowledge |
| m\_we\_o | 1 | O | bus master write transaction enable |
| m\_sel\_o | 8 | O | bus master byte lane select (always FFh) |
| m\_adr\_o | 48 | O | bus master address output |
| m\_dat\_i | 64 | I | bus master data input |
| m\_dat\_o | 64 | O | bus master data output |
| invalidate | 1 | I |  |
| invalidate\_all | 1 | I | invalidates all entries in the TLB |
| pta | 48 | I | physical address of page table in memory. The page table should be 8kB aligned. Low order bits select table depth. Each level covers 1024 times the lower level memory range.   |  |  |  |  | | --- | --- | --- | --- | | PTA bits [10:8] | Address Space |  |  | | 0 | 8MB | root page table only |  | | 1 | 8GB | two level table |  | | 2 | 8TB | three table levels |  | | 3 | 8XB | four table level |  | | 4 |  | five table levels |  | | 5 |  | six table levels |  | | 6 |  | reserved |  | | 7 |  | reserved |  | |
| page\_fault | 1 | O | activated when a page is not present |
| pl\_i | 8 | I | privilege level input |
| ol\_i | 2 | I | operator level input (machine level (0) bypasses address mapping) |
| icl\_i | 1 | I | indicates an instruction cache load is taking place |
| cyc\_i | 1 | I | indicates a bus cycle is active |
| we\_i | 1 | I | indicates a write cycle is taking place |
| sel\_i | 8 | I | byte lane selects |
| vadr\_i | 64 | I | virtual address to translate |
| cyc\_o | 1 | O | bus cycle taking place |
| we\_o | 1 | O | write cycle taking place – comes from we\_i but may be masked off if page is read-only |
| sel\_o | 8 | O | byte lane selects from sel\_i |
| padr\_o | 48 | O | physical address output |
| cac\_o | 1 | O | page is not cachable |
| prv\_o | 1 | O | privilege violation |
| exv\_o | 1 | O | execute violation |
| rdv\_o | 1 | O | read violation |
| wrv\_o | 1 | O | write violation |