# Noc1

## Overview

The Noc1 network is a simple ring configuration. The output from one node is connected to input of the next. The output of the last node is connected back to the first in order to form a ring. All the network nodes are identical except for the one which interfaces to the rest of the system. Each node consists of two RiSC-V R32Im compatible cores which share RAM and ROM. There is a single network interface for each node which only cpu #1 of the node has access to.

## Network

### Hardware

The network is implemented as a parallel bus 96 bits in width. The goal was to keep things simple and avoid using serial transceivers. The bus is also very high-speed given it’s parallel nature. The bus and the cores are all clocked by a common clock signal. The bus operates in a synchronous fashion.

### Protocol

The network protocol is very simple. Network packets are fixed length for simplicity. There is enough room in the packet to transmit two thirty-two bit words of information plus packet control bits. The packet size is three thirty-two bit words or 96 bits.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 95 92 | 91 88 | 87 | 86 81 | 80 0 |
| RID | TID | ACK | AGE | Payload Area |

The packet contains the following fields:

RID – id of intended receiver

TID – id of transmitter

ACK – acknowledge receipt of packet

AGE – age of the packet in ring cycles

* the packet gets to being too old it is automatically deleted.

ID #0 means the packet is empty (no receiver)

ID #1 is the system controller – it takes care of interfacing to the outside world I/O and aging the packets as they travel around the ring.

ID #2 to #13 are used by nodes

ID #15 indicates the target is a global broadcast, all nodes should pay attention.

### System Access Packet

The following packet is used by the nodes to send system read/write requests.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 95 92 | 91 88 | 87 | 86 81 | 80 69 | 68 | 67 64 | 63 32 | 31 0 |
| 1 | TID | ACK | AGE | 0 | We | Sel4 | Addr32 | Data32 |

## Network Controller

### Overview

The network controller core takes care of interfacing to the network. It accepts a 96 bit input bus and outputs a 96 bit output. Input passes to output on every clock cycle if the controller isn’t transmitting. When the cpu requests to transmit a packet, the controller will wait for an opening in the stream of packets passing through it before transmitting. The opening is an empty packet signalled by the RID and TID fields equal to zero.

If the network controller receives a packet destined for one of the cpu cores, it is buffered in a 63 entry fifo buffer. CPU #1 of a node must poll the receive buffer state to determine when there is data available.

### Bus Interface

The controller acts as a WISHBONE slave device coupled to cpu #1 in a node.

### Register Set

The controller is mapped into the address space of cpu #1 at $FFD80xx

|  |  |  |  |
| --- | --- | --- | --- |
| Regno | Read | Write |  |
| 0x00 | packet data [31:0] | packet data [31:0] | On a read this register reflects the oldest incoming packet data from the fifo. On a write the packet output buffer is updated. |
| 0x04 | packet data [63:32] | packet data [63:32] |
| 0x08 | packet data [95:64] | packet data [95:64] |
| 0x0C | reserved |  | These registers are reserved, possibly for a larger packet size. |
| 0x10 | reserved |  |
| 0x14 | reserved |  |
| 0x18 | advance fifo ptr | tx pulse | reading this register advances the fifo pointer, writing this register causes the packet data to be transmitted. |
| 0x1C | status reg  Bits 5-0 read count  bit 8 indicates transmit status | status reg | This register is a read-only status register. The low order five bits indicate how many packets are in the read fifo.  Bit 8 indicates the transmit status, 0 = ready for new transmit data, 1 = packet not transmitted yet (busy). |

The controller automatically inserts the transmitter id into the packet.

The controller automatically clears the ack bit of the packet when transmitting.