|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 95 | 94 91 | 90 87 | 86 | 85 78 | 77 0 | | | | |
| GB | RID | TID | ACK | AGE | Payload Area | | | | |
|  |  |  |  |  |  | 68 | 67 64 | 63 32 | 31 0 |
| GB | RID | TID | ACK | AGE |  | We | Sel4 | Addr32 | Data32 |
|  |  |  |  |  |  | |  |  |  |

GB – global broadcast

* this bit is set all receivers should pay attention to the packet.

RID – id of intended receiver

TID – id of transmitter

ACK – acknowledge receipt of packet

AGE – age of the packet in ring cycles

* the packet gets to being too old it is automatically deleted.

ID #0 means the packet is empty (no receiver)

ID #1 to #4 are used by nodes

ID #15 is the system controller – it takes care of interfacing to the outside world I/O and aging the packets as they travel around the ring.

|  |  |  |  |
| --- | --- | --- | --- |
| Regno | Read | Write |  |
| 0x00 | packet data [31:0] | packet data [31:0] | On a read this register reflects the oldest incoming packet data from the fifo. On a write the packet output buffer is updated. |
| 0x04 | packet data [63:32] | packet data [63:32] |
| 0x08 | packet data [95:64] | packet data [95:64] |
| 0x0C | reserved |  | These registers are reserved, possibly for a larger packet size. |
| 0x10 | reserved |  |
| 0x14 | reserved |  |
| 0x18 | advance fifo ptr | tx pulse | reading this register advances the fifo pointer, writing this register causes the packet data to be transmitted. |
| 0x1C | status reg  Bits 5-0 read count  bit 8 indicates transmit status | status reg | This register is a read-only status register. The low order five bits indicate how many packets are in the read fifo.  Bit 8 indicates the transmit status, 0 = ready for new transmit data, 1 = packet not transmitted yet. |

The controller automatically inserts the transmitter id into the packet.