# Overview

The primary extension to the RISCV ISA is the addition of 64 bit instruction support for larger constants. Branch instructions have been extended to include compare to 20 bit immediate.

# Base Instruction Formats

These are the basic RISCV instruction formats (for reference).

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 25 | | 24 20 | | 19 15 | 14 12 | 11 7 | | 6 0 |  |
| funct7 | | rs25 | | rs15 | funct3 | rd5 | | Opcode7 | R-Type |
| Imm11..0 | | | | rs15 | funct3 | rd5 | | Opcode7 | I-Type |
| Imm11..5 | | rs25 | | rs15 | funct3 | Imm4..1 | I0 | Opcode7 | S-Type |
| I12 | Imm10..5 | rs25 | | rs15 | funct3 | Imm4..1 | I11 | Opcode7 | SB-Type |
| Imm31..12 | | | | | | rd5 | | Opcode7 | U-Type |
| I20 | Imm10..5 | Imm4..1 | I11 | Imm19..15 | Imm14..12 | rd5 | | Opcode7 | UJ-Type |

These are the new instruction formats:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| w0 | Imm11..0 | | | | rs15 | funct3 | rd5 | | 3Fh7 | I64-Type |
| w1 | Imm31..12 | | | | | | ~5 | | Opcode7 |  |
| w0 | Imm11..5 | | rs25 | | rs15 | funct3 | Imm4..1 | I0 | 3Fh7 | S64-Type |
| w1 | Imm31..12 | | | | | | ~5 | | Opcode7 |  |
| w0 | I12 | Imm10..5 | | rs25 | rs15 | funct3 | Imm4..1 | I11 | 3Fh7 | SB64-Type |
| w1 | Imm19..0 | | | | | | ~5 | | Opcode7 |  |

The opcode field is moved to bits 32 to 38 but the opcodes remain the same. Note that there are redundant opcodes which may be used for other purposes. In particular the shift operations never require extended immediate constants.

# Greenfield Extensions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| VA31..29 |  | Reset Value | CSR | Read /Write |  |
|  | EXR |  | 79Dh |  | exception routing |
|  | SLL | 0 | 79Eh |  | stack lower limit |
|  | SLU | FFFFFFFFh | 79Fh |  | stack upper limit |

The stack lower and upper limit registers are checked against the stack pointer (x14) and frame pointer (x2) registers when a data access (load or store) occurs in the data segment.

## Immediate Constants

A larger immediate constant is directly supported through the use of 64 bit instructions.

# Brownfield Modifications

## MCAUSE Register

When a hardware interrupt occurs the most significant bit of the mcause register is set, the exception code is set to 15 ( a previously reserved value) and bits 4 through 12 of the register are set to a vector number supplied by the interrupt hardware.

|  |  |  |  |
| --- | --- | --- | --- |
| 31 | 30 13 | 12 4 | 3 0 |
| Interrupt | Unused | Vector Number | Exception Code |
| 11 | 018 | Vector9 | Fh4 |

## MEPC Register

This register must be 256 byte page aligned.

## Instructions