Packet Types

|  |  |
| --- | --- |
| Header (4 bits) | Payload (32 bits) |
| 0 | select / deselect / NOP token |
| 1 | Address bits 0 to 31 |
| 2 | address bits 32 to 63 |
| 3 | control wr + byte lane selects 0 to 15 |
| 4 | data bits 0 to 31 |
| 5 | data bits 32 to 63 |
| 6 | data bits 64 to 95 |
| 7 | data bits 96 to 127 |
| 8 to 15 | reserved |

No master or slave shall use be numbered zero.

Slaves:

Slave transmitters are disabled until they receive a select request from a master. Upon receiving a deselect request the slave transmitters will be disabled.

The master may request a synchronization cycle for which the slave begins sending a device enable + sync pulse.

If the master does not cancel the sync request within 65,536 clock cycles then the master is considered invalid and the slave will no longer respond to it.

If the slave is in the IDLE state it will send a NOP to the master.

Masters:

The master will send sync + device enable + sync request to the slave at start-up before transferring any data to allow the slave receiver to synchronize to the master. If the slave does not respond within 65,536 cycles the slave is considered invalid.

The master will send a slave select token to select the slave before transferring data. When the transfer is complete the master will a deselect token to the slave.

Only data packets that need to be transmitted are. If the byte lane select indicates that a data packet is not required then it is not transmitted.

Idle NOP:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 35 32 | 31 30 | 29 24 | 23 8 | 7 | 6 | 5 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Sync Request:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 35 32 | 31 30 | 29 24 | 23 8 | 7 | 6 | 5 0 |
| 0 | 0 | master number | 0 | 1 | 0 | slave number |

Device Select:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 35 32 | 31 30 | 29 24 | 23 8 | 7 | 6 | 5 0 |
| 0 | 0 | master number | 0 | 0 | 0 | slave number |

Device Deselect:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 35 32 | 31 30 | 29 24 | 23 8 | 7 | 6 | 5 0 |
| 0 | 0 | master number | 0 | 0 | 0 | 0 |

Address:

|  |  |
| --- | --- |
| 35 32 | 31 0 |
| 1 | Address bits 0 to 31 |

Read:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 35 32 | 31 30 | 29 24 | 23 16 | 15 0 |
| 3 | 0 | master number | 0 | byte lane selects |

Write:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 35 32 | 31 30 | 29 24 | 23 16 | 15 0 |
| 3 | 2 | master number | 0 | byte lane selects |

Write Trigger Cycle:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 35 32 | 31 30 | 29 24 | 23 16 | 15 0 |
| 3 | 3 | master number | 0 | byte lane selects |

Slave Tran Ack:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 35 32 | 31 30 | 29 24 | 23 6 | 5 0 |
| 3 | 1 | slave number | 0 | master number |

Data:

|  |  |
| --- | --- |
| 35 32 | 31 0 |
| 4 | Data bits 0 to 31 |
| 5 | Data bits 32 to 63 |
| 6 | Data bits 64 to 95 |
| 7 | Data bits 96 to 127 |