rtfUart

# Overview

A UART component (Universal Asynchronous Transmitter / Receiver) is used for the asynchronous transmission and reception of data. Asynchronous referring to the lack of a clock signal during transmission or reception.

rtfUart is a WDC6551 register compatible uart. The uart is a 32-bit peripheral device. It may be used as an eight-bit peripheral by connecting the high order 24-bit data input lines to ground, and grounding select lines one to three.

Baud rate is controlled by a harmonic frequency synthesizer assuming a 100MHz clock input. If a different clock frequency is used, then the multiplier table will need to be updated. The baud rate may also be controlled via a clock multiplier directly with a clock multiplier register. This register is 32 bits so gives a frequency resolution of 0.0233 Hz assuming a 100MHz clock.

While many uarts support five to eight bit transfers (nine if the parity bit is used) to support legacy applications, this uart is capable of transferring up to 32 bits.

## Special Features

* WDC6551 register compatibility
* harmonic frequency synthesis for baud rate generation
* ability to transmit or receive up to 32 bits
* transfer rates up to 3.7M Baud

# Register Description

There are only four registers in the design. The function of the low order eight bits of the registers matches the 6551 function. The controller honors byte lane selects so only the portion of the register selected is written.

|  |  |  |
| --- | --- | --- |
| Reg | Moniker | Description |
| 0 | UART\_TRB | Transmit and receive buffer. Data written is transmitted, on a read data available is read. Also reads / writes the clock multiplier if access to clock multiplier is enabled. |
| 1 | UART\_STAT | Status Register. Returns status bits on a read, a write of any value will cause a reset of some of the command register bits |
| 2 | UART\_CMD | Command register |
| 3 | UART\_CTRL | Control register |

## UART\_TRB

This register is 32-bits wide allowing data of up to 32 bits width to be transmitted or received by the uart. Data written to the register is transmitted. A register read returns data received by the uart. When the fifo’s are enabled writing to this register writes to the transmit fifo. Reading this register reads the receive fifo. If clock multiplier access is enabled (via control register bit 31) then this register allows modifying or reading the clock multiplier value.

## UART\_STAT

Uart status register.

|  |  |  |
| --- | --- | --- |
| Bit | Status |  |
| 0 | Parity Error | 1 = parity error occurred, 0 = no error |
| 1 | Framing Error | 1 = framing error |
| 2 | Overrun | 1 = overrun |
| 3 | Rx Full | 1 = receiver data available |
| 4 | Tx Empty | 1 = open slot in transmit fifo |
| 5 | DCD | 0 = data carrier present |
| 6 | DSR | 0 = data set ready |
| 7 | IRQ | 1 = irq occurred |
|  | **Additional Line Status Byte** | |
| 8 | reserved |  |
| 9 | reserved |  |
| 10 | reserved |  |
| 11 | reserved |  |
| 12 | Break received | 1 if a break signal is received |
| 13 | Tx Full | 0 = transmit fifo full |
| 14 | reserved |  |
| 15 | G Rcv Err | 1 = global receiver error (set if any error status is set) |
|  | **Additional Modem Status Byte** | |
| 16 | CTS | 1 = CTS line changed state |
| 17 | DSR | 1 = DSR line changed state |
| 18 | RI | 1 = RI line changed state |
| 19 | DCD | 1 = DCD line changed state |
| 20 | CTS | CTS state |
| 21 | reserved |  |
| 22 | RI | RI state |
| 23 | reserved |  |
|  | **IRQ Status** | |
| 24,25 | zero | these two bits are zero |
| 26 to 28 | IRQENC | encoded irq value (0 to 7) |
| 29 to 30 | reserved |  |
| 31 | irq | IRQ is set |

## UART\_CMD

|  |  |  |
| --- | --- | --- |
| Bit |  |  |
| 0 | DTR | output 1 = low, 0 = high |
| 1 | RxIe | receiver interrupt enable 0 = enabled, 1 = disabled |
| 2,3 | RTS Control |  |
|  | 00 | output RTS high |
|  | 01 | output RTS low, enable transmit interrupt |
|  | 10 | output RTS low, |
|  | 11 | output RTS low, send a break signal |
| 4 | LLB | 1 = local loopback (receiver echo) |
| 5 to 7 | Parity Control |  |
|  | 000 | no parity |
|  | 001 | odd parity |
|  | 011 | even parity |
|  | 101 | transmit mark parity (parity error disabled) |
|  | 111 | transmit space parity (parity error disabled) |
| 8 | LSIe | line status change interrupt enable 1 = enabled |
| 9 | MSIe | modem status change interrupt enable 1 = enabled |
| 10 | RxToIe | receiver timeout interrupt enable 1 = enabled |
| 11 to 31 | reserved |  |

## UART\_CTRL

|  |  |  |
| --- | --- | --- |
| Bit |  |  |
| 0 to 3 | Baud Rate |  |
|  | |  |  | | --- | --- | | 0000 | Use 16x external clock | | 0001 | 50 | | 0010 | 75 | | 0011 | 109.92 | | 0100 | 134.58 | | 0101 | 150 | | 0110 | 300 | | 0111 | 600 | | 1000 | 1200 | | 1001 | 1800 | | 1010 | 2400 | | 1011 | 3600 | | 1100 | 4800 | | 1101 | 7200 | | 1110 | 9600 | | 1111 | 19200 | | This table is expanded using an extra control bit #27. |
| 4 | Rx clock source | 1 = external, 0 = baud rate generator |
| 5,6 | Word length   |  |  | | --- | --- | | 00 | 8 | | 01 | 7 | | 10 | 6 | | 11 | 5 | | code for word length in bits (legacy) |
| 7 | Stop Bit   |  |  | | --- | --- | | 0 | 1 | | 1 | 1 if 8 bits and parity | | 1 | 1.5 if 5 bits and no parity | | 1 | 2 otherwise | |  |
| 8 to 13 | Word length | number of bits in word to transmit or receive, this may be set from 0 to 32. |
| 14,15 | reserved |  |
| 16 | Fifo enable | 1 = fifo’s enabled |
| 17 | Rx Fifo Clear | 1 = clear receiver fifo |
| 18 | Tx Fifo Clear | 1 = clear transmit fifo |
| 19 | reserved |  |
| 20,21 | Transmit Threshold   |  |  | | --- | --- | | 0 | 1 byte | | 1 | ¼ full | | 2 | ½ full | | 3 | ¾ full | | Threshold for DMA signal activation  If the transit fifo count is less than the threshold then a DMA transfer is triggered. |
| 22, 23 | Receive Threshold   |  |  | | --- | --- | | 0 | 1 byte | | 1 | ¼ full | | 2 | ½ full | | 3 | ¾ full | | Threshold for DMA signal activation. If the receive fifo count is greater than the threshold then a DMA transfer is triggered. |
| 24 | hwfc | 1 = automatic hardware flow control |
| 25 | xClkSrc | 1=external clock source (xclk pin) |
| 26 | dmaEnable | 1 = dma enabled |
| 27 | Baud Rate bit 4   |  |  | | --- | --- | | 10000 | 38400 | | 10001 | 57600 | | 10010 | 115200 | | 10011 | 230600 | | 10100 | 460800 | | 10101 | 921600 | | 10110 | 1843200 | | 10111 | 3686400 | | 11xxx | reserved | | Extended baud rate selection bit, used in combination with bits 0 to 3. |
| 28,29 | reserved |  |
| 30 | selCM | 1 = use clock multiplier register, 0 = use baud table |
| 31 | accessCM | 1 = access clock multiplier via TRB register, 0 = normal TRB operation |