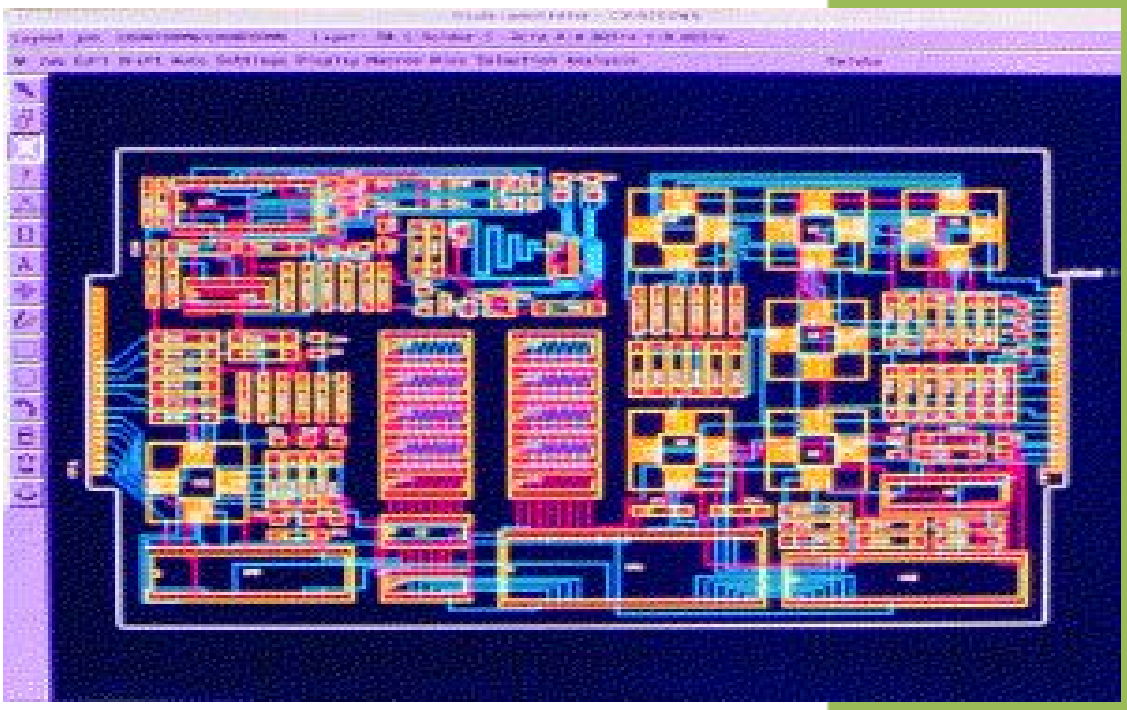
Computer Engineering Department
Faculty of Engineering
Cairo University

Spring 2018
CMP 305
VLSI

DCNN Accelerator

2018



VLSI Semester Term Project
Phase Two

VLSI Project
Computer Engineering Department

Objectives

- To understand Digital Design Flow better
- To be proficient at VHDL
- To create real world hardware applications
- To understand the mapping between Algorithm Specifications & Hardware Implementation
- To understand Design Trade-offs
- To learn how to optimize Hardware Designs

Introduction

In this phase, You will walk through the ASIC Design flow to generate final working GDSII file for your DCNN Accelerator design delivered in phase 1. RTL implementation and validation are the 1st and 2nd steps in ASIC design flow as shown in Figure 1. You will use Mentor tools as you practiced in the labs to complete the ASIC Design flow.

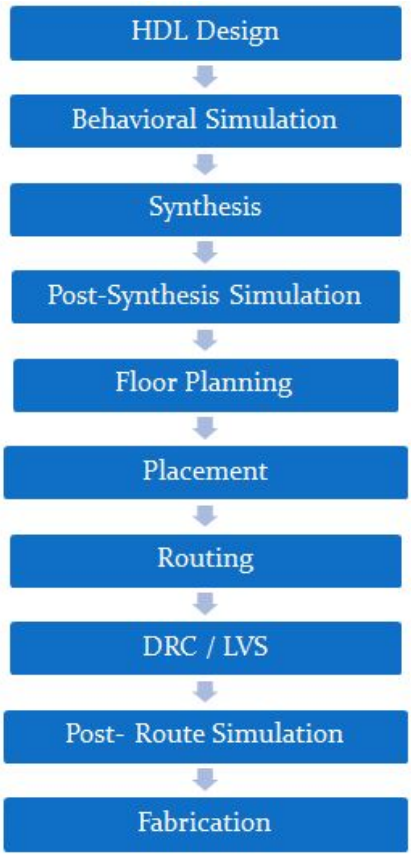


Figure 1: ASIC Design Flow

Phase 2 Requirements

- Check that your top level design has the pins mentioned in "Detailed Interfacing" section.
- Implement your Design using VHDL.
- Simulate your Design using Do File.
- Synthesize your Design using Mentor LeonardoSpectrum on ***TSMC035*** Technology.
- Verify the synthesized netlist generated using your Do File.
- Place & Route your netlist using Mentor Pyxis.
- Generate GDSII file & verify your design for DRC & LVS.

Detailed Interfacing

Your design must have the following interfacing pins:

Port	Direction	Size
Clk	IN	1 bit
Rst	IN	1 bit
Start	IN	1 bit
Inst	IN	1 bit
Size	IN	1 bit
Stride	IN	1 bit
Done	OUT	1 bit
RAM_En	OUT	1 bit
RAM_RW	OUT	1 bit
RAM_Address	OUT	Your choice
RAM_DataIn	IN	40 bits
RAM_DataOut	Out	8 bits

Rules & Regulations

- Don't forget to take backups every mile stone.
- You are free to modify your design as long as you perform correct functionality.
- Your design should be modifiable to ease the optimization in Placement and Routing.
- Take care that your design is logically mappable to hardware or you will have to repeat it all again.
- Open your mind and don't limit yourself.
- You are not allowed to copy from any external resources in your implementation .
- Use Tcl scripts, its reusable, faster, more efficient.
- You are allowed to consult external resources for Design but Do your OWN & you have to fully understand it.
- **Grades are based Mainly on Individual work + your team work . if you didn't work and the project was complete you will still get a zero grade. And we really mean it.**
- The Document is variable to change with a previous notification.

Tools

Languages: VHDL (RTL Implementation) & Verilog (Netlist)
Tools: Modelsim, LeonardoSpectrum, Pyxis & Calibre

Deliverables

- Modules' (Entity) VHDL codes.
- Verification DO Files + Memory Files.
- Synthesis Tcl Script
- Synthesis Design Constraint file
- Synthesis Netlist file
- Synthesis Reports (Timing / Area)
- Floor Planning & Placement reports
- Layout Verification Reports (DRC / LVS)
- Layout GDSII File
- Project Documentation:
    - Project File Tree
    - Each Module (Entity) Description
    - I/O Description
    - Timing Diagrams for Initialization / Processing / Results
    - Verification Results (Behavioral / Netlist)

- Design Flow Reports

Evaluation Criteria

- Unit Implementation (10 %)
- Integration (15%)
- Simulation & Verification Do File (20%)
- Synthesis (15%)
- Netlist Verification (10%)
- Placement, Routing, DRC, VLS (20%)
- Individual work (10%)
- Submit All deliverables in “Deliverables” section (-5%)
- Modularity & Design Neatness (-10%)

Deadline: Sunday 13/5/2018 at Eng. Ayman’s Mailbox

All teams should deliver their work on one CD/DVD, each team should put their deliverables in a folder with its team number “Team_##”

Discussion: will be scheduled later