The only differential pairs used in the OE acq. board are
in the headstage connector, and not even all of it.
All other differential pairs can be moved around or
routed as single lines if needed, but keeping as much diff pairs
as possible is more future proof

In summary:
-J1 (except even pins 32-47): KEEP I/IO and polarity.
-J1 pins 32-47: Do what's easiest. Keeping diff pairs is recommended
-J2: Do what's easiest, except S0[0-7]. Keeping diff pairs is recommended

"JP3" in acq. board.
Right connector, LVDS HS conn.

Possible locations
for S0[0-7]:
-pins 47-63
-pins 29-45
-pins 65-79

All other pins in this connector can really be shuffled around as needed

J1
BSE-040-01-X-D-A

J2
BSE-040-01-X-D-A

+5V
+3V3
+2V5
RAM_VDD
GND

Even pins 32-74 are not really used in the acq. board
(32-33 for daisy chain conn. 74 to gnd. Others to breakout section)
So they can be moved freely.

RAM
File: RAM.kicad_sch

Power
File: Power.kicad_sch

FPGA
File: FPGA.kicad_sch

FTDI
File: FTDI.kicad_sch

{RAMCTRL}
{RAMADDR}
{DQu}
{DQL}
{Bank6D}
{Bank8S}
{Bank0S}
{Bank1S}
{Bank2D}
{Bank3D}
{LED[0..3]}
INIT
DONE
{FT600}
FT_RSTReq
WAKEUP
{GPIO[1..0]}

Status LEDs
R8 4.7k
R9 4.7k
R10 4.7k
D1 LED_RED
D2 LED_GREEN
D3 LED_RED
DONE
INIT

User LEDs
R11 1K
R12 1K
R13 1K
R14 1K
D4 LED_GREEN LED3
D5 LED_GREEN LED2
D6 LED_GREEN LED1
D7 LED_GREEN LED0

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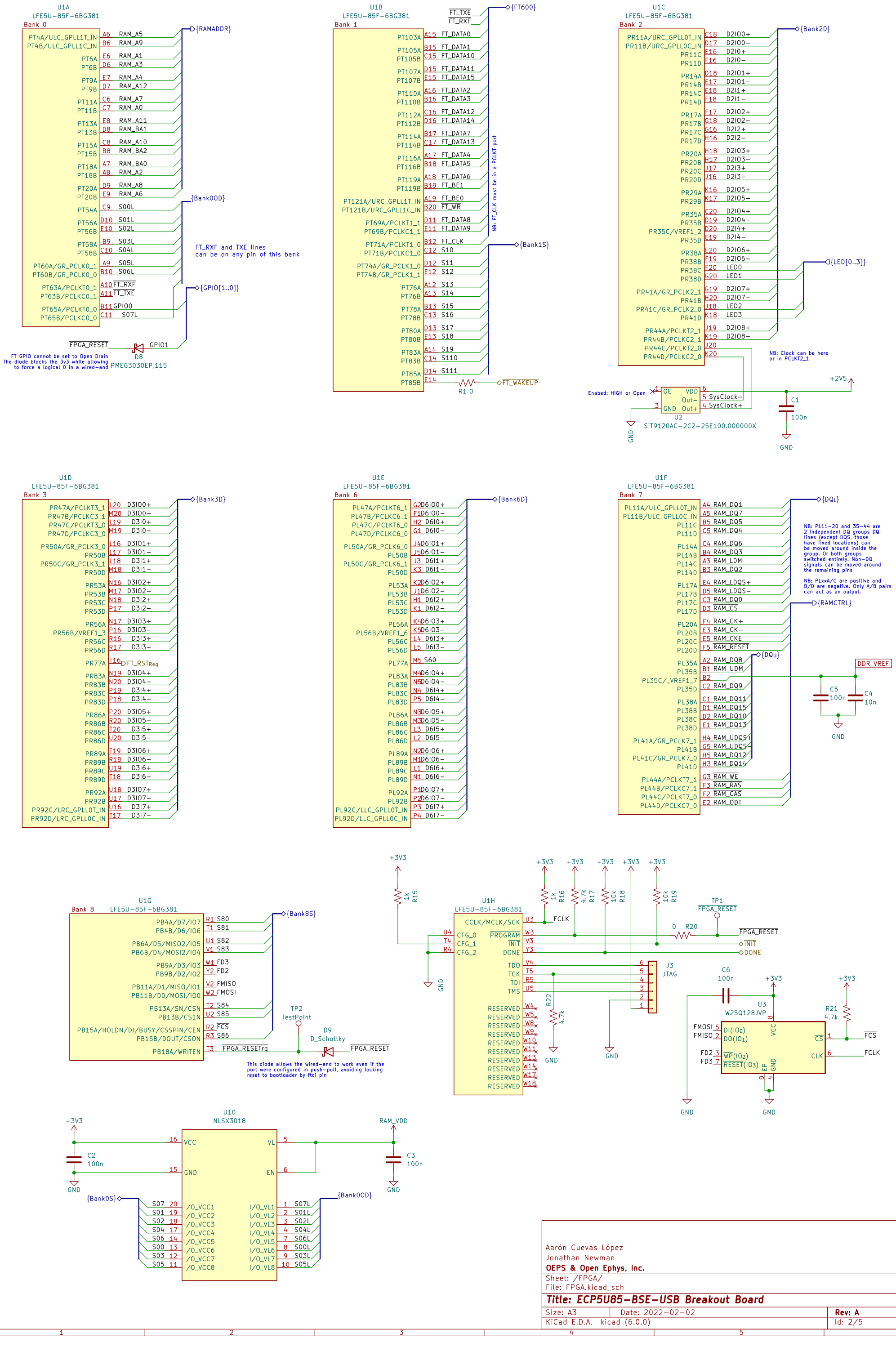
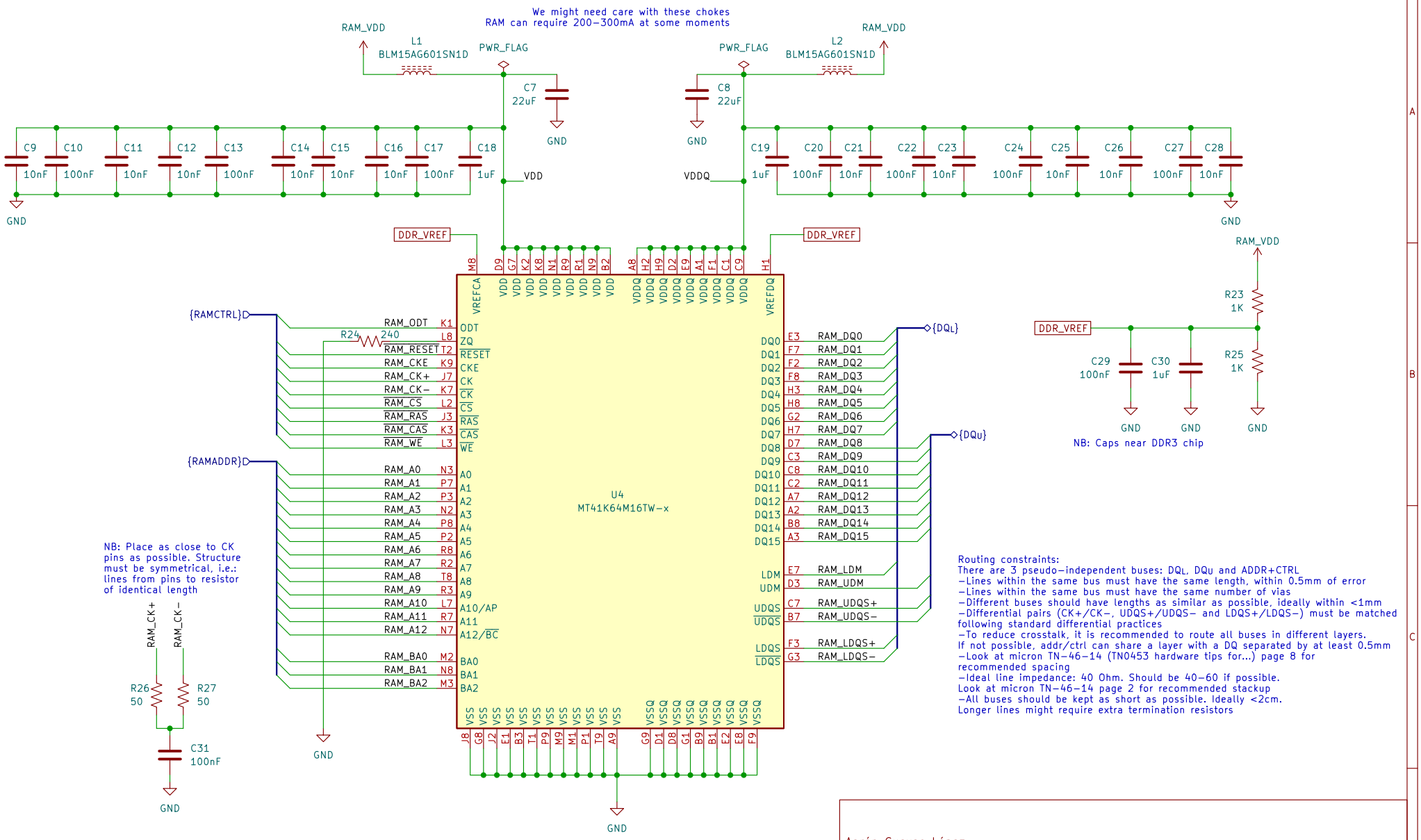
Jonathan Newman
OEPS & Open Ephys, Inc.

Sheet: /
File: ecp5u85-bse-usb.kicad_sch

Title: ECP5U85-BSE-USB Breakout Board

Size: A4	Date: 2022-02-02	**Rev: A**
KiCad E.D.A. kicad (6.0.0)		Id: 1/5


U1A
LFE5U-85F-6BG381
Bank 0
PT4A/ULC_GPLL1T_IN A6 RAM_A5
PT4B/ULC_GPLL1C_IN B6 RAM_A9
PT6A E6 RAM_A1
PT6B D6 RAM_A3
PT9A E7 RAM_A4
PT9B D7 RAM_A12
PT11A C6 RAM_A7
PT11B C7 RAM_A0
PT13A E8 RAM_A11
PT13B D8 RAM_BA1
PT15A C8 RAM_A10
PT15B B8 RAM_BA2
PT18A A7 RAM_BA0
PT18B A8 RAM_A2
PT20A D9 RAM_A8
PT20B E9 RAM_A6
PT54A C9 S00L
PT56A D10 S01L
PT56B E10 S02L
PT58A B9 S03L
PT58B C10 S04L
PT60A/GR_PCLK0_1 A9 S05L
PT60B/GR_PCLK0_0 B10 S06L
PT63A/PCLKT0_1 A10 FT_RXF
PT63B/PCLKC0_1 A11 FT_TXE
PT65A/PCLKT0_0 B11 GPIO0
PT65B/PCLKC0_0 C11 S07L
{RAMADDR}
{Bank0OD}
{GPIO[1..0]}
FT_RXF and TXE lines
can be on any pin of this bank
FPGA_RESET
GPIO1
D8
PMEG3030EP,115
FT GPIO cannot be set to Open Drain
The diode blocks the 3v3 while allowing
to force a logical 0 in a wired-and
U1B
LFE5U-85F-6BG381
Bank 1
PT103A A15 FT_DATA0
PT105A B15 FT_DATA1
PT105B C15 FT_DATA10
PT107A D15 FT_DATA11
PT107B E15 FT_DATA15
PT110A A16 FT_DATA2
PT110B B16 FT_DATA3
PT112A C16 FT_DATA12
PT112B D16 FT_DATA14
PT114A B17 FT_DATA7
PT114B C17 FT_DATA13
PT116A A17 FT_DATA4
PT116B B18 FT_DATA5
PT119A A18 FT_DATA6
PT119B B19 FT_BE1
PT121A/URC_GPLL1T_IN A19 FT_BE0
PT121B/URC_GPLL1C_IN B20 FT_WR
PT69A/PCLKT1_1 D11 FT_DATA8
PT69B/PCLKC1_1 E11 FT_DATA9
PT71A/PCLKT1_0 B12 FT_CLK
PT71B/PCLKC1_0 C12 S10
PT74A/GR_PCLK1_0 D12 S11
PT74B/GR_PCLK1_1 E12 S12
PT76A A12 S13
PT76B A13 S14
PT78A B13 S15
PT78B C13 S16
PT80A D13 S17
PT80B E13 S18
PT83A A14 S19
PT83B C14 S110
PT85A D14 S111
PT85B E14
FT_TXE
FT_RXF
{FT600}
NB: FT_CLK must be in a PCLKT port
{Bank1S}
R1 0
FT_WAKEUP
U1C
LFE5U-85F-6BG381
Bank 2
PR11A/URC_GPLL0T_IN C18 D2I00+
PR11B/URC_GPLL0C_IN D17 D2I00-
PR11C E16 D2I0+
PR11D F16 D2I0-
PR14A D18 D2I01+
PR14B E17 D2I01-
PR14C E18 D2I1+
PR14D F18 D2I1-
PR17A F17 D2I02+
PR17B G18 D2I02-
PR17C G16 D2I2+
PR17D H16 D2I2-
PR20A H18 D2I03+
PR20B H17 D2I03-
PR20C J17 D2I3+
PR20D J16 D2I3-
PR29A K16 D2I05+
PR29B K17 D2I05-
PR35A C20 D2I04+
PR35B D19 D2I04-
PR35C/VREF1_2 D20 D2I4+
PR35D E19 D2I4-
PR38A E20 D2I06+
PR38B F19 D2I06-
PR38C F20 LED0
PR38D G20 LED1
PR41A/GR_PCLK2_1 G19 D2I07+
PR41B H20 D2I07-
PR41C/GR_PCLK2_0 J18 LED2
PR41D K18 LED3
PR44A/PCLKT2_1 J19 D2I08+
PR44B/PCLKC2_1 K19 D2I08-
PR44C/PCLKT2_0 J20
PR44D/PCLKC2_0 K20
{Bank2D}
{LED[0..3]}
NB: Clock can be here
or in PCLKT2_1
Enabled: HIGH or Open
OE
VDD
Out-
GND
Out+
SysClock-
SysClock+
U2
SiT9120AC-2C2-25E100.000000X
C1
100n
+2V5
GND
U1D
LFE5U-85F-6BG381
Bank 3
PR47A/PCLKT3_1 L20 D3I00+
PR47B/PCLKC3_1 M20 D3I00-
PR47C/PCLKT3_0 L19 D3I0+
PR47D/PCLKC3_0 M19 D3I0-
PR50A/GR_PCLK3_0 L16 D3I01+
PR50B L17 D3I01-
PR50C/GR_PCLK3_1 L18 D3I1+
PR50D M18 D3I1-
PR53A N16 D3I02+
PR53B M17 D3I02-
PR53C N18 D3I2+
PR53D P17 D3I2-
PR56A N17 D3I03+
PR56B/VREF1_3 P16 D3I03-
PR56C R16 D3I3+
PR56D R17 D3I3-
PR77A T16 FT_RSTReq
PR83A N19 D3I04+
PR83B N20 D3I04-
PR83C P19 D3I4+
PR83D P18 D3I4-
PR86A P20 D3I05+
PR86B R20 D3I05-
PR86C T20 D3I5+
PR86D U20 D3I5-
PR89A T19 D3I06+
PR89B R18 D3I06-
PR89C U19 D3I6+
PR89D T18 D3I6-
PR92A U18 D3I07+
PR92B U17 D3I07-
PR92C/LRC_GPLL0T_IN U16 D3I7+
PR92D/LRC_GPLL0C_IN T17 D3I7-
{Bank3D}
U1E
LFE5U-85F-6BG381
Bank 6
PL47A/PCLKT6_1 G2 D6I00+
PL47B/PCLKC6_1 F1 D6I00-
PL47C/PCLKT6_0 H2 D6I0+
PL47D/PCLKC6_0 G1 D6I0-
PL50A/GR_PCLK6_0 J4 D6I01+
PL50B J5 D6I01-
PL50C/GR_PCLK6_1 J3 D6I1+
PL50D K3 D6I1-
PL53A K2 D6I02+
PL53B J1 D6I02-
PL53C H1 D6I2+
PL53D K1 D6I2-
PL56A K4 D6I03+
PL56B/VREF1_6 K5 D6I03-
PL56C L4 D6I3+
PL56D L5 D6I3-
PL77A M5 S60
PL83A M4 D6I04+
PL83B N5 D6I04-
PL83C N4 D6I4+
PL83D P5 D6I4-
PL86A N3 D6I05+
PL86B M3 D6I05-
PL86C L3 D6I5+
PL86D L2 D6I5-
PL89A N2 D6I06+
PL89B M1 D6I06-
PL89C L1 D6I6+
PL89D N1 D6I6-
PL92A P1 D6I07+
PL92B P2 D6I07-
PL92C/LLC_GPLL0T_IN P3 D6I7+
PL92D/LLC_GPLL0C_IN P4 D6I7-
{Bank6D}
U1F
LFE5U-85F-6BG381
Bank 7
PL11A/ULC_GPLL0T_IN A4 RAM_DQ1
PL11B/ULC_GPLL0C_IN A5 RAM_DQ7
PL11C B5 RAM_DQ5
PL11D C5 RAM_DQ4
PL14A C4 RAM_DQ6
PL14B B4 RAM_DQ3
PL14C A3 RAM_LDM
PL14D B3 RAM_DQ2
PL17A E4 RAM_LDQS+
PL17B D5 RAM_LDQS-
PL17C C3 RAM_DQ0
PL17D D3 RAM_CS
PL20A F4 RAM_CK+
PL20B E3 RAM_CK-
PL20C E5 RAM_CKE
PL20D F5 RAM_RESET
PL35A A2 RAM_DQ8
PL35B B1 RAM_UDM
PL35C/_VREF1_7 B2
PL35D C2 RAM_DQ9
PL38A C1 RAM_DQ11
PL38B D1 RAM_DQ15
PL38C D2 RAM_DQ10
PL38D E1 RAM_DQ13
PL41A/GR_PCLK7_1 H4 RAM_UDQS+
PL41B G5 RAM_UDQS-
PL41C/GR_PCLK7_0 H5 RAM_DQ12
PL41D H3 RAM_DQ14
PL44A/PCLKT7_1 G3 RAM_WE
PL44B/PCLKC7_1 F3 RAM_RAS
PL44C/PCLKT7_0 F2 RAM_CAS
PL44D/PCLKC7_0 E2 RAM_ODT
{DQL}
{DQU}
{RAMCTRL}
NB: PL11-20 and 35-44 are
2 independent DQ groups DQ
lines (except DQS, those
have fixed locations) can
be moved around inside the
group. Or both groups
switched entirely. Non-DQ
signals can be moved around
the remaining pins
NB: PLxxA/C are positive and
B/D are negative. Only A/B pairs
can act as an output.
DDR_VREF
C5
100n
C4
10n
GND
U1G
Bank 8
LFE5U-85F-6BG381
PB4A/D7/IO7 R1 S80
PB4B/D6/IO6 T1 S81
PB6A/D5/MISO2/IO5 U1 S82
PB6B/D4/MOSI2/IO4 V1 S83
PB9A/D3/IO3 W1 FD3
PB9B/D2/IO2 Y2 FD2
PB11A/D1/MISO/IO1 V2 FMISO
PB11B/D0/MOSI/IO0 W2 FMOSI
PB13A/SN/CSN T2 S84
PB13B/CS1N U2 S85
PB15A/HOLDN/DI/BUSY/CSSPIN/CEN R2 FCS
PB15B/DOUT/CSON R3 S86
PB18A/WRITEN T3 FPGA_RESETrq
{Bank8S}
TP2
TestPoint
D9
D_Schottky
FPGA_RESET
This diode allows the wired-and to work even if the
port were configured in push-pull, avoiding locking
reset to bootloader by ftdi pin
U1H
LFE5U-85F-6BG381
CCLK/MCLK/SCK U3 FCLK
CFG_0 U4
CFG_1 T4
CFG_2 R4
PROGRAM W3
INIT V3
DONE Y3
TDO V4
TCK T5
TDI R5
TMS U5
RESERVED W4
RESERVED W5
RESERVED W8
RESERVED W9
RESERVED W10
RESERVED W11
RESERVED W13
RESERVED W14
RESERVED W17
RESERVED W18
+3V3
1k R15
1k R16
4.7k R17
10k R18
10k R19
0 R20
FPGA_RESET
INIT
DONE
R22 4.7k
J3
JTAG
GND
C6
100n
U3
W25Q128JVP
FMOSI 5
FMISO 2
FD2 3
FD3 7
DI(IO0)
DO(IO1)
WP(IO2)
RESET(IO3)
VCC
CS
CLK
EP
GND
R21
4.7k
FCS
FCLK
U10
NLSX3018
VCC 16
GND 15
VL 5
EN 6
I/O_VCC1 S07 20
I/O_VCC2 S01 19
I/O_VCC3 S02 18
I/O_VCC4 S04 17
I/O_VCC5 S06 14
I/O_VCC6 S00 13
I/O_VCC7 S03 12
I/O_VCC8 S05 11
I/O_VL1 1 S07L
I/O_VL2 2 S01L
I/O_VL3 3 S02L
I/O_VL4 4 S04L
I/O_VL5 7 S06L
I/O_VL6 8 S00L
I/O_VL7 9 S03L
I/O_VL8 10 S05L
{Bank0S}
{Bank0OD}
C2
100n
C3
100n
RAM_VDD
Aarón Cuevas López
Jonathan Newman
OEPS & Open Ephys, Inc.
Sheet: /FPGA/
File: FPGA.kicad_sch
Title: ECP5U85-BSE-USB Breakout Board
Size: A3
Date: 2022-02-02
Rev: A
KiCad E.D.A. kicad (6.0.0)
Id: 2/5



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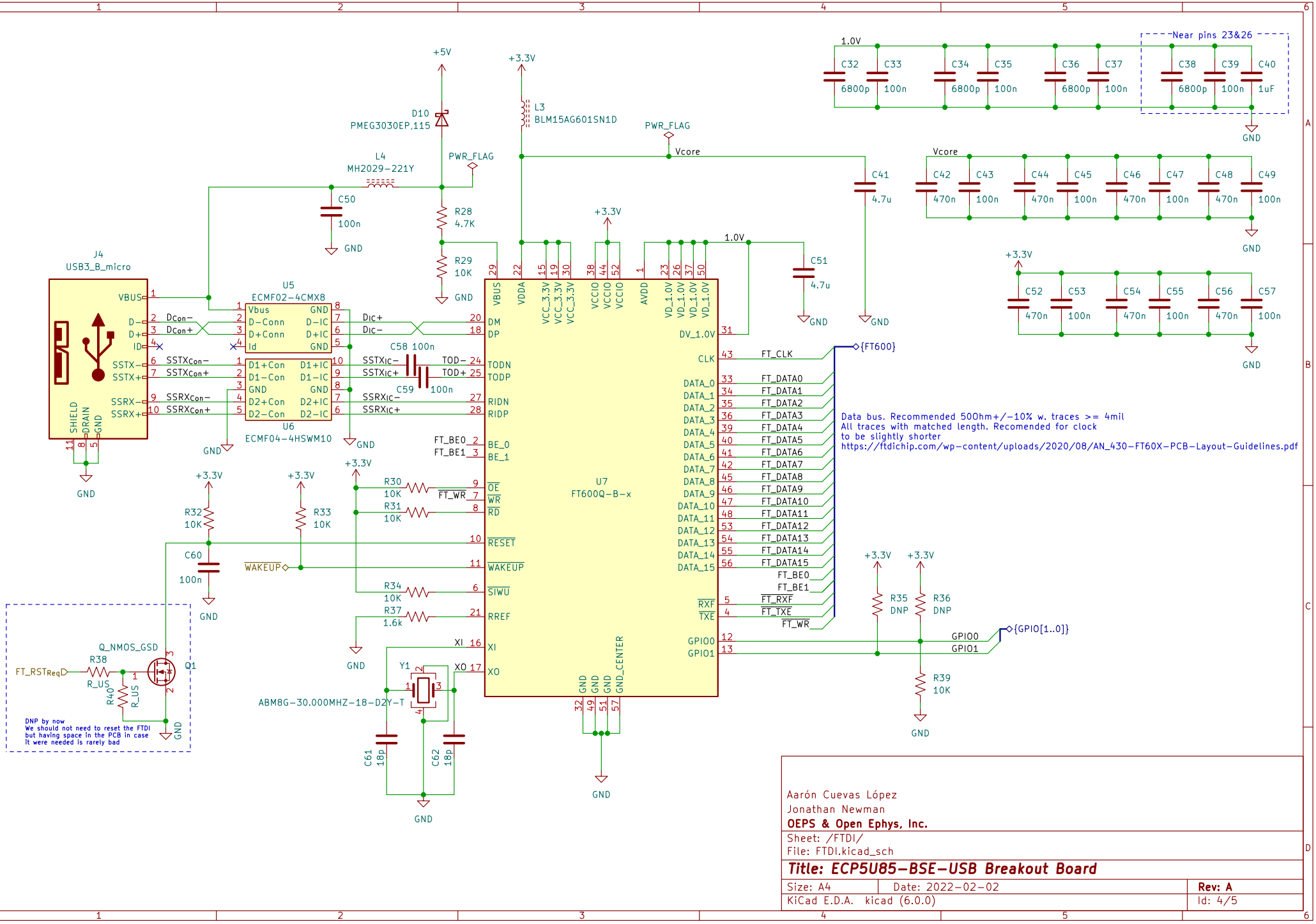
Jonathan Newman
OEPS & Open Ephys, Inc.

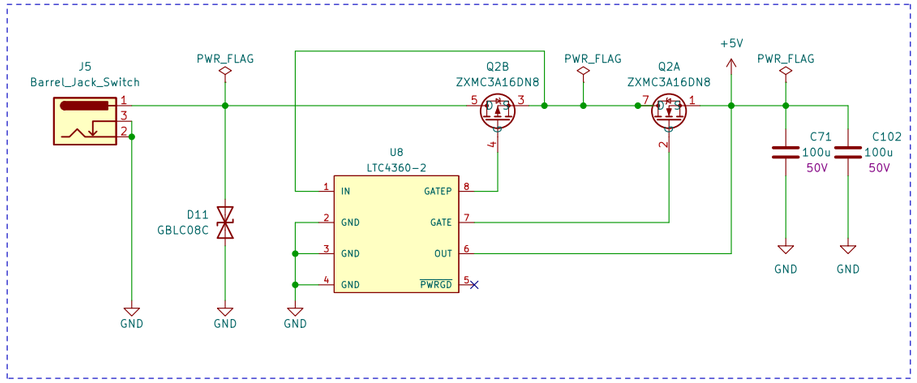
Sheet: /RAM/
File: RAM.kicad_sch

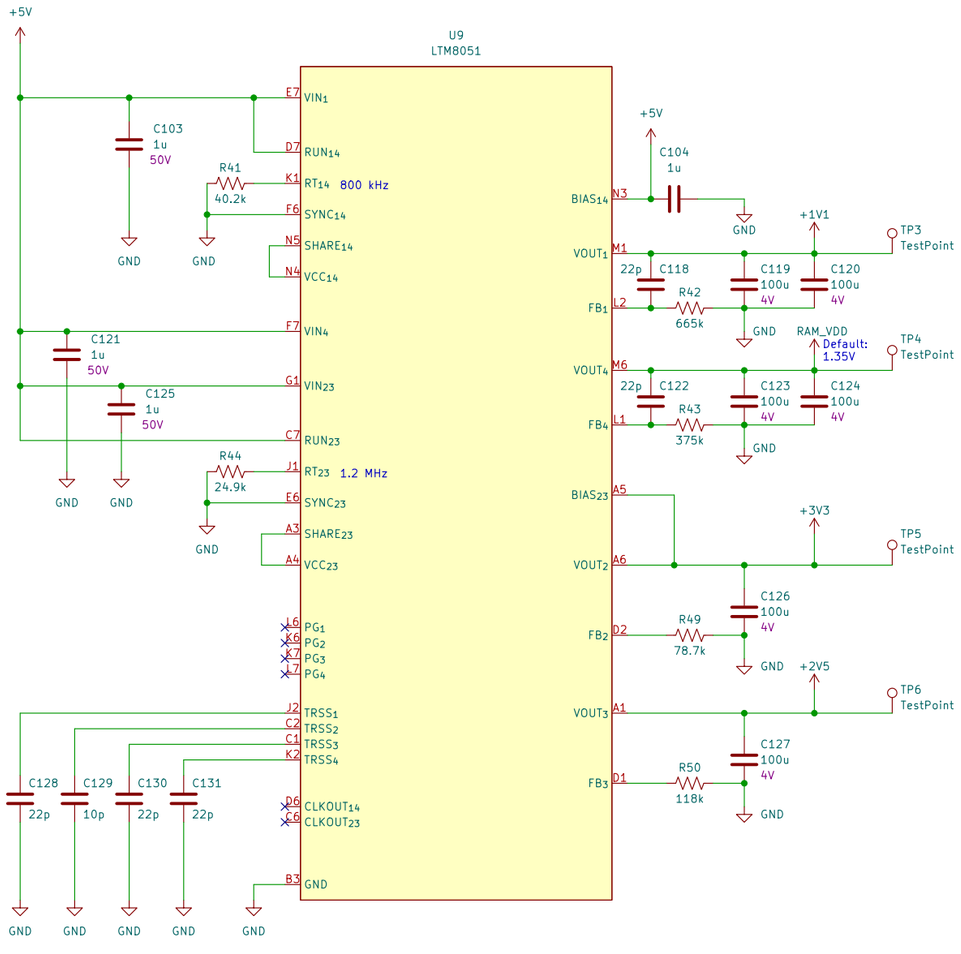
Title: ECP5U85-BSE-USB Breakout Board

Size: A4	Date: 2022-02-02	**Rev: A**
KiCad E.D.A. kicad (6.0.0)		Id: 3/5

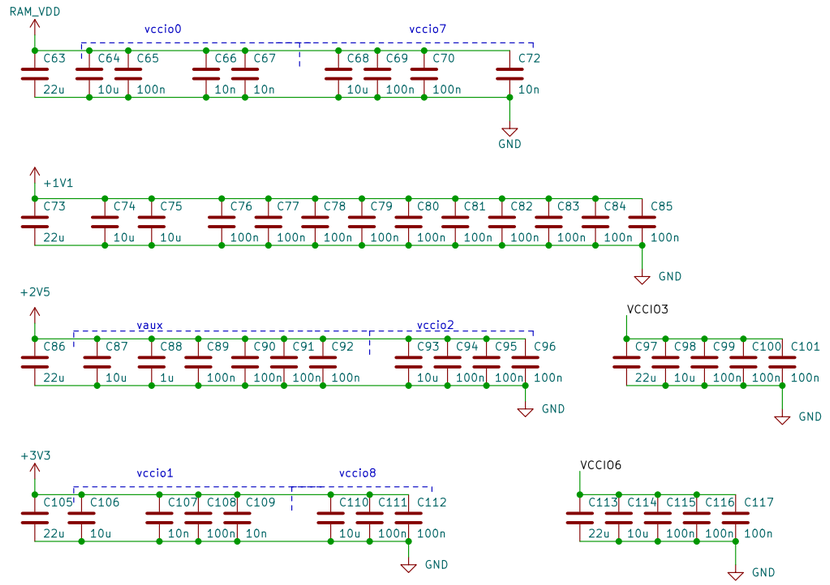

Near pins 23&26
1.0V
C32 6800p
C33 100n
C34 6800p
C35 100n
C36 6800p
C37 100n
C38 6800p
C39 100n
C40 1uF
GND
Vcore
C41 4.7u
C42 470n
C43 100n
C44 470n
C45 100n
C46 470n
C47 100n
C48 470n
C49 100n
+3.3V
C52 470n
C53 100n
C54 470n
C55 100n
C56 470n
C57 100n
+5V
D10
PMEG3030EP,115
L3
BLM15AG601SN1D
PWR_FLAG
L4
MH2029-221Y
C50 100n
R28 4.7K
R29 10K
C51 4.7u
J4
USB3_B_micro
VBUS
D-
D+
ID
SSTX-
SSTX+
SSRX-
SSRX+
SHIELD
DRAIN
GND
U5
ECMF02-4CMX8
U6
ECMF04-4HSWM10
C58 100n
C59 100n
U7
FT600Q-B-x
DM
DP
TODN
TODP
RIDN
RIDP
BE_0
BE_1
OE
WR
RD
RESET
WAKEUP
SIWU
RREF
XI
XO
CLK
DATA_0
DATA_1
DATA_2
DATA_3
DATA_4
DATA_5
DATA_6
DATA_7
DATA_8
DATA_9
DATA_10
DATA_11
DATA_12
DATA_13
DATA_14
DATA_15
RXF
TXE
GPIO0
GPIO1
DV_1.0V
FT_CLK
FT_DATA0
FT_DATA1
FT_DATA2
FT_DATA3
FT_DATA4
FT_DATA5
FT_DATA6
FT_DATA7
FT_DATA8
FT_DATA9
FT_DATA10
FT_DATA11
FT_DATA12
FT_DATA13
FT_DATA14
FT_DATA15
FT_BE0
FT_BE1
FT_RXF
FT_TXE
FT_WR
{FT600}
{GPIO[1..0]}
R30 10K
R31 10K
R32 10K
R33 10K
R34 10K
R35 DNP
R36 DNP
R37 1.6k
R39 10K
C60 100n
Y1
ABM8G-30.000MHZ-18-D2Y-T
C61 18p
C62 18p
Q_NMOS_GSD
Q1
R38
R_US
R40
FT_RSTReq
DNP by now
We should not need to reset the FTDI
but having space in the PCB in case
it were needed is rarely bad
Data bus. Recommended 50Ohm+/-10% w. traces >= 4mil
All traces with matched length. Recomended for clock
to be slightly shorter
https://ftdichip.com/wp-content/uploads/2020/08/AN_430-FT60X-PCB-Layout-Guidelines.pdf
Aarón Cuevas López
Jonathan Newman
OEPS & Open Ephys, Inc.
Sheet: /FTDI/
File: FTDI.kicad_sch
Title: ECP5U85-BSE-USB Breakout Board
Size: A4
Date: 2022-02-02
Rev: A
KiCad E.D.A. kicad (6.0.0)
Id: 4/5

Power Regulation



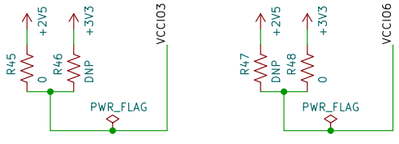


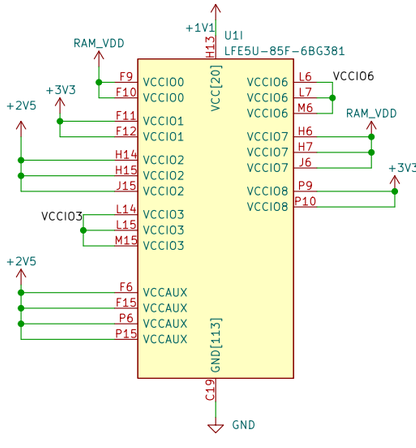
FPGA Power



This is for future-proofing. This way bank3 (most of even row of right samtec) could behave as 2v5 lvds as it is now, or 3v3 (single ended or differential) The same way, bank6 (most of even part od left samtec and half rhe odd) could act as 3v3 (now is 3v3 single) or provide differential signals.

If this becomes an issue, we can just get rid of this and connect vccio3 fixed to 2v5 and vccio6 fixed to 3v3, which is the way it is compatible with the acquisition board.





Aarón Cuevas López
Jonathan Newman
OEPS & Open Ephys, Inc.

Sheet: /Power/
File: Power.kicad_sch

Title: ECP5U85-BSE-USB Breakout Board

Size: A3	Date: 2022-02-02	**Rev: A**
KiCad E.D.A. kicad (6.0.0)		Id: 5/5