

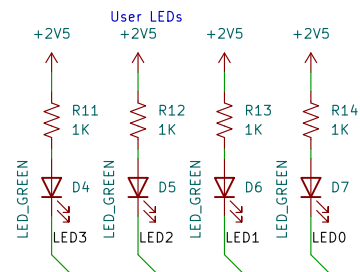
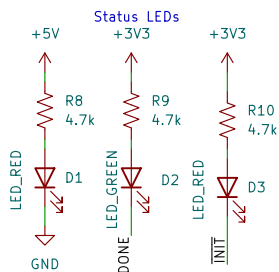
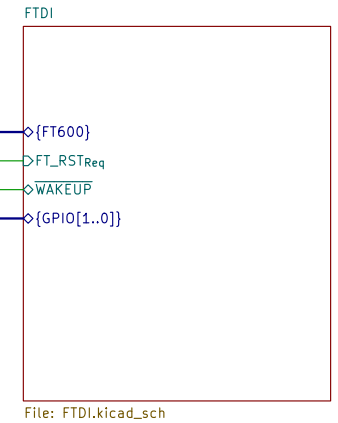
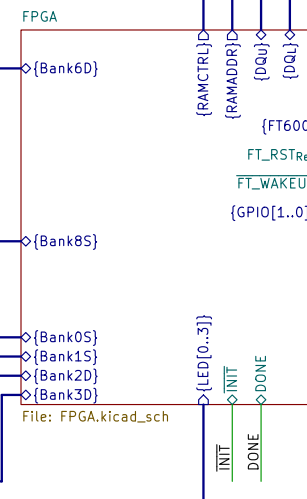
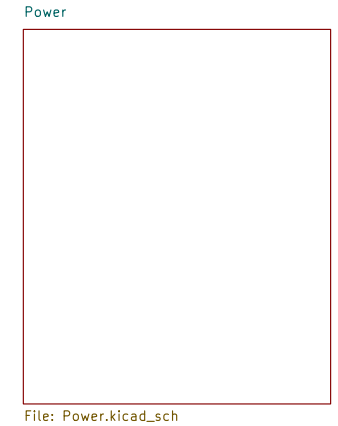
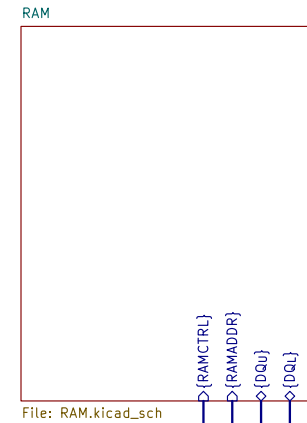
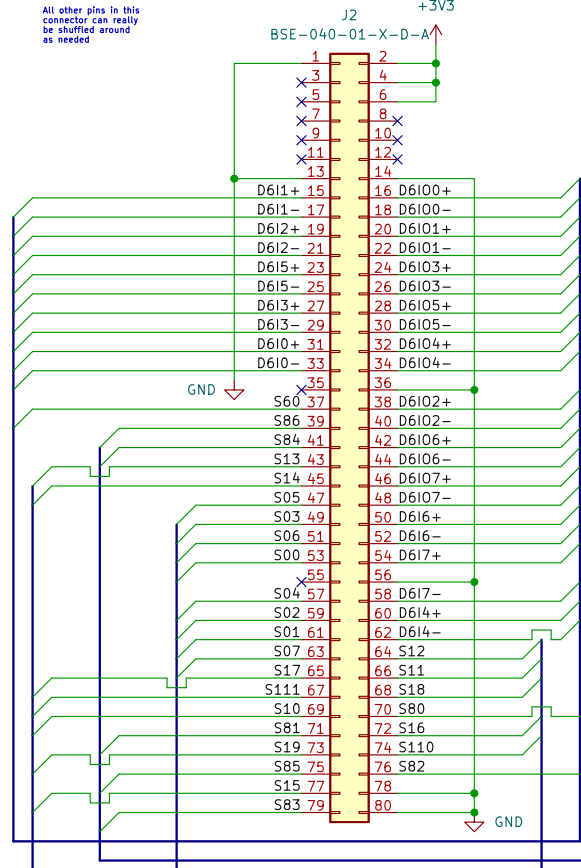
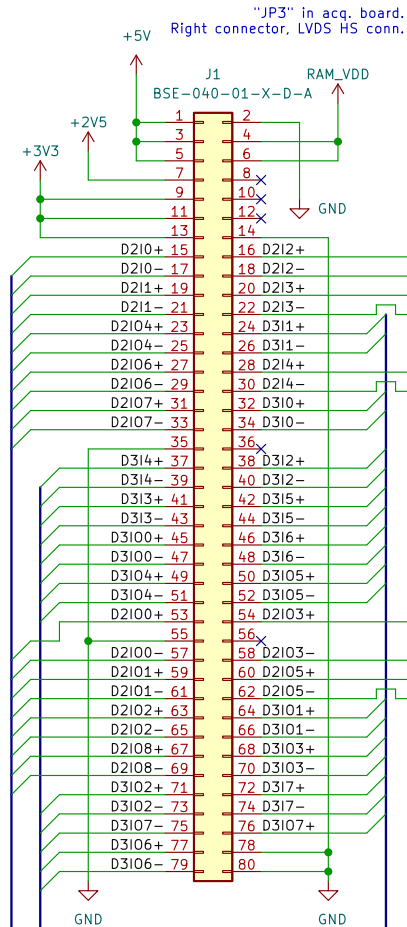
The only differential pairs used in the OE acq. board are in the headstage connector, and not even all of it. All other differential pairs can be moved around or routed as single lines if needed, but keeping as much diff pairs as possible is more future proof

In summary:  
 - J1 (except even pins 32-47): KEEP I/O and polarity.  
 - J1 pins 32-47: Do what's easiest. Keeping diff pairs is recommended  
 - J2: Do what's easiest, except S0[0-7]. Keeping diff pairs is recommended

Possible locations for S0[0-7]:  
 - pins 47-63  
 - pins 29-45  
 - pins 65-79

All other pins in this connector can really be shuffled around as needed

Even pins 32-74 are not really used in the acq. board (32-33 for daisy chain conn. 74 to gnd. Others to breakout section). So they can be moved freely.



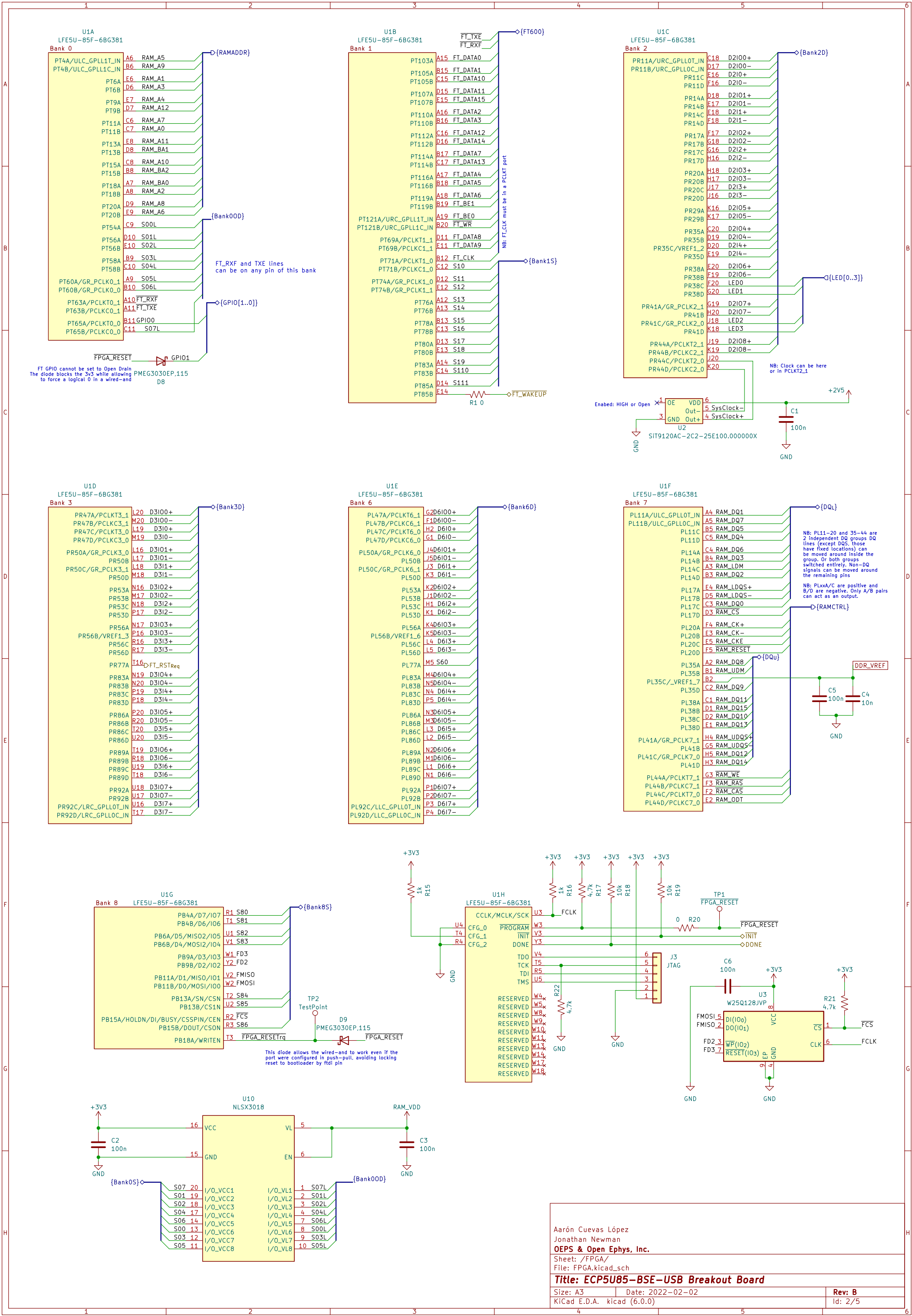
Aarón Cuevas López  
 Jonathan Newman  
**OEPS & Open Ephys, Inc.**

Sheet: /  
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**Title: ECP5U85-BSE-USB Breakout Board**

Size: A4 Date: 2022-02-02  
 KiCad E.D.A. kicad (6.0.0)

Rev: B  
 Id: 1/5



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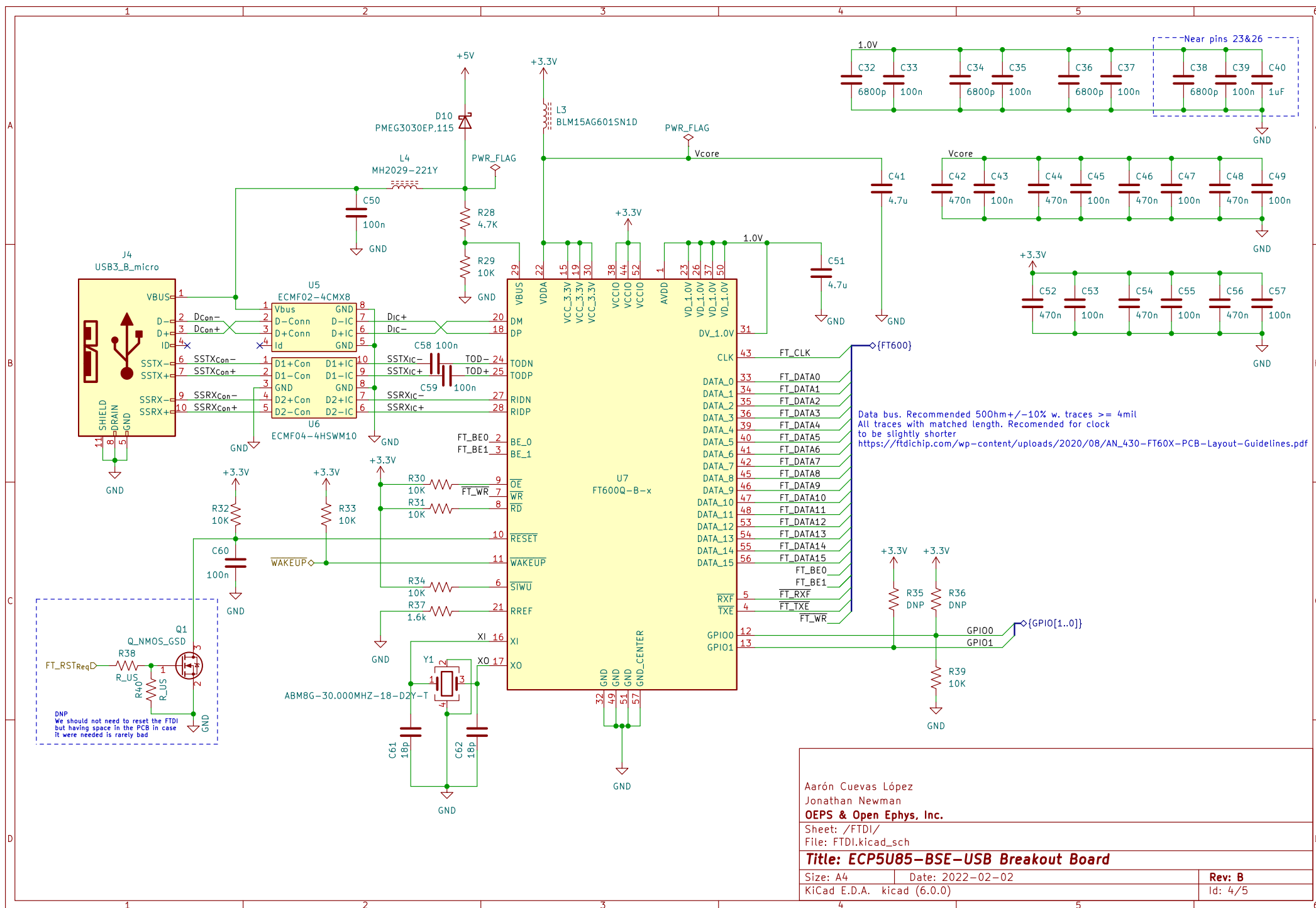
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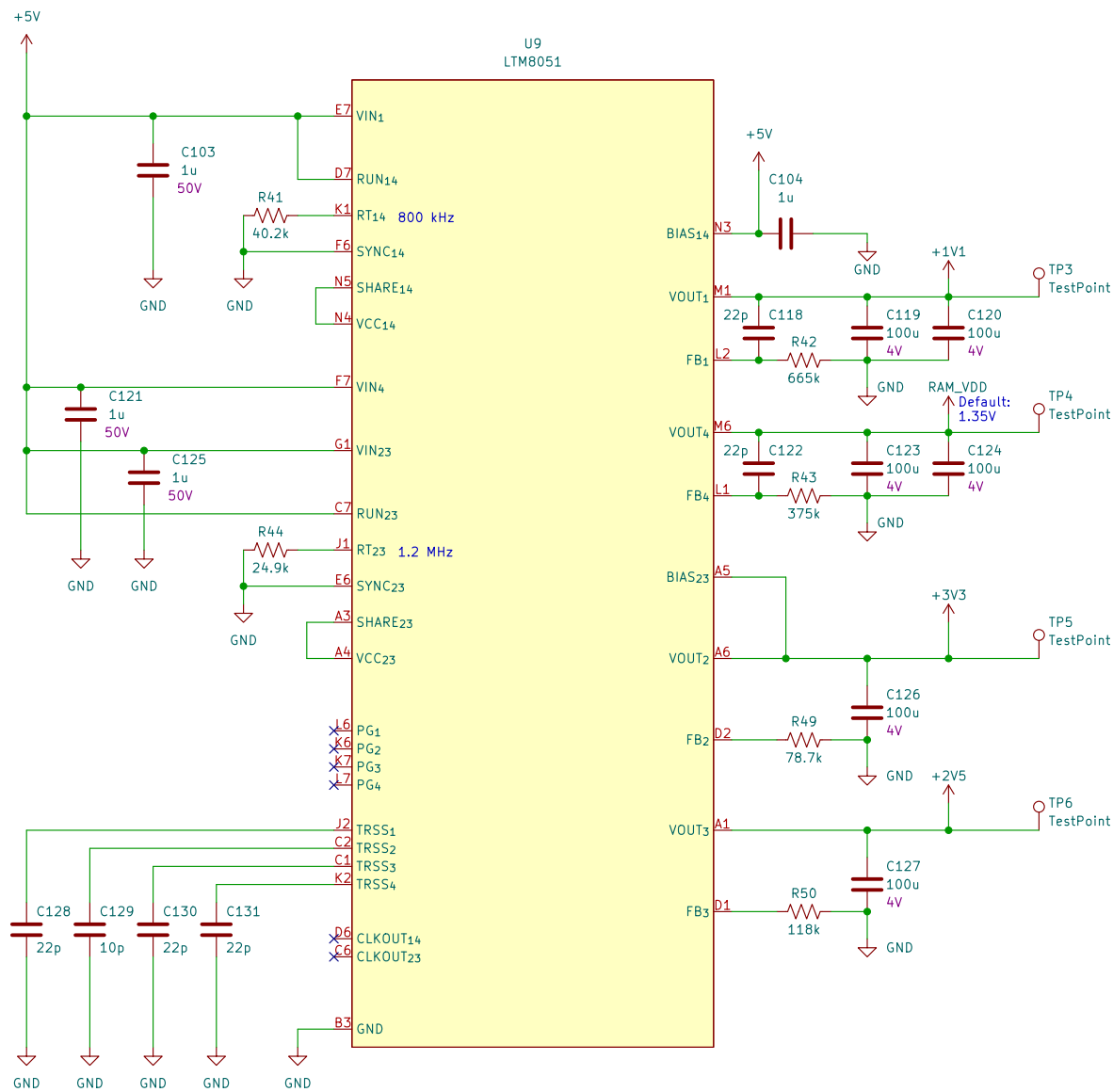
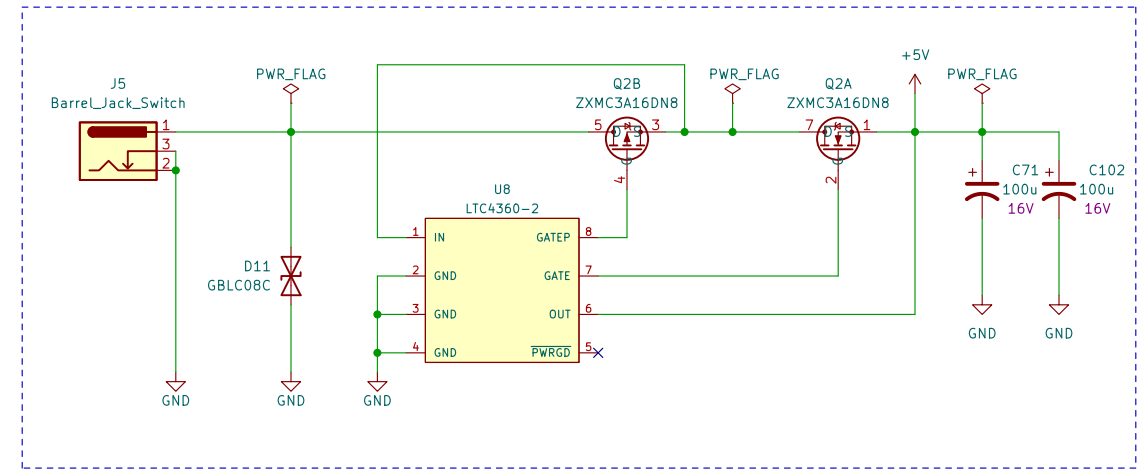
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KiCad E.D.A. kicad (6.0.0)

Rev: B  
Id: 2/5





Power Regulation



FPGA Power

