







## FPGA Power Power Regulation PWR\_FLAG PWR\_FLAG PWR FLAG Q2A ZXMC3A16DN8 J5 Barrel\_Jack\_Switch Q2B ZXMC3A16DN8 5 (PI) 7 <u>√</u> 2 C71 + C102 C68 C69 C70 U8 LTC4360-2 u 100u 16V 16V D11 GBLC08C 1+1V1 PWRGD 5 → GND +2V5 VCCI03 C87 C88 C89 C90 C91 C92 10u 1u 100n 100n 100n 100n C93 C94 C95 C96 +5V C97 C98 C99 C100 C101 U9 LTM8051 $\stackrel{\textstyle \downarrow}{\smile}$ GND +5V C103 VCCI06 C104 vccio1 vccio8 1u $\rightarrow$ ↓ GND GND GND R42 -**VVV**-665k GND RAM\_VDD AM\_VDD Default: TP4 1.35V TestPoint C121 22p C122 R43 M-375k C123 C124 100u 100u 4V 4V C124 +1V1 U1I LFE5U-85F-6BG381 This is for future-proofing. This way bank3 (most of even row of right samtec) could behave as 2v5 [vds as it is now, or 3v3 (single ended or differential) The same way, bank6 (most of even part od left samtec and half rhe odd) could act as 3v3 (now is 3v3 single) or provide differential signals. UN23 GND 24.9k RT23 1.2 MHz VCCIO BIAS23 GND GND VCCI07 SYNC<sub>23</sub> SHARE23 TP5 TestPoint ACCIO. GND VCCI08 VOUT<sub>2</sub> VCCI03 C126 100u 4V PWR\_FLAG PWR\_FLAG /CCAUX → GND +2V5 F15 VCCAUX P6 VCCAUX TP6 TestPoint C2 TRSS2 C1 TRSS3 TRSS3 C127 C128 C129 C130 C131 --\/\/\-118k ↓ GND 10p CLKOUT14 CLKOUT23 22p GND GND GND GND Aarón Cuevas López Jonathan Newman OEPS & Open Ephys, Inc. Sheet: /Power/ File: Power.kicad\_sch Title: ECP5U85-BSE-USB Breakout Board Size: A3 Date: 2022-02-02 KiCad E.D.A. kicad (6.0.0)