IRNSS Receiver

Group No: B17

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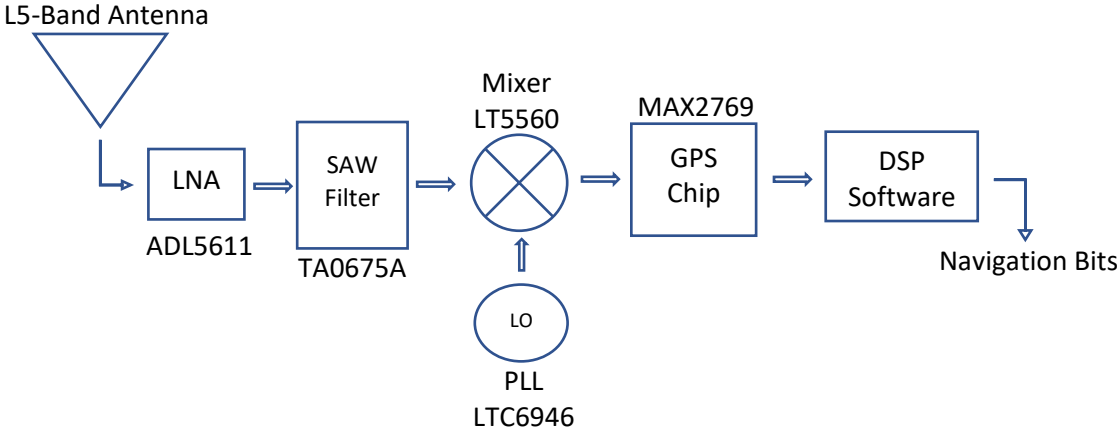
Objectives:

- To design the RF front-end of IRNSS receiver on a single PCB.
- To design an antenna for the L5 band (1176.45 MHz).

Block Diagram:



Subsystems Designed/Completed:

- Simulated and designed a dual-feed square MSA with a 3 dB two-branch line coupler on ZELAND IE3D software.
- Circuits for each block have been finalised (including values of RLCs)
- PCB of the front-end has been designed.
- Code for configuring PLL has been tested on the IQ Modulator board. (We are using the same PLL for our project)

Major Results:

- We verified that the antenna met the required specifications by testing using a Vector Network Analyser (VNA).
  Antenna S11 parameter result –
  -10 dB bandwidth: 979.58 MHz to 1278.8 MHz.
  This corresponds to a VSWR less than 1.9 in the desired frequency range.

  We observed a difference of 7 dB in S21 parameter between source co-polarisation and source cross polarisation at our center frequency.

- Testing of PLL on IQ Modulator board has been successful. We were able to generate required LO (2751.87 MHz) and observe it on a spectrum analyser. However, the power of LO obtained was very low, around -29 dBm, as opposed to the requirement of atleast -2 dBm.

  This loss can be attributed to the fact that the loop filter, impedance matching circuits and the IQ modulator chip weren't designed for our frequency.

Evaluation 2 Demo:

We plan to demonstrate the working of our antenna.

We shall program the PLL on IQ Modulator board and demonstrate its working.

Further plan:

We expect to receive our PCB by the end of next week. We will try to complete the code for configuring the GPS chip meanwhile. After we receive our PCB, we shall test the individual blocks and then integrate all the subsystems.