Project 2 - Fault tolerant FIR filter implemented using N-modular redundancy technique

Create a fault-tolerant FIR filter using the N-modular redundancy hardware fault tolerance approach. Let the FIR filter be a 10^{th} order filter, and the number of modules in the redundant system, N, should be equal to 5.
VHDL model of the FIR filter must allow the user to specify the values of the filter coefficients (b_i) as well as the location and the type of the fault that is present in the filter (if any). Use the following block diagram to develop the VHDL model of the filter.

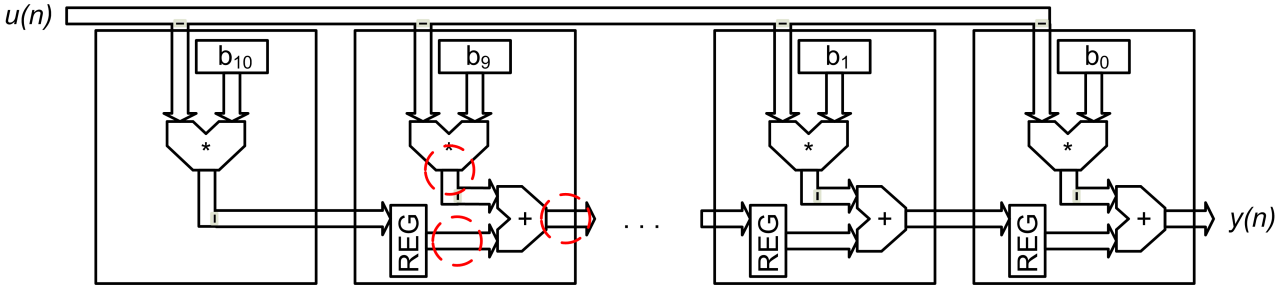

Figure 1. Architecture of the 10^{th} order FIR filter

Locations of the possible faults that should be modeled are highlighted by the red circles. Please note that faults in these locations can be present in every module that makes the filter.
When developing the fault tolerant FIR filter the N-modular redundancy hardware fault tolerance approach should be used. Fault tolerant architecture that should be developed is presented in the Figure 2.

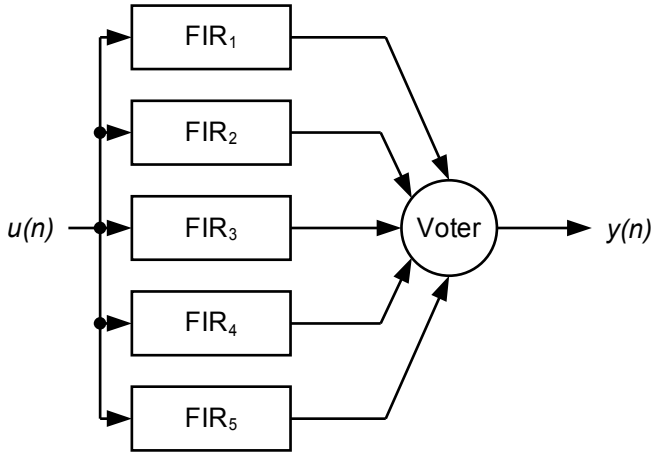

Figure 2. Fault tolerant FIR filter architecture

Fault tolerant architecture has 5 identical FIR modules that can be switched on and off depending on the decision that is made inside the voter module.

Tasks that must the done in order to finish the project:

1. Develop a VHDL model of the 10^{th} order FIR filter based on the architecture in Figure 1 that enables the user to specify the coefficient values and to insert the fault at the desired location inside the filter.
2. Develop a VHDL model of the fault tolerant FIR filter system based on the architecture in Figure 2.
3. Develop a testbench that will test the operation of the fault tolerant FIR filter architecture in case when faults are inserted randomly into the system. Simulation should clearly illustrate the operation of the fault masking mechanism that is the basis of the N-modular redundancy hardware fault tolerance approach.