Datasheet for 144 pins FPGA board PCB

EVD17I009

EVD17I014

ESD17I012

EVD17I020

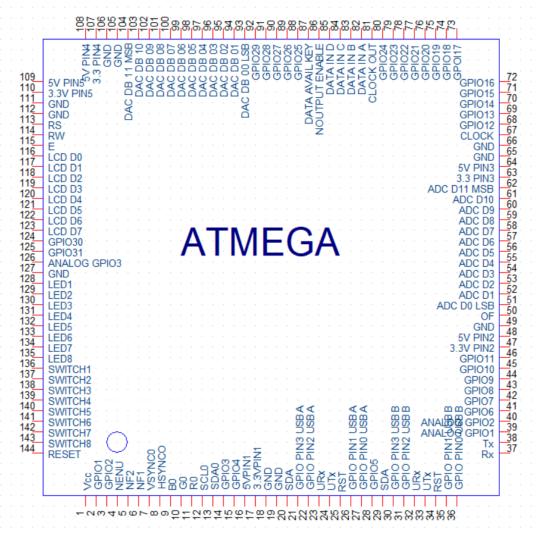
ESD17I009

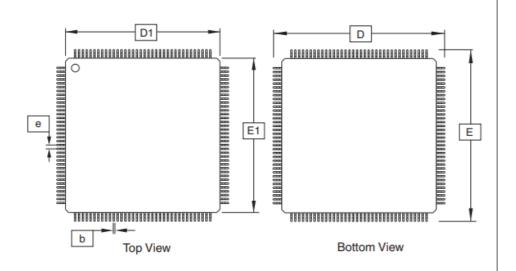
List of Contents:

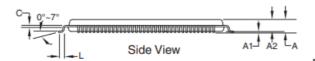
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1.Fpga core IC









COMMON DIMENSIONS (Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----------|------|--------|
| Α | - | _ | 1.60 | |
| A1 | 0.05 | - | 0.15 | |
| A2 | 1.35 | 1.40 | 1.45 | |
| D | | 22.00 BSC | | |
| D1 | | Note 2 | | |
| E | | | | |
| E1 | 20.00 BSC | | | Note 2 |
| b | 0.17 | 0.22 | 0.27 | |
| С | 0.09 - | | 0.20 | |
| L | 0.45 | 0.60 0.75 | | |
| e | | | | |

Notes: 1. This package conforms to JEDEC reference MS-026, Variation BFB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

| Pinno | Name | Function |
|-------|------------|---|
| 1 | Vcc | Supply voltage 3.3v |
| 2 | GPi/o1/GND | General purpose input output, also dedicated to ic ground |
| 3 | ŒPi/o2 | General purpose input output |
| 4 | NENU ENU) | USB Enable Input. Drive ENU low to enable the USB power-supply outputs.(Active Low) |

| | T . | T | | | |
|------------|------------------|--|--|--|--|
| 5 | NF2(F2) | Fault Output 2. F2 is an active-low, open-drain output that asserts when a fault condition is detected on USB2 | | | |
| 6 | NFI(F1) | Fault Output 1. F1 is an active-low, open-drain | | | |
| | | output that asserts when a fault condition is | | | |
| | | detected on USB1 | | | |
| 7 | VSYNCO | Vertical Sync Input | | | |
| 8 | HEAVOO | Horizontal Sync Input | | | |
| 9 | B 0 | RGB Analog Input | | | |
| 10 | G 0 | RGB Analog Input | | | |
| 11 | R0 | RGB Analog Input | | | |
| 12 | SOLO | DDC(digital down converter) Input/Output | | | |
| 13 | SDA0 | DDC(digital down converter) Input/Output | | | |
| 14 | œ1/03 | General purpose input output | | | |
| 15 | GPI/04 | General purpose input output | | | |
| 16 | 5VPin1 | 5V output | | | |
| 17 | 3.3VPin1 | 3.3V output | | | |
| 18 | GND | Dedicated Ground Pin | | | |
| 19 | GND | Dedicated Ground Pin | | | |
| 20 | SDA | I^2C Data line | | | |
| 2 1 | Œi∕oPin3 | General-purpose I/O or alternate | | | |
| | USBA | function pin | | | |
| 22 | Œi∕oPin2 | General-purpose I/O or alternate | | | |
| | USBA | function pin | | | |
| 23 | UR x | UART RX pin (input) | | | |
| 24 | UTx | UART TX pin (Output) | | | |
| 25 | RST | reset | | | |
| 26 | Œi∕oPin1 | General-purpose I/O or alternate | | | |
| | USBA | function pin | | | |
| 2 7 | ŒPi∕oPin0 | General-purpose I/O or alternate | | | |
| | USBA | function pin | | | |
| 28 | GPI/05/Nbt | General purpose input output/ not connected | | | |
| | Connected | | | | |
| 29 | SDA | I^2C Data line | | | |
| 30 | Œi∕oPin3 | General-purpose I/O or alternate | | | |
| | USBA | function pin | | | |
| | • | · | | | |

| 31 | Œi/oPin2 | General-purpose I/O or alternate | | |
|------------|-----------|--|--|--|
| | USBA | function pin | | |
| 32 | URx | UART RX pin (input) | | |
| 33 | UTx | UART TX pin (Output) | | |
| 34 | RST | General purpose input output | | |
| 35 | ŒPi∕oPin1 | General-purpose I/O or alternate | | |
| | USBA | function pin | | |
| 36 | GPi∕oPin0 | General-purpose I/O or alternate | | |
| | USBA | function pin | | |
| 37 | Rx | Serial receiver | | |
| 38 | Tx | Serial transmitter | | |
| 39 | Analog CP | Analog General purpose input output | | |
| | i/o1 | | | |
| 40 | Analog GP | Analog General purpose input output | | |
| | i/o2 | | | |
| 41 | Œ1/06 | General purpose input output | | |
| 42 | GPI/07 | General purpose input output | | |
| 43 | œ1/08 | General purpose input output | | |
| 44 | Œ1/09 | General purpose input output | | |
| 45 | GPI/010 | General purpose input output | | |
| 46 | GPI/011 | General purpose input output | | |
| 47 | 3.3VPin2 | 3.3V output | | |
| 48 | 5VPin2 | 5V output | | |
| 49 | GND | Dedicated Ground Pin | | |
| 50 | OF . | Overflow Output. This signal is high when the | | |
| | | digital output is 011111111111 or 10000000000. | | |
| 51 | ACC COLSB | Data Outputs. The output format | | |
| E 2 | ADCD | is two's complement. | | |
| 52 | ADCDI | Data Outputs. The output format is two's complement. | | |
| 53 | ADC D2 | Data Outputs. The output format | | |
| | | is two's complement. | | |
| 54 | ACCB | Data Outputs. The output format | | |
| | | is two's complement. | | |
| 55 | ADC D4 | Data Outputs. The output format | | |
| F/ | ADOPT | is two's complement. | | |
| 56 | ADC D5 | Data Outputs. The output format | | |

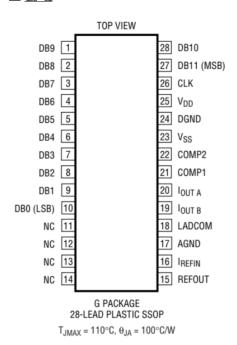
| | | is two's complement. | | |
|------------|-------------|--|--|--|
| 57 | ADC D6 | Data Outputs. The output format | | |
| | | is two's complement. | | |
| 58 | ADC D7 | Data Outputs. The output format | | |
| | | is two's complement. | | |
| 59 | ADC D8 | Data Outputs. The output format | | |
| | 10000 | is two's complement. | | |
| 60 | ADC D9 | Data Outputs. The output format | | |
| /1 | ADCIDIO | is two's complement. | | |
| 61 | ADC DIO | Data Outputs. The output format is two's complement. | | |
| 62 | ADC DI1 MSB | Data Outputs. The output format | | |
| 02 | ACCITION | is two's complement. | | |
| 63 | 3.3VPin3 | 3.3V output | | |
| 64 | 5VPin3 | 5V output | | |
| 65 | GND | Dedicated Ground Pin | | |
| 66 | G\D | Dedicated Ground Pin | | |
| 67 | arak | Crystal oscillator input (upto 50Mhz) | | |
| 68 | GPI/012 | General purpose input output | | |
| 69 | GPI/013 | General purpose input output | | |
| 7 0 | GPI/014 | General purpose input output | | |
| 71 | GPI/015 | General purpose input output | | |
| 72 | GP1/016 | General purpose input output | | |
| 7 3 | GPI/017 | General purpose input output | | |
| 74 | GPI/018 | General purpose input output | | |
| 7 5 | GPI/019 | General purpose input output | | |
| 76 | œ/020 | General purpose input output | | |
| 7 7 | GPI/021 | General purpose input output | | |
| 78 | œ/022 | General purpose input output | | |
| 7 9 | GPI/023 | General purpose input output | | |
| 80 | GPI/024 | General purpose input output | | |
| 81 | Clock Out | 50Mhz clock out | | |
| 82 | DATAINA | Data channel b/w encoder and core ICs | | |
| 83 | DATAINB | Data channel b/w encoder and core ICs | | |
| 84 | DATAINC | Data channel b/w encoder and core ICs | | |
| 85 | DATAIND | Data channel b/w encoder and core ICs | | |
| w | | Data dilatility of the dilated and cold los | | |

| 86 | NOUTPUT | Active low, output enabler for keypad encoder | | |
|-----|------------|---|--|--|
| | EVABLE | | | |
| 87 | DATA AVAIL | Active high for no data passing(indicates that input | | |
| | KEY | is possible) | | |
| 88 | GPI/025 | General purpose input output | | |
| 89 | GPI/026 | General purpose input output | | |
| 90 | GPI/027 | General purpose input output | | |
| 91 | GPI/028 | General purpose input output | | |
| 92 | GPI/029 | General purpose input output | | |
| 93 | DACDB00 | Digital Output Data Bits. | | |
| | LSB | | | |
| 94 | DACDB01 | Digital Output Data Bits. | | |
| 95 | DACDB02 | Digital Output Data Bits. | | |
| 96 | DACDB03 | Digital Output Data Bits. | | |
| 97 | DACDB04 | Digital Output Data Bits. | | |
| 98 | DACDB05 | Digital Output Data Bits. | | |
| 99 | DACDB06 | Digital Output Data Bits. | | |
| 100 | DACDB07 | Digital Output Data Bits. | | |
| 101 | DACDB08 | Digital Output Data Bits. | | |
| 102 | DACDB09 | Digital Output Data Bits. | | |
| 103 | DACDB10 | Digital Output Data Bits. | | |
| 104 | DAC DB11 | Digital Output Data Bits. | | |
| | MSB | | | |
| 105 | GND | Dedicated Ground Pin | | |
| 106 | GND | Dedicated Ground Pin | | |
| 107 | 3.3VPIN4 | 3.3V output | | |
| 108 | 5VPIN4 | 5V output | | |
| 109 | 5VPIN5 | 5V output | | |
| 110 | 3.3VPIN5 | 3.3V output | | |
| 111 | G/VD | Dedicated Ground Pin | | |
| 112 | G/VD | Dedicated Ground Pin | | |
| 113 | R s | Boolean(H/L) H: DATA, L: Instruction code | | |
| 114 | Rw | Boolean(H/L) H: Read (MPU(Module) L: Write (MPU(Module) | | |
| 115 | E | Chip enable signal (Output) | | |

| 116 | шш | Data bit 0 (H/L) | |
|-----|------------|--|--|
| 117 | שם | Data bit 1 (H/L) | |
| 118 | | Data bit 2 (H/L) | |
| 119 | шв | Data bit 3 (H/L) | |
| 120 | | Data bit 4 (H/L) | |
| 121 | | Data bit 5 (H/L) | |
| 122 | TODD? | Data bit 6 (H/L) | |
| 123 | | Data bit 7 (H/L) | |
| 124 | GPI/030 | General purpose input output | |
| 125 | GPI/031 | General purpose input output | |
| 126 | Analog GP | Analog General purpose input output | |
| | 1/03 | | |
| 127 | GND | Dedicated Ground Pin | |
| 128 | LED1 | LED in common cathode controlled by active high | |
| | | output pin | |
| 129 | LED2 | LED in common cathode controlled by active high | |
| 100 | LEDO | output pin | |
| 130 | LED3 | LED in common cathode controlled by active high output pin | |
| 131 | LED4 | LED in common cathode controlled by active high | |
| | | output pin | |
| 132 | ⊞ 5 | LED in common cathode controlled by active high | |
| | | output pin | |
| 133 | Ш6 | LED in common cathode controlled by active high | |
| 134 | 107 | output pin LED in common cathode controlled by active high | |
| 134 | LED7 | output pin | |
| 135 | шВ8 | LED in common cathode controlled by active high | |
| | | output pin | |
| 136 | SWTCH1 | Reads input from active high switch | |
| 137 | SWTCH2 | Reads input from active high switch | |
| 138 | SWTCH3 | Reads input from active high switch | |
| 139 | SWTCH4 | Reads input from active high switch | |
| 140 | SWTCH5 | Reads input from active high switch | |
| 141 | SWTCH6 | Reads input from active high switch | |
| 142 | SWTCH7 | Reads input from active high switch | |
| 143 | SWTCH8 | Reads input from active high switch | |

| 144 RESET Resets the FPGA | | | |
|---------------------------|-----|-------|-----------------|
| | 144 | RESET | Resets the FPGA |

2 DAC



Pin Functions

LTC1666

REFOUT (Pin 15): Internal Reference Voltage Output. Nominal value is 2.5V. Requires a $0.1\mu F$ bypass capacitor to AGND.

 I_{REFIN} (Pin 16): Reference Input Current. Nominal value is 1.25mA for $I_{FS} = 10$ mA. $I_{FS} = I_{REFIN} \cdot 8$.

AGND (Pin 17): Analog Ground.

LADCOM (Pin 18): Attenuator Ladder Common. Normally tied to GND.

 $I_{OUT\,B}$ (Pin 19): Complementary DAC Output Current. Full-scale output current occurs when all data bits are 0s.

I_{OUT A} (Pin 20): DAC Output Current. Full-scale output current occurs when all data bits are 1s.

COMP1 (Pin 21): Current Source Control Amplifier Compensation. Bypass to V_{SS} with $0.1 \mu F$.

COMP2 (Pin 22): Internal Bypass Point. Bypass to V_{SS} with $0.1 \mu F$.

 V_{SS} (Pin 23): Negative Supply Voltage. Nominal value is -5V.

DGND (Pin 24): Digital Ground.

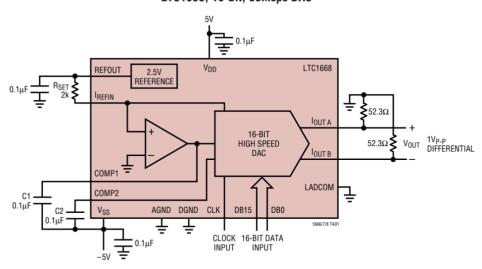
V_{DD} (Pin 25): Positive Supply Voltage. Nominal value is 5V.

CLK (Pin 26): Clock Input. Data is latched and the output is updated on positive edge of clock.

DB11 to DB0 (Pins 27, 28, 1 to 10): Digital Input Data Bits.

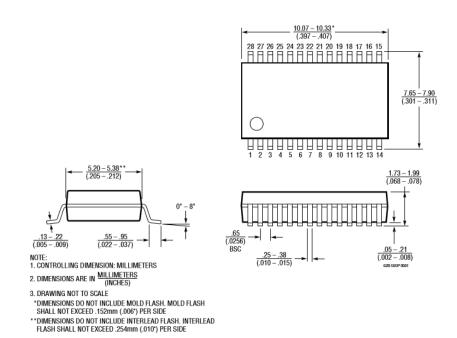
TYPICAL APPLICATION

LTC1668, 16-Bit, 50Msps DAC

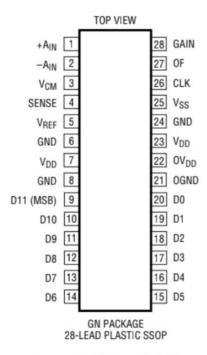


PACKAGE DESCRIPTION

G Package 28-Lead Plastic SSOP (5.3mm) (Reference LTC DWG # 05-08-1640)



3.ADC



 $T_{JMAX} = 125$ °C, $\theta_{JA} = 80$ °C/W

Pin Functions

+AIN (Pin 1): Positive Analog Input.

-AIN (Pin 2): Negative Analog Input.

 V_{CM} (Pin 3): 2.5V Reference Output.Optional input common mode for single supply operation. Bypass to GND with a $1\mu F$ to $10\mu F$ ceramic.

SENSE (Pin 4): Reference Programming Pin. Ground selects V_{REF} = 4.096V. Short to V_{REF} for 2.048V. Connect SENSE to V_{DD} to drive V_{REF} with an external reference.

 V_{REF} (Pin 5): DAC Reference. Bypass to GND with a $1\mu F$ to $10\mu F$ ceramic.

 $\textbf{V}_{\textbf{DD}}$ (Pin 23): Analog 5V Supply. Bypass to GND with a $1\mu F$ ceramic.

GND (Pin 24): Analog Power Ground.

 V_{SS} (Pin 25): Negative Supply. Can be -5V or 0V. If V_{SS} is not shorted to GND, bypass to GND with a $1\mu F$ ceramic.

GND (Pin 6): DAC Reference Ground.

 V_{DD} (Pin 7): Analog 5V Supply. Bypass to GND with a $1\mu F$ to $10\mu F$ ceramic.

GND (Pin 8): Analog Power Ground.

D11 to D0 (Pins 9 to 20): Data Outputs. The output format is two's complement.

OGND (Pin 21): Output Logic Ground. Tie to GND.

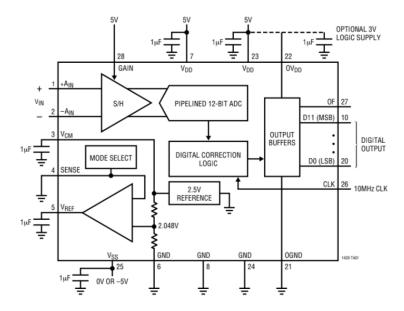
 OV_{DD} (Pin 22): Positive Supply for the Output Logic. Connect to Pin 23 for 5V logic. If not shorted to Pin 23, bypass to GND with a $1\mu F$ ceramic.

CLK (Pin 26): Conversion Start Signal. This active high signal starts a conversion on its rising edge.

OF (Pin 27): Overflow Output. This signal is high when the digital output is 0111111111111 or 1000000000000.

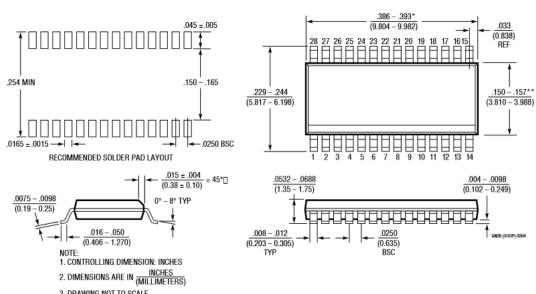
GAIN (Pin 28): Gain Select for Input PGA. 5V selects an input gain of 1, 0V selects a gain of 2.

TYPICAL APPLICATION



PACKAGE DESCRIPTION

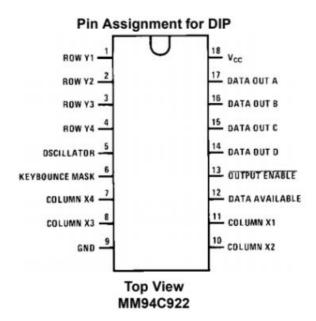
GN Package 28-Lead Plastic SSOP (Narrow 0.150) (LTC DWG # 05-08-1641)



- 3. DRAWING NOT TO SCALE
- *DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
- SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

 **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

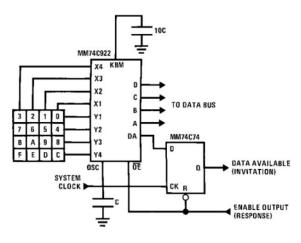
4.Keypad Encoder



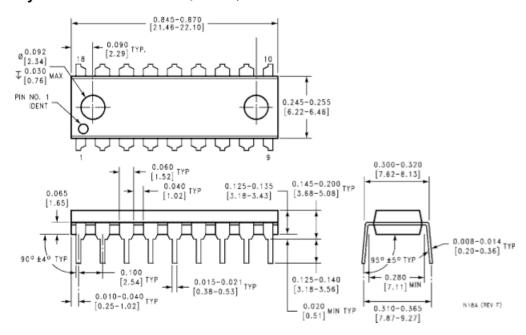
Pin Functions

| DATA out A | Data channel b/w encoder and core ICs | | |
|--|---|--|--|
| DATA out B Data channel b/w encoder and core ICs | | | |
| DATA out C Data channel b/w encoder and core ICs | | | |
| DATA out D | Data channel b/w encoder and core ICs | | |
| Output Enable | Active low, output enabler for keypad encoder | | |
| DATA AVAIL KEY | Active high for no data passing (indicates that | | |
| | input is possible) | | |

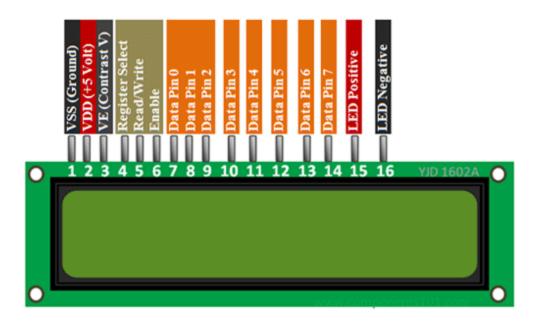
Synchronous Handshake (MM74C922)



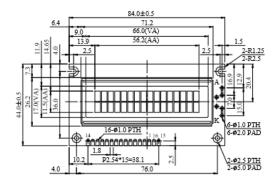
Physical Dimensions inches (millimeters) unless otherwise noted

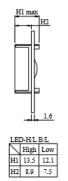


5. <u>LCD</u>

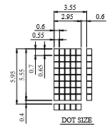


| Pin No. | Symbol | Level | Description | |
|---------|----------|------------|--|--|
| 1 | V_{SS} | 0V | Ground | |
| 2 | V_{DD} | 5.0V | Supply Voltage for logic | |
| 3 | VO | (Variable) | Operating voltage for LCD | |
| 4 | RS | H/L | H: DATA, L: Instruction code | |
| 5 | R/W | H/L | H: Read(MPU→Module) L: Write(MPU→Module) | |
| 6 | Е | H,H→L | Chip enable signal | |
| 7 | DB0 | H/L | Data bit 0 | |
| 8 | DB1 | H/L | Data bit 1 | |
| 9 | DB2 | H/L | Data bit 2 | |
| 10 | DB3 | H/L | Data bit 3 | |
| 11 | DB4 | H/L | Data bit 4 | |
| 12 | DB5 | H/L | Data bit 5 | |
| 13 | DB6 | H/L | Data bit 6 | |
| 14 | DB7 | H/L | Data bit 7 | |
| 15 | A | _ | LED + | |
| 16 | K | _ | LED- | |





| PIN NO. | SYMBOL | | |
|---------|--------|--|--|
| 1 | Vss | | |
| 2 | Vdd | | |
| 3 | Vo | | |
| 4 | RS | | |
| 5 | R/W | | |
| 6 | E | | |
| 7 | DB0 | | |
| 8 | DB1 | | |
| 9 | DB2 | | |
| 10 | DB3 | | |
| 11 | DB4 | | |
| 12 | DB5 | | |
| 13 | DB6 | | |
| 14 | DB7 | | |
| 15 | A/Vee | | |
| 16 | K | | |



The non-specified tolerance of dimension is $\pm 0.3 \mathrm{mm}$.

6.USB (type A and type B)

MCP2221 4 x 4 QFN*

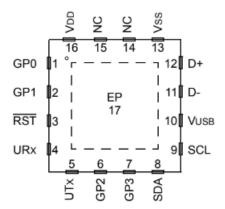
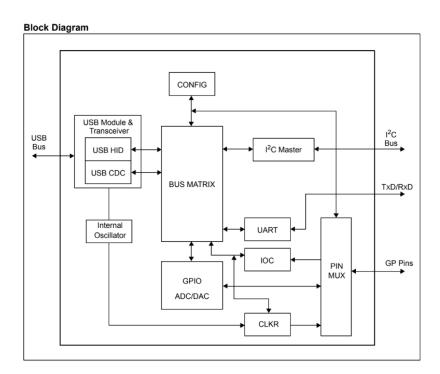
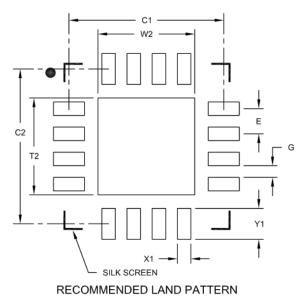


TABLE 1-1: PINOUT DESCRIPTION

| IABLE | 1-11 | PIN | NOUT DESCRIPTION | | | | |
|-------------|------------------------|----------|------------------|---|--|---|--|
| Pin Name | PDIP, SOIC, SSOP | QFN | Pin Type | Standard Function | Al | ternate Functions | |
| GP0 | 2 | 1 | I/O | General-purpose I/O or alternate function pin | SSPND (OUT) LED_URX (OUT) | Signals when the host has entered Suspend mode UART Rx LED activity output (factory default) | |
| GP1 | 3 | 2 | I/O | General-purpose I/O or alternate function pin | CLKR (OUT) ADC1 (IN) LED_UTX (OUT) IOC (IN) | Clock Reference Output ADC Channel 1 UART Tx Led activity output (factory default) External interrupt edge detector | |
| RST | 4 | 3 | - 1 | Reset input (with internal pull-up) | N/A | | |
| URx | 5 | 4 | - 1 | UART Rx pin (input) | N/A | | |
| UTx | 6 | 5 | 0 | UART Tx pin (output) | N/A | | |
| GP2 | 7 | 6 | I/O | General-purpose I/O or alternate function pin | USBCFG (OUT) ADC2 (IN) DAC1 (OUT) | USB device configured status (factory default) ADC Channel 2 DAC Output 1 | |
| GP3 | 8 | 7 | I/O | General-purpose I/O or alternate function pin | LED_I2C (OUT) ADC3 (IN) DAC2 (OUT) | USB-I ² C traffic indicator (factory default) ADC Channel 3 DAC Output 2 | |
| SDA | 9 | 8 | I/O | I ² C Data line | N/A | | |
| SCL | 10 | 9 | I/O | I ² C Clock line | N/A | | |
| Vusb | 11 | 10 | USB | USB Power pin (internally connected to 3.3V) Should be locally bypassed with a high-quality ceramic capacitor | | | |
| D- | 12 | 11 | USB | USB D- | | | |
| D+ | 13 | 12 | USB | USB D+ | | | |
| Vss | 14 | 13 | Р | Ground | | | |
| NC | _ | 14 15 | _ | Not Connected | | | |
| VDD | 1 | 16 | Р | Power | | | |
| EP | _ | 17 | _ | Exposed Thermal Pad (EP) Do not electrically connect. | | | |

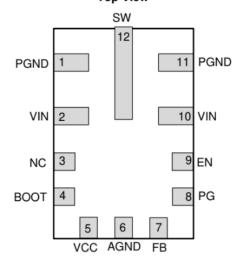




| | Units | N | IILLIMETER | S |
|----------------------------|--------|------|-------------------|------|
| Dimension | Limits | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | W2 | | | 2.50 |
| Optional Center Pad Length | T2 | | | 2.50 |
| Contact Pad Spacing | C1 | | 4.00 | |
| Contact Pad Spacing | C2 | | 4.00 | |
| Contact Pad Width (X16) | X1 | | | 0.35 |
| Contact Pad Length (X16) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.30 | | |

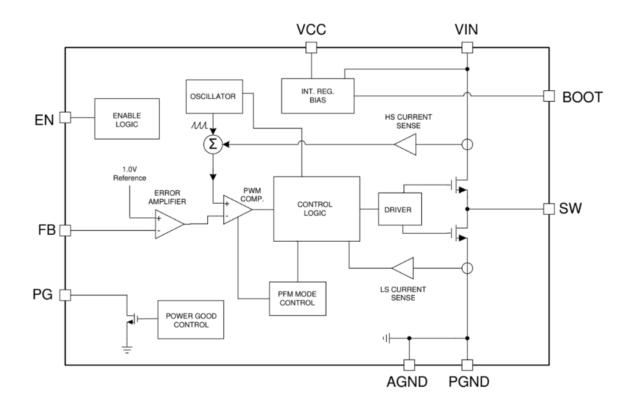
7.Power Supply a.12V to 5V

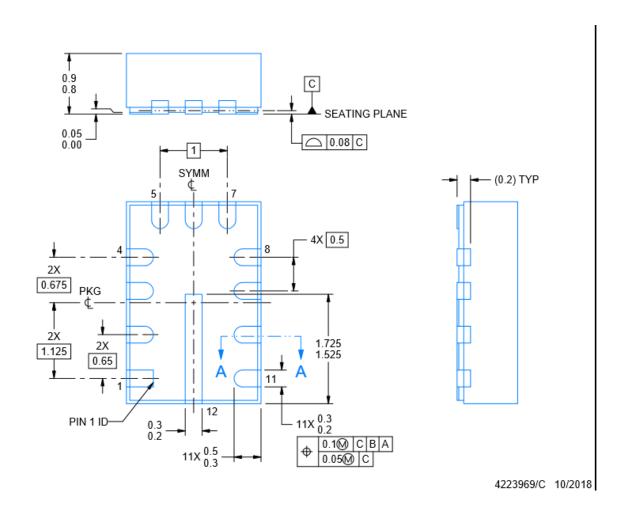
RNX Package 12-Pin VQFN-HR Top View



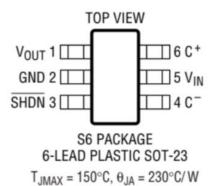
Pin Functions

| NO. | NAME | TYPE | DESCRIPTION |
|----------|---------------|------------|--|
| 1, 11 | PGND | G | Power ground terminal. Connect to system ground and AGND. Connect to C _{IN} with short wide traces. |
| 2, 10 | VIN | Р | Input supply to regulator. Connect to C _{IN} with short wide traces. |
| 3 | NC | _ | Connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin. This pin has no internal connection to the regulator. |
| 4 | воот | Р | Boot-strap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. Connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin. |
| 5 | VCC | Р | Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND. |
| 6 | AGND | G | Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB. |
| 7 | FB | Α | Feedback input to regulator. Connect to tap point of feedback voltage divider. DO NOT FLOAT. DO NOT GROUND. |
| 8 | PG | А | Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Goes low when EN = Low. Can be open or grounded when not used. |
| 9 | EN | Α | Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; DO NOT FLOAT. |
| 12 | SW | Р | Regulator switch node. Connect to power inductor. Connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin. |
| A = Anal | og, P = Power | , G = Grou | nd |





b.5Vto 3.3V



PIN FUNCTIONS

 V_{OUT} (Pin 1): Regulated Output Voltage. For best performance, V_{OUT} should be bypassed with a $6.8\mu F$ (min) low ESR capacitor as close as possible to the pin.

GND (Pin 2): Ground. Should be tied to a ground plane for best performance.

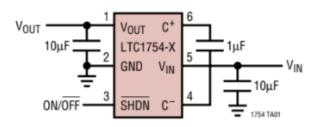
SHDN (Pin 3): Active Low Shutdown Input. A low on SHDN disables the LTC1754. SHDN must not be allowed to float.

C- (Pin 4): Flying Capacitor Negative Terminal.

 V_{IN} (Pin 5): Input Supply Voltage. V_{IN} should be bypassed with a $6.8\mu F$ (min) low ESR capacitor.

C+ (Pin 6): Flying Capacitor Positive Terminal.

TYPICAL APPLICATION

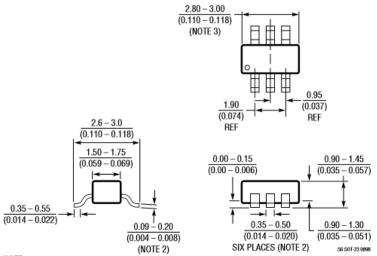


Regulated 3.3V Output from 2V to 4.4V Input

$$\begin{split} &V_{OUT}=3.3V\pm4\%\\ &I_{OUT}=0\text{mA TO }20\text{mA, }V_{IN}>2.0V\\ &I_{OUT}=0\text{mA TO }40\text{mA, }V_{IN}>2.5V \end{split}$$

PACKAGE DESCRIPTION Dimensions in inches (millimeters), unless otherwise noted.

S6 Package 6-Lead Plastic SOT-23 (LTC DWG # 05-08-1634)



NOTE:

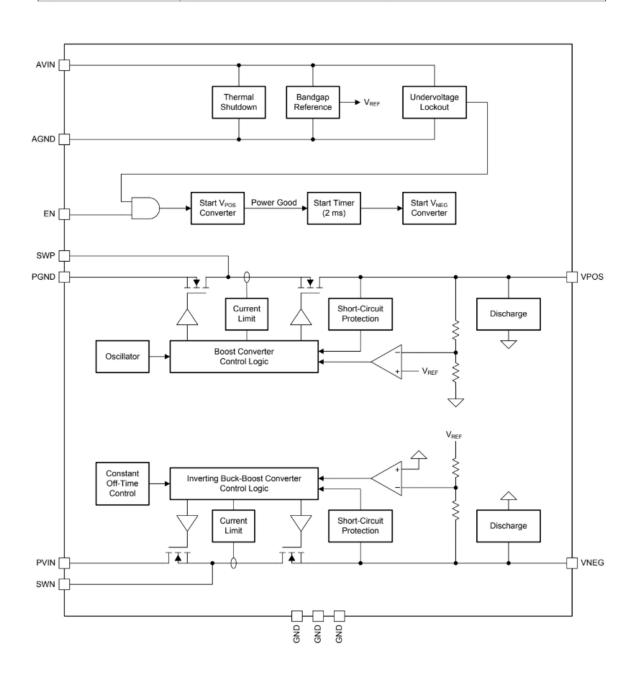
- NOTE:
 1. DIMENSIONS ARE IN MILLIMETERS
 2. DIMENSIONS ARE INCLUSIVE OF PLATING
 3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
 4. MOLD FLASH SHALL NOT EXCEED 0.254mm
 5. PACKAGE EIAJ REFERENCE IS SC-74A (EIAJ)

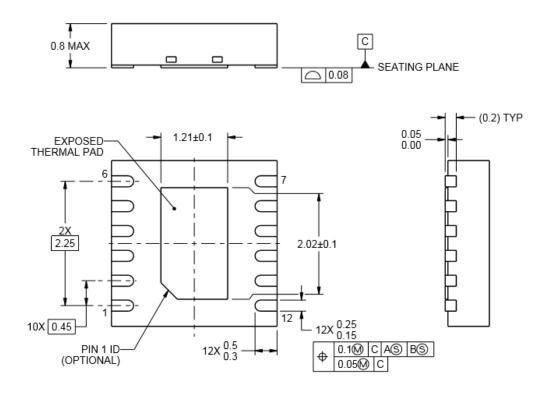
c.5Vto-5V

DPD Package 12-Pin WSON (Top View) (12 PVIN **PGND** _2) AVIN (11_ VPOS _3) (10 SWN Exposed Thermal GND <u>4</u>) Pad $(\bar{9})$ VNEG 5) AGND (8 GND GND <u>_</u>6_) ΕN

Pin Functions

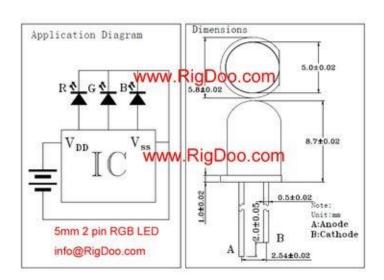
| PI | N | DESCRIPTION |
|-----------------|---------|---|
| NAME | NO. | DESCRIPTION |
| AGND | 5 | Analog ground |
| AVIN | 11 | Internal logic supply pin |
| EN | 7 | Enable of boost and buck-boost converter |
| GND | 4, 6, 8 | Ground |
| SWP | 1 | Switch pin of the boost converter |
| PGND | 2 | Power ground of the boost converter |
| PVIN | 12 | Supply pin for the negative buck-boost converter. Place a capacitor close to this pin. |
| SWN | 10 | Switch pin of the negative buck-boost converter |
| VNEG | 9 | Output of the negative buck-boost converter (V _{NEG}), place a capacitor close to this pin. |
| VPOS | 3 | Output of the boost converter (V _{POS}), place a capacitor close to this pin. |
| Exposed thermal | pad | Exposed thermal pad. Connect this pad to all GND pins. |





8. LEDs and Switches

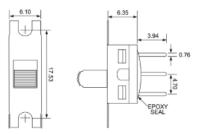
аШ

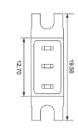


b.Switch



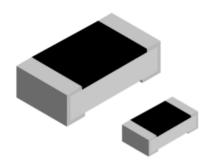
| | Tog | gle Posi | tion |
|-----------|-----|----------|------|
| Function | _ | 4 | _ |
| 1 | ON | NONE | ON |
| 2 | ON | NONE | (ON) |
| 3 | ON | OFF | ON |
| Terminals | 2-3 | n/a | 2-1 |





9.Mscellaneus

1. Resistors



| DESCRIPTION | RCS0402 e3 |
|--|------------|
| Imperial size | 0402 |
| Metric size code | RR1005M |
| Resistance range | |
| Resistance tolerance | |
| Temperature coefficient | |
| Rated dissipation, P ₇₀ (1) | 0.2 W |
| Operating voltage, U _{max.} AC _{RMS} /DC | 50 V |
| Permissible film temperature, $\mathcal{P}_{F \text{ max.}}^{(1)}$ | |
| Operating temperature range | |
| Max. resistance change at P_{70} for resistance range, $ \Delta R/R $ after: | |
| 1000 h | 1 |
| 8000 h | ı |
| Permissible voltage against ambient (insulation): | |
| 1 min, U _{ins} | 75 V |

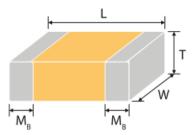
SOLDER PAD DIMENSIONS



| RECOMMEND | ED SOLDE | R PAD DIN | IENSIONS | | | | | |
|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| | | WAVE SO | LDERING | | | REFLOW S | OLDERING | |
| TYPE / SIZE | G (mm) | Y (mm) | X (mm) | Z (mm) | G (mm) | Y (mm) | X (mm) | Z (mm) |
| RCS0402 e3 | - | - | - | - | 0.45 | 0.6 | 0.6 | 1.65 |
| RCS0603 e3 | 0.65 | 1.10 | 1.25 | 2.85 | 0.75 | 0.75 | 1.00 | 2.15 |
| RCS0805 e3 | 0.90 | 1.30 | 1.60 | 3.50 | 1.00 | 0.95 | 1.45 | 2.90 |
| RCS1206 e3 | 1.40 | 1.40 | 1.95 | 4.20 | 1.50 | 1.05 | 1.80 | 3.60 |

2 Capacitors

External Dimensions:



The outline of MLCC

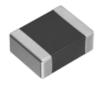
General Electrical Data:

| Dielectric | NP0 | X7R | Y5V | |
|-------------------------|---|--------------------------------|------------------------|--|
| Size | 0402, 0603, 0 | 805, 1206, 1210, 1812 | | |
| Capacitance* | 0.5pF to 0.1µF | 100pF to 0.82μF | 10nF to 0.68μF | |
| Capacitance tolerance** | Cap≤5pF: B (±0.1pF), C (±0.25pF) 5pF <cap<10pf: (±0.25pf),="" (±0.5pf)="" (±1%),="" (±10%)<="" (±2%),="" (±5%),="" c="" cap≥10pf:="" d="" f="" g="" j="" k="" th=""><th>J (±5%), K (±10%), M (±20%)</th><th>M (±20%), Z (-20/+80%)</th></cap<10pf:> | J (±5%), K (±10%), M (±20%) | M (±20%), Z (-20/+80%) | |
| Rated voltage (WVDC) | 10V, 16V, 25V, 50V, 100V | 6.3V, 10V, 16V, | 25V, 50V, 100V | |
| DF (Tan δ)* | Cap<30pF: Q≥400+20C Cap≥30pF: Q≥1000 | No | te 1 | |
| Operating temperature | -55°C to +125°C | | -55°C to +85°C | |
| Capacitance change | ±30ppm | ±1 | 5% | |
| Termination | Ni/Sn (lea | d-free termination) | | |

| Size Inch (mm) | L (mm) | W (mm) | T (mm)/Syml | bol | Remark | MB (mm) |
|-------------------|-------------------|-------------------|-------------------|-----|--------|--------------------|
| 0402 (1005) | 1 ±0.05 | 0.5 ±0.05 | 0.5 ±0.05 | N | # | 0.25 +0.05/-0.1 |
| | 1.6 ±0.1 | 0.8 ±0.1 | 0.8 ±0.07 | S | - | |
| 0603 (1608) | 1.6 +0.15/-0.1 | 0.8 +0.15/-0.1 | 0.8 +0.15/-0.1 | х | - | 0.4 ±0.15 |
| | | | 0.6 ±0.1 | Α | - | |
| 0005 (2012) | 2 ±0.15 | 1.25 ±0.1 | 0.8 ±0.1 | В | - | 0.5 ±0.2 |
| 0805 (2012) | | | 1.25 ±0.1 | D | # | 0.5 ±0.2 |
| | 2 ±0.2 | 1.25 ±0.2 | 1.25 ±0.2 | Ι | # | |
| | | | 0.8 ±0.1 | В | - | |
| | | | 0.95 ±0.1 | С | - | |
| | 3.2 ±0.15 | 1.6 ±0.15 | 1.15 ±0.15 | J | # | |
| 1206 (3216) | | | 1.25 ±0.1 | D | # | 0.6 ±0.2 |
| | | | 1.6 ±0.2 | G | # | |
| | 3.2 +0.3/-0.1 | 1.6 +0.3/0.1 | 1.6 +0.3/-0.1 | Р | # | |
| | 3.2 ±0.3 | 2.5 ±0.2 | 0.95 ±0.1 | С | # | |
| | 3.2 ±0.3 | 2.0 ±0.2 | 1.25 ±0.1 | D | # | |
| 1210 (3225) | | | 1.6 ±0.2 | G | # | 0.75 ±0.25 |
| | 3.2 ±0.4 | 2.5 ±0.3 | 2 ±0.2 | К | # | |
| | | | 2.5 ±0.3 | М | # | |
| 1812 (4532) | 4.5 ±0.4 | 3.2 ±0.3 | 1.25 ±0.1 | D | # | 0.75 ±0.25 |
| 1012 (4032) | 4.0 ±0.4 | 3.2 ±0.3 | 2 ±0.2 | К | # | U.10 ±U.20 |

3. Inductors

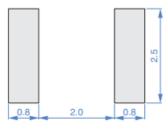
TFM322512ALMA



■ CHARACTERISTICS SPECIFICATION TABLE

| L | | L measuring frequency | DC resistar | ice | Rated cu | rrent* | | | Rated voltage | Part No. |
|------|-----------|-----------------------|------------------|-------------------|----------|---------|---------|---------|---------------|----------------------|
| | | | | | Isat | | Itemp | | | |
| (µH) | Tolerance | (MHz) | $(m\Omega)$ max. | (m Ω)typ. | (A)max. | (A)typ. | (A)max. | (A)typ. | (V)max. | |
| 1.0 | ±20% | 1 | 37 | 30 | 4.6 | 5.1 | 4.0 | 4.4 | 20 | TFM322512ALMA1R0MTAA |
| 1.5 | ±20% | 1 | 57 | 46 | 4.0 | 4.5 | 3.2 | 3.5 | 20 | TFM322512ALMA1R5MTAA |
| 2.2 | ±20% | 1 | 77 | 64 | 3.3 | 3.6 | 2.7 | 3.0 | 20 | TFM322512ALMA2R2MTAA |
| 3.3 | ±20% | 1 | 113 | 97 | 2.5 | 2.8 | 2.3 | 2.5 | 20 | TFM322512ALMA3R3MTAA |
| 4.7 | ±20% | 1 | 151 | 127 | 2.2 | 2.5 | 1.9 | 2.1 | 20 | TFM322512ALMA4R7MTAA |
| 6.8 | ±20% | 1 | 260 | 220 | 1.8 | 2.1 | 1.4 | 1.6 | 20 | TFM322512ALMA6R8MTAA |
| 10 | ±20% | 1 | 360 | 305 | 1.6 | 1.8 | 1.2 | 1.4 | 20 | TFM322512ALMA100MTAA |

■ RECOMMENDED LAND PATTERN



Dimensions in mm

4. Keypad(switches)

TACT SWITCHES RADIAL LEAD



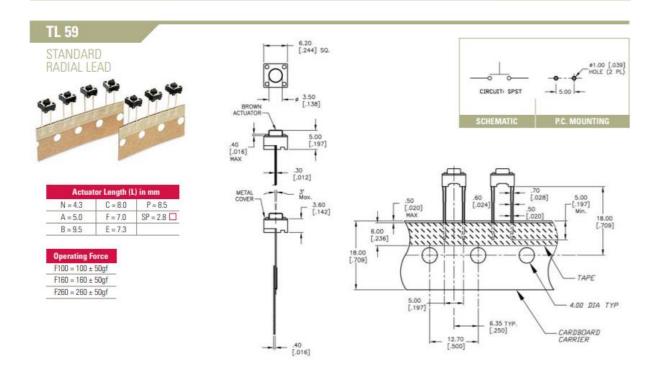
| Contact Rating: | 50mA @ 12 VDC |
|------------------------|--|
| Life Expectancy: | 100,000 cycles |
| Contact Resistance: | 100mΩ max., typical @ 2-4 VDC 100mA for both silver plated contacts |
| Insulation Resistance: | 100MΩ min. |
| Dielectric Strength: | 250 VAC |
| Actuation Force: | 100 ± 50 gf, 160 ± 50 gf, 260 ± 50 gf |
| Operating Temperature: | -20°C to 70°C |
| Travel: | 0.25 Typ |

FEATURES & BENEFITS

- Designed for automatic feed
 Radial lead packaging

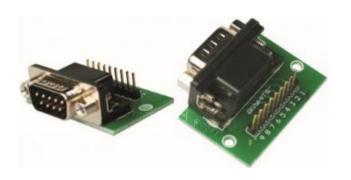
APPLICATIONS/MARKETS

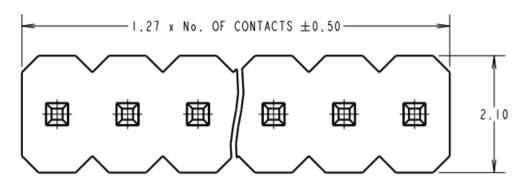
- ► Telecommunications
- ► Consumer Electronics
- ► Audio/visual
- ► Testing/instrumentation
- ► Computer/servers/peripherals

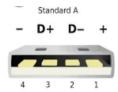












7. Usb part B



8. Power supply port

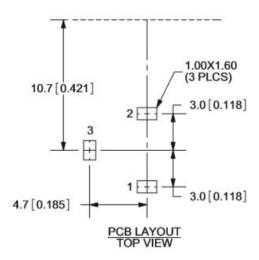
MODEL: PJ-102A | DESCRIPTION: DC POWER JACK

FEATURES

- 2.0 mm center pin
- 2.5 A rating right-angle orientation
- through hole
- tapered pins

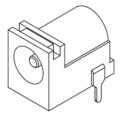






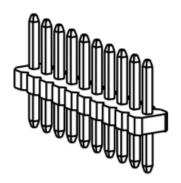
MECHANICAL DRAWING

units: mm[inches] tolerance: X.X ±0.2mm X.XX ±0.1mm X.XXX ±0.05mm



| MATERIAL | PLATING |
|--------------|--|
| copper | nickel |
| brass | tin |
| copper alloy | tin |
| brass | tin |
| PBT | |
| | copper brass copper alloy brass |

9. Berg Connector



SPECIFICATION: MATERIAL: MOULDING = PA9T, UL94V-0, BLACK CONTACT = BRASS FINISH = 0.76-1.52 µ NICKEL ALL OVER, 0.012 µ MIN GOLD ON CONTACT AREA, 2.54-5.08 µ 100% TIN ON TAILS ELECTRICAL: CURRENT RATING = IA CONTACT RESISTANCE = $20m\Omega$ MAX INSULATION RESISTANCE = 1000M Ω MAX VOLTAGE PROOF = 500V AC FOR ONE MINUTE MECHANICAL: DURABILITY = 500 CYCLES ENVIRONMENTAL: OPERATING TEMPERATURE = -40°C TO +105°C PACKING: BOX FOR COMPLETE SPECIFICATION, SEE COMPONENT SPECIFICATION CO29XX (LATEST ISSUE)

