General Description

Silego SLG4B41337 is a low power and small form device. The SoC is housed in a 1.6 x 2.5 mm STQFN package which is optimal for using with small devices.
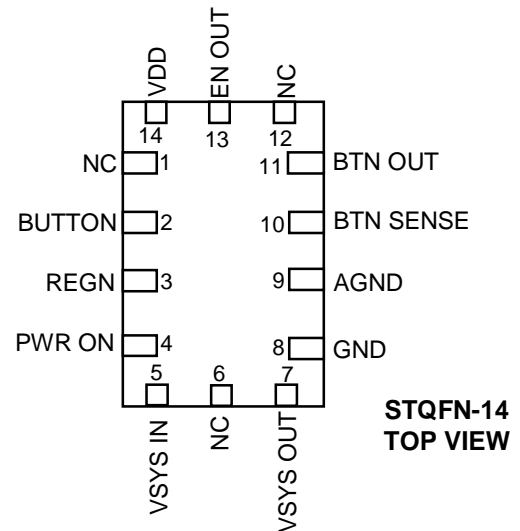
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
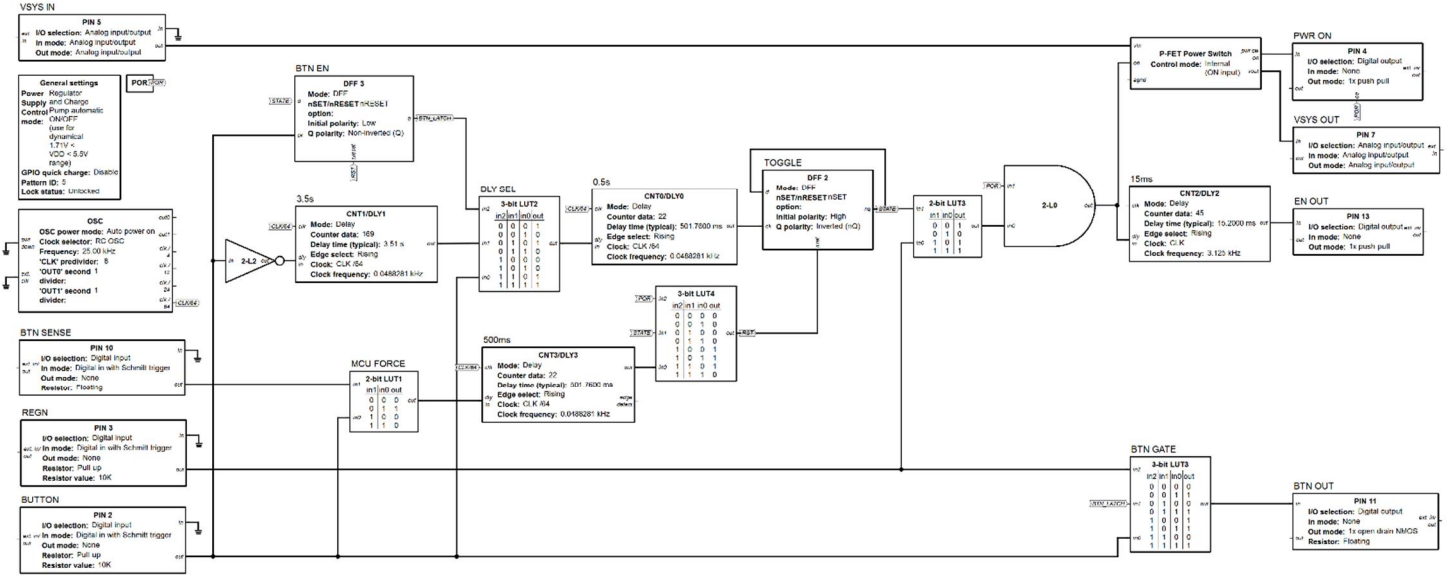- Halogen-Free
- STQFN-14 Package

Output Summary

- 2 Outputs — Push Pull 1X
- 1 Output — Open Drain NMOS 1X

Pin Configuration

Pin	Signal
14	VDD
13	EN OUT
12	NC
1	NC
2	BUTTON
3	REGN
4	PWR ON
5	VSYS IN
6	NC
7	VSYS OUT
8	GND
9	AGND
10	BTN SENSE
11	BTN OUT

STQFN-14 TOP VIEW

Block Diagram

Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	NC	--	Keep Floating or Connect to GND
2	BUTTON	Digital Input	Digital Input with Schmitt trigger
3	REGN	Digital Input	Digital Input with Schmitt trigger
4	PWR ON	Digital Output	Push Pull 1X
5	VSYS IN	P-FET Power Switch Input	P-FET Power Switch Input
6	NC	--	Keep Floating or Connect to GND
7	VSYS OUT	P-FET Power Switch Output	P-FET Power Switch Output
8	GND	GND	Ground
9	AGND	AGND	Ground
10	BTN SENSE	Digital Input	Digital Input with Schmitt trigger
11	BTN OUT	Digital Output	Open Drain NMOS 1X
12	NC	--	Keep Floating or Connect to GND
13	EN OUT	Digital Output	Push Pull 1X
14	VDD	PWR	Supply Voltage

Ordering Information

Part Number	Package Type
SLG4B41337V	V=STQFN-14L
SLG4B41337VTR	STQFN-14L – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Condition	Min.	Max.	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at input pins		-0.3	7	V
Current at input pin		-1.0	1.0	mA
Storage temperature range		-65	125	°C
Junction temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		
P-FET Power Switch IDS_{PK}	For no more than 1 ms with 1% duty cycle	--	1.5	A

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.3	3.3	4.35	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input with Schmitt Trigger, at VDD=3.3V	2.13	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Logic Input with Schmitt Trigger, at VDD=3.3V	--	--	0.95	V
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage (note 1)	Push Pull & PMOS OD, I_{OH} = 3mA, 1X Driver, at VDD=3.3 V	2.71	3.09	--	V
V_{OL}	LOW-Level Output Voltage (note 1)	Push Pull, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.15	0.28	V
		Open Drain, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.080	0.147	
I_{OH}	HIGH-Level Output Current (note 1)	Push Pull & PMOS OD, V_{OH} = 2.4 V, 1X Driver, at VDD=3.3 V	6.01	12.07	--	mA
I_{OL}	LOW-Level Output Current (note 1)	Push Pull, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	4.06	6.92	--	mA
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	7.313	12.37	--	
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 2, 3	7	10	13	kΩ
T_{DLY0}	Delay0 Time	At temperature 25°C	456.75	501.76	534.79	ms
		At temperature -40°C +85°C (note 1)	412.66	501.76	633.16	
T_{DLY1}	Delay1 Time	At temperature 25°C	3.24	3.51	3.69	s
		At temperature -40°C +85°C (note 1)	2.93	3.51	4.37	

			Min	Typ	Max	
T_{DLY2}	Delay2 Time	At temperature 25°C	13.97	15.2	16.05	ms
		At temperature -40°C +85°C (note 1)	12.62	15.2	19	
T_{DLY3}	Delay3 Time	At temperature 25°C	456.75	501.76	534.79	ms
		At temperature -40°C +85°C (note 1)	412.66	501.76	633.16	
V_{IN}	Power Switch Input Voltage	-40 °C to 85 °C	1.5	--	5.0	V
I_{IN}	Power Switch Current (PIN 5)	when Off, V_{IN} = 5.0 V	--	0.02	0.1	µA
		when PWR_SW_ON = V_{IN}, No load	--	0.02	0.1	
I_{DS_LKG}	Leakage Measured from PIN 5 to PIN 7	when Off, V_{IN} = 5.0 V	--	0.05	1	µA
I_{ON_LKG}	PWR_SW_ON Pin Input Leakage		--	--	0.1	µA
RDS_{ON}	Static Drain to Source ON Resistance @ T_A 25°C	@ V_{IN} = 5.5 V	--	28.5	32.0	mΩ
		@ V_{IN} = 3.3 V	--	36.4	40.0	
		@ V_{IN} = 2.5 V	--	44.3	49.0	
		@ V_{IN} = 1.8 V	--	60.8	65.0	
		@ V_{IN} = 1.5 V	--	77.6	82.0	
RDS_{ON}	Static Drain to Source ON Resistance @ T_A 85°C	@ V_{IN} = 5.5 V	--	34.0	36.0	mΩ
		@ V_{IN} = 3.3 V	--	43.8	46.0	
		@ V_{IN} = 2.5 V	--	53.3	56.0	
		@ V_{IN} = 1.8 V	--	72.2	76.0	
		@ V_{IN} = 1.5 V	--	90.7	94.0	
I_{DS}	Operating Current	V_{IN} = 1.5 V to 5.0 V	--	--	1.0	A
T_{On_Delay}	PWR_SW_ON pin Delay Time	50% PWR_SW_ON to Ramp Begin, V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	12.0	15.0	18.5	µs
		50% PWR_SW_ON to Ramp Begin, V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	17.0	22.0	30.0	
		50% PWR_SW_ON to Ramp Begin, V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	44.0	55.0	76.0	
T_{Total_On}	Total Turn On Time	50% PWR_SW_ON to 90% VOUT, V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	114	122	134	µs
		50% PWR_SW_ON to 90% VOUT, V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	146	156	176	
		50% PWR_SW_ON to 90% VOUT, V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	292	332	399	
T_{RISE}	Rise Time	10% VOUT to 90% VOUT, V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	92	97	107	µs
		10% VOUT to 90% VOUT, V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	116	120	131	
		10% VOUT to 90% VOUT, V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	228	253	296	
PWR_SW _ON_V_{IH}	Initial Turn On Voltage		0.85	--	VIN or VDD	V

PWR_SW _ON_V_{IL}	Low Input Voltage on PWR_SW_ON pin		-0.3	0	0.3	V
T_{Delay_Off}	Off Delay Time	50% PWR_SW_ON to VOUT Fall, V_{IN} = 5 V, R_L =10 Ω	6.2	6.5	7.0	µs
T_{SU}	Start up Time	From VDD rising past 1.35V	--	0.27	--	ms
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.182	1.346	1.505	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.752	0.918	1.110	V

1. Guaranteed by Design.

Functionality Waveforms

Channel 1 (yellow/top line) – PIN#5 (VSYS IN)
D0 – PIN#2 (BUTTON)
D1 – PIN#3 (REGN)
D2 – PIN#10 (BTN SENSE)
Channel 2 (light blue) – PIN#7 (VSYS OUT) with external 5kΩ pull down resistor
D3 – PIN#4 (PWR ON)
D4 – PIN#13 (EN OUT)
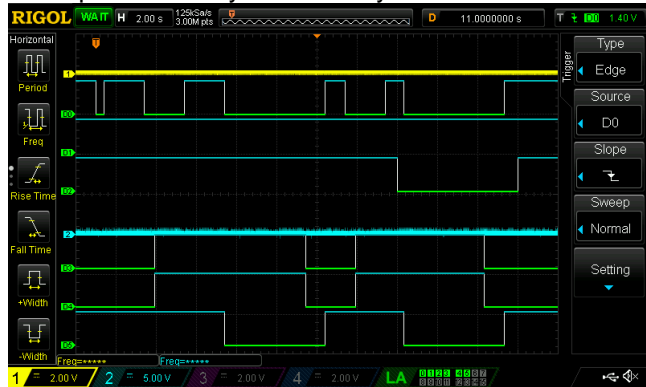D5 – PIN#11 (BTN OUT) with external 5kΩ pull up resistor
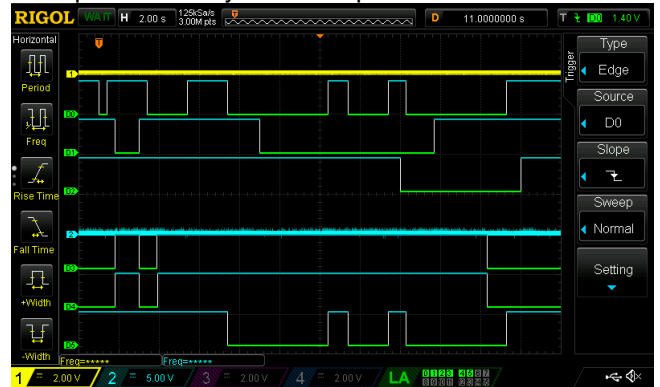
1. Chip functionality: REGN only in HIGH
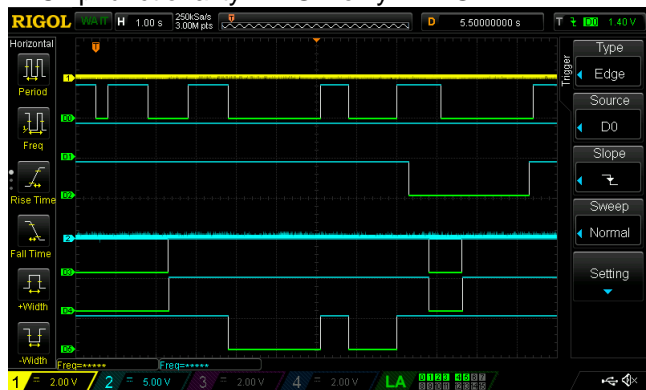
2. Chip functionality: normal operation
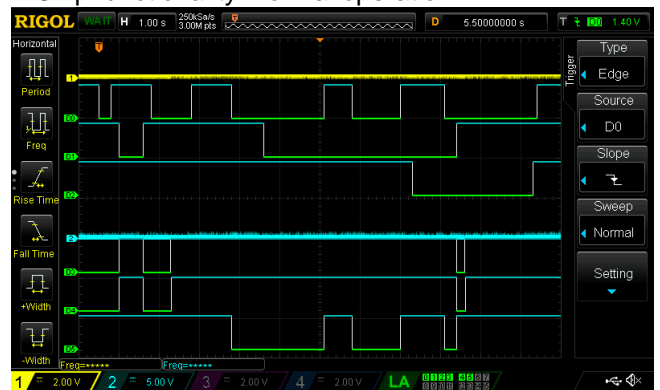
3. Chip functionality: REGN only in HIGH

4. Chip functionality: normal operation

Channel 1 (yellow/top line) – PIN#5 (VSYS IN)
D0 – PIN#2 (BUTTON)
D1 – PIN#3 (REGN)
D2 – PIN#10 (BTN SENSE)
Channel 2 (light blue) – PIN#7 (VSYS OUT) with external 5kΩ pull down resistor
D3 – PIN#4 (PWR ON)
D4 – PIN#13 (EN OUT)
D5 – PIN#11 (BTN OUT) with external 5kΩ pull up resistor

5. Chip functionality: shape delay time for EN OUT
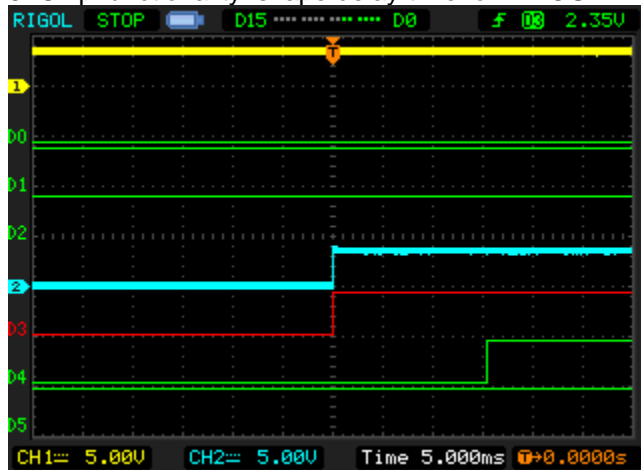
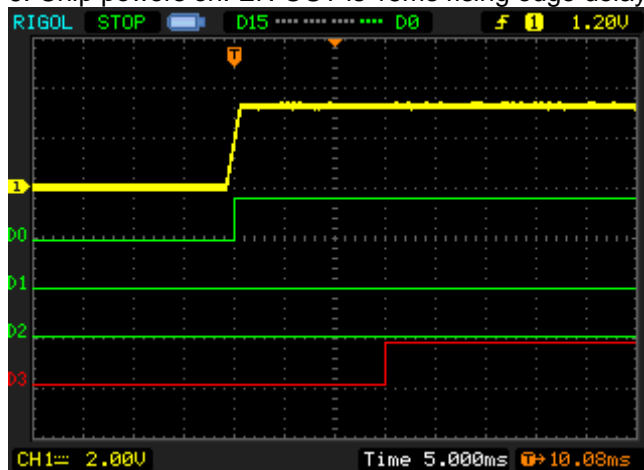Channel 1 (yellow/top line) – PIN#14 (VDD)
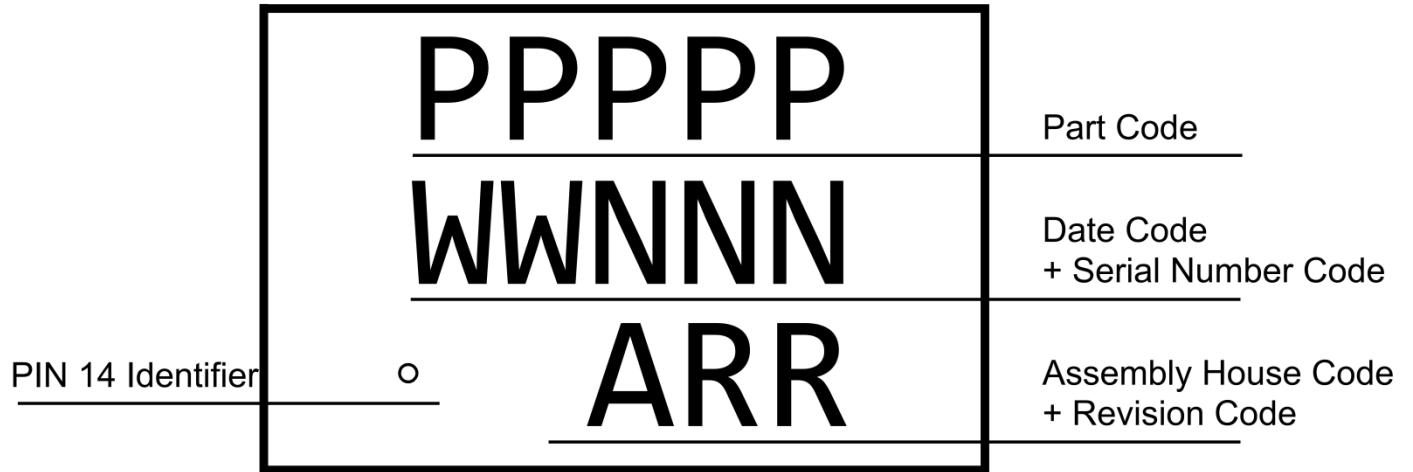D0 – POR
D1 – DFF2 Output
D2 – PIN#3 (REGN)
D3 – PIN#13 (EN OUT)

6. Chip powers on: EN OUT is 15ms rising edge delayed

SILEGO

**Package Top Marking**

```
PPPPP        Part Code
WWNNN        Date Code
             + Serial Number Code
ARR          Assembly House Code
             + Revision Code
```

PIN 14 Identifier   o

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.00	005	L	41337	AB	10/20/2016

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

14 Lead STQFN Package 1.6 x 2.5 mm
JEDEC MO-252
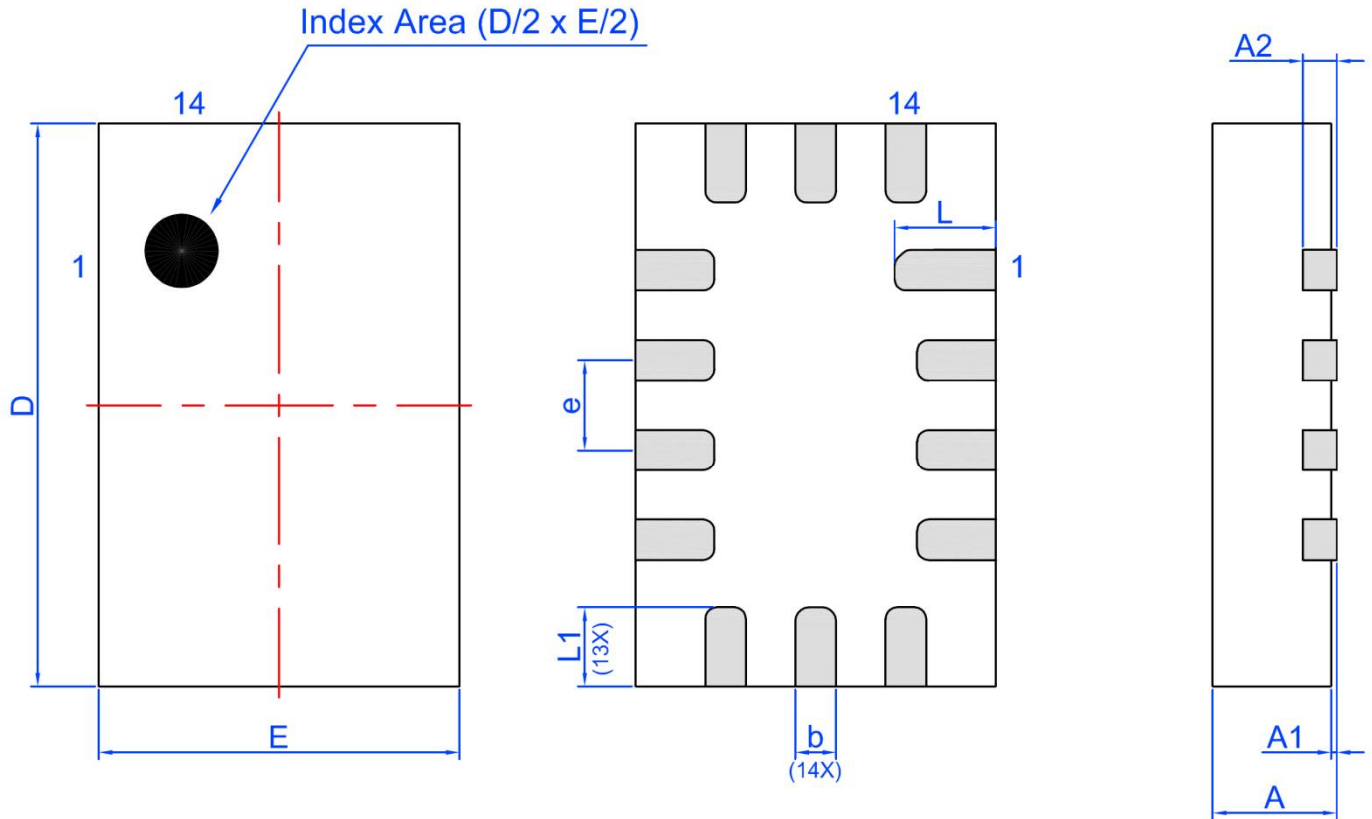
Unit: mm

| Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.45	2.50	2.55
A1	0.005	-	0.050	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.40	0.45	0.50
b	0.13	0.18	0.23	L1	0.30	0.35	0.40
e	0.40 BSC						

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 14L 1.6x2.5 mm FC 0.4P Green	14	1.6x2.5x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6x2.5 mm FC 0.4P Green	1.8	2.8	0.7	4	4	1.55	1.75	3.5	8

Refer to EIA-481 Specifications
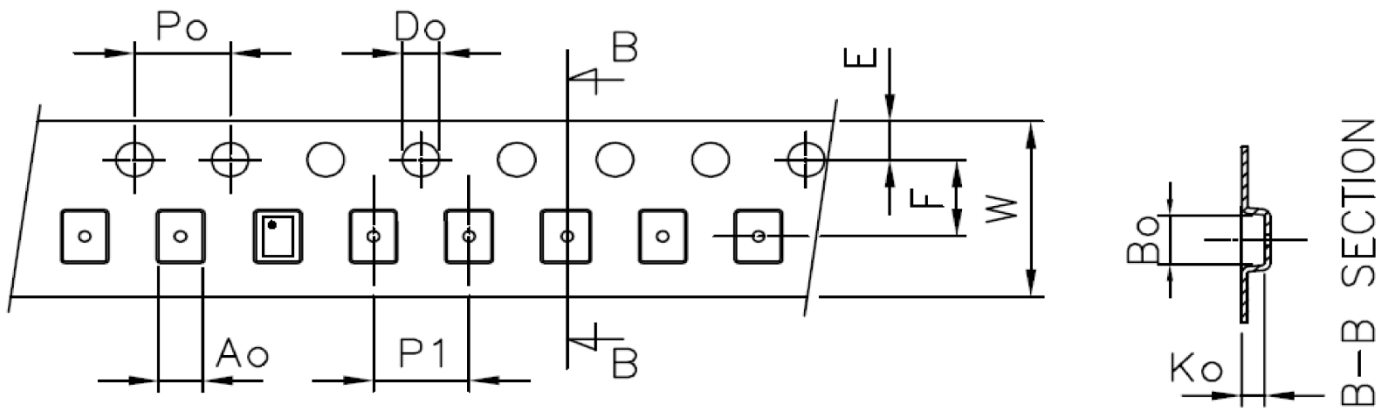
Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm^3 (nominal). More information can be found at www.jedec.org.

Datasheet Revision History

Date	Version	Change
07/12/2016	0.10	New design for SLG46116 chip
07/21/2016	0.11	Updated design operation and Functionality Waveforms
07/25/2016	0.12	Updated the time in DLY1 from 1.5 seconds to 3.5 seconds and Functionality Waveforms
07/25/2016	0.13	Updated Device Revision Table
08/10/2016	0.14	Updated design operation and added Functionality Waveform
08/11/1016	0.15	Updated Electrical Characteristics Table
08/16/2016	0.16	Updated block diagram, retook Waveforms 1 through 4
08/16/2016	0.17	Updated Device Revision Table
10/17/2016	0.18	Updated Lock Status
10/20/2016	1.00	Production Release

Silego Website & Support

Silego Technology Website

Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit our website.

Our Green product lines feature:

GreenPAK1 / GreenPAK2 / GreenPAK3/ GreenPAK 4 / GreenPAK 5: Programmable Mixed Signal Matrix products
GreenFET1 / GreenFET3: MOSFET Drivers and ultra-small, low RDSon Load Switches
GreenCLK1 / GreenCLK2 / GreenCLK3: Crystal replacement technology

Products are also available for purchase directly from Silego at the Silego Online Store at http://www.silego.com/buy/ .

Silego Technical Support

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send e-mail requests to GreenPAK@silego.com

Users of Silego products can receive assistance through several channels:

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Silego can be contacted directly via e-mail at info@silego.com or user submission form, located at the following URL: http://support.silego.com/

Other Information

The latest Silego Technology press releases, listing of seminars and events, listings of world wide Silego Technology offices and representatives are all available at http://www.silego.com/

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