CUSTOMER PRODUCT SPECIFICATION (CPS)

Holographic Display Panel

Model: HDP-1280-2

Revision B

Displaytech, Inc.

2602 Clover Basin Drive

Longmont, Colorado 80503-7604 USA

303-772-2191

303-772-2193 fax

www.displaytech.com

DisplayTECH®

Table of Contents

List of Tables

List of Figures

Introduction

This specification provides a detailed technical description of the Displaytech Holographic Display Panel (HDP), Model HDP-1280-2 and offers the basic information needed to integrate and control the HDP. The document is divided into six primary sections: summary, HDP overview, system and optical specification, mechanical specification, electrical specification, and mechanical stress/reliability. Additional information is provided in the Appendices, including general device handling instructions, a summary of the registers, and the environmental compliance list.

Summary

The Displaytech HDP-1280-2 is a high speed, low power Holographic Display Panel intended for use in holographic imaging systems. This product takes advantage of the fast switching speeds and superior optical qualities of Displaytech's patented Ferroelectric Liquid Crystal (FLC) materials.

The HDP-1280-2 is designed to be environmentally friendly. Appendix C lists certain hazardous substances and the maximum levels allowed.

Table 1 summarizes the key parameters that describe the HDP-1280-2. In the sections following, details behind each of the parameters will be provided as well as additional information on the proper application and control of the device.

Table 1: Nominal Specifications for HDP-1280-2

Parameter	Specification
HDP technology	Ferroelectric Liquid Crystal (FLC) on reflective CMOS
HDP mode	Binary
HDP data format	1280 (H) x 1280 (V)
HDP optical format	1280 (H) x 1280 (V)
HDP optical active area/cover opening	7.27mm x 7.27 mm
HDP pixelated apron	205.4 µm (on all 4 sides of active area)
HDP optical diagonal	10.28 mm
HDP pixel pitch	5.68(H) x 5.68(V) µm
Pixel fill factor	88.1%
Frame rate	≤ 2.4 kHz*
Data clock rate (Max)	140 MHz
Data interface	32 Data bits with Valid
Control interface	4 wire serial
Operating supply voltages	2.5 V, 5.25 V (nominal)
Power consumption	200mW
Dimensions (L x W x H)	24.8 × 11.3 × 4.7 mm
Weight	2 grams
Operating temperature	-10 °C to 70 °C (panel temperature)
Storage temperature	-30 °C to 83 °C

*** Valid under the conditions outlined in this document.**

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

HDP Overview

The HDP-1280-2 provides a compact solution for displaying an array of binary data. The main component of the HDP-1280-2 is the low power Ferroelectric Liquid Crystal (FLC) reflective microdisplay panel. The HDP panel assembly consists of a reflective silicon backplane, a layer of ferroelectric liquid crystal, and a glass cover. The electronic binary data is fed to the silicon backplane controlling the voltage applied to its top reflective and pixelated surface. The voltage determines the orientation of the liquid crystal molecules, which in turn determines the polarization state of the light reflected from the panel.

System & Optical Specification

The HDP-1280-2 can optically be described as a switchable and reflective zero-order half wave plate. There are two defined optical states, where switching from one to the other is done by reversing the polarity of the electric field applied across the liquid crystal slab. The HDP-1280-2 is assembled such that the angle between the two optical states is nominally bisected by the pixel columns (i.e. phase buff).

As for all liquid crystal devices, the electric field applied across the FLC needs to be "DC balanced" over time. The term "DC balance" implies that the time average of the electrical field applied across any given area of the pixel array is zero. In practice, this means that if a certain field polarity was applied to a pixel for a time *t*, the opposite field polarity also needs to be applied over a time *t*. This requirement dictates that the time average of the applied electric field needs to be zero (within 10%) over any time period longer than the time period listed in Table 2.

However, the user of the HDP cannot directly specify the electric field across the FLC. Instead, the user specifies when he or she wants one optical state or the other. Since there is a direct relationship between the applied electric field and the optical state, the DC balance requirement means that the same requirement applies to the optical states. Hence, over any time period longer than the time period listed in Table 2, the total time one optical state is used should not be shorter or longer than the total time the other optical state is used. The maximum deviation from this condition needs to be limited to the percentage value listed in the same row of the table.

This requirement may be accomplished using either of two methods. In the simplest method, each image being sent to and displayed by the HDP is followed by showing the inverse image on the HDP. The HDP-1280-2 has control features that facilitate this method, as described in the Electrical Specification section. Alternatively, the requirement can be met if the data patterns are known to approximately contain the same integrated time of each of the two optical states, for every pixel, over the time period listed in Table 2 (as described above). This method can be achieved by careful choice of data algorithm and data symbols, and by explicitly inverting alignment targets or other features.

Table 2: System requirements for operation of the HDP-1280-2.

Property	Specification
Time period that requires the HDP to be DC balanced to within 10%	> 100 ms

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Table 3: Cosmetic and surface properties of the HDP-1280-2 in the wavelength range of 440 to 640 nm.

Property	Specification
Reflectivity of air to glass interface (450nm to 650nm)	≤ 1 %
Electrically bad and/or fully obscured pixels[1]	2 columns, 2 rows, 2048 pixels
Sum of length of AR coating scratches (width <12um)	No limit
Refractive Index of Glass (n_d)	1.510 @ 530nm
Glass Thickness	0.630mm ±0.050mm

[1]Fully obscured pixels can be caused by contamination, scratches or digs of the surface of the window glass. Fully obscured pixels can also be caused by contamination and FLC imperfections within the cell gap. In all cases the imperfection "fully obscures" the pixel when ½ or greater of the pixel area is covered by the imperfection.

Optical Specification

For HDP temperature (as measured by the internal panel temp sensor) $T_P = 25 \pm 2$ °C and $AV_{cc} = 5.25$ V ± 5%:

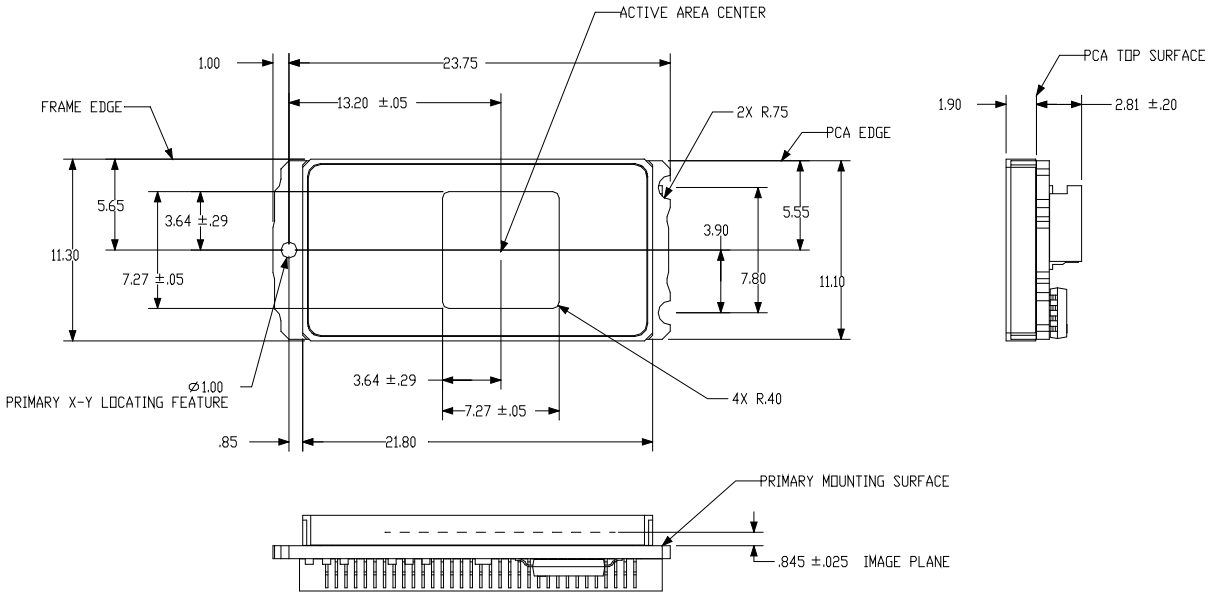
Table 4: Optical Specifcations of the HDP-1280-2

PARAMETER	MIN	TYP	MAX
Center wavelength	TBD	555nm	TBD
Tilt angle	TBD	48.6°	---
Switching speed	---	200 µs	TBD

Mechanical Specification

The package for the HDP-1280-2 is shown below in Figure 1. The package is a simple multi-layer FR4 based package with a 67-pin FCI ZIF flex connector on the rear surface (FCI p/n 62789-67111). The package includes a frame to contain the wirebond encapsulant material. The package does not include an optical aperture, however a protective cover is included. The recommended mounting shall be via registration to the FR4 front surface. Mounting shall not induce pressure or torque to the package, as this may result in a change in the product's optical properties.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com



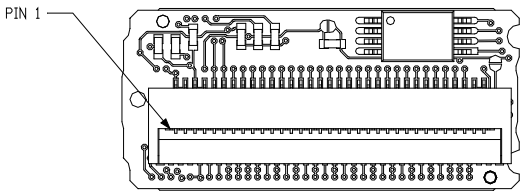
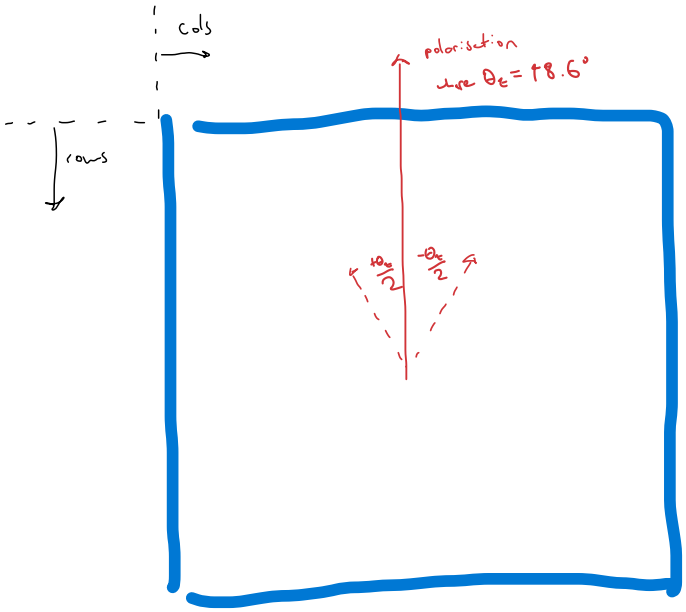


Figure 1: HDP-1280-2 Package

Dimension tolerances are +/- 0.10mm unless noted.



Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Electrical Description

The HDP-1280-2 converts binary data to modulated light. The HDP contains two frame buffers to allow the simultaneous display of one data page and writing of a second page. The HDP includes a data interface and a separate 4-wire serial control interface. Additionally, discrete signal pins are included to trigger some pixel update functions.

Electrical Interface

During normal operation, data is supplied to the HDP through a 32 bit data bus (DATA [31:0]). The data interface also includes a VALID signal, a SYNC signal, and a CLOCK. VALID is used to instruct the HDP when to capture a line of data from the DATA pins. SYNC is asserted to control the vertical data pointer position. The DATA bus, VALID and SYNC signals are sampled at the rising edge of the CLOCK signal. The DATA bus, VALID, SYNC, and CLOCK signals are routed on controlled impedance traces to yield a characteristic impedance of 50 Ohms.

The HDP can be configured to respond to the additional control signal pins called UPDATE and INVERT. These signals and their use are described in detail later in this document.

The HDP serial control interface is composed of 4 signals: SCK, SEN, SDAT, and SOUT. The signals SCK, SEN, and SDAT are driven by the host while SOUT is controlled by the HDP. Operating modes, register values, and other display settings and characteristics may be programmed or interrogated through this serial interface.

The signal NRESET is provided to allow the user to force the HDP into the power-on reset state.

Power to the HDP is provided via two supplies. The core supply is 2.5V. Analog voltages for drive of the pixels are developed from the AVCC (5.25V) supply. All power supplies and signals are referenced to the GND pins.

Table 5 shows the pin assignments for the 67 pin connector to the HDP.

Table 5: Pin Descriptions

Pin Num.	Pin Name	Pin Direction	Typical pull-up/down value (Ohms)	Pin Function
1.	GND	Ground	-	Power and signal return
2.	AVCC	Power	-	Analog power supply
3.	GND	Ground	-	Power and signal return
4.	AVCC	Power	-	Analog power supply
5.	GND	Ground	-	Power and signal return
6.	GND	Ground	-	Power and signal return
7.	GND	Ground	-	Power and signal return
8.	GND	Ground	-	Power and signal return
9.	UPDATE	Input	25K down	HDP update signal
10.	SYNC	Input	25K down	Sync input
11.	VALID	Input	25K down	Valid data input
12.	INVERT	Input	25K down	Invert HDP update signal
13.	GND	Ground	-	Power and signal return

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

14.	CLOCK	Input	25K up	Clock input
15.	GND	Ground	-	Power and signal return
16.	DATA10	Input	25K down	Pixel data input
17.	CRCERROR	Output	-	CRCERROR calculation output, unverified
18.	DATA11	Input	25K down	Pixel data input
19.	GND	Ground	-	Power and signal return
20.	DATA12	Input	25K down	Pixel data input
21.	DATA9	Input	25K down	Pixel data input
22.	DATA13	Input	25K down	Pixel data input
23.	VDD	Power	-	Core power supply
24.	DATA14	Input	25K down	Pixel data input
25.	DATA8	Input	25K down	Pixel data input
26.	DATA15	Input	25K down	Pixel data input
27.	GND	Ground	-	Power and signal return
28.	DATA16	Input	25K down	Pixel data input
29.	DATA7	Input	25K down	Pixel data input
30.	DATA17	Input	25K down	Pixel data input
31.	VDD	Power	-	Core power supply
32.	DATA18	Input	25K down	Pixel data input
33.	DATA6	Input	25K down	Pixel data input
34.	DATA19	Input	25K down	Pixel data input
35.	GND	Ground	-	Power and signal return
36.	DATA20	Input	25K down	Pixel data input
37.	DATA5	Input	25K down	Pixel data input
38.	DATA21	Input	25K down	Pixel data input
39.	VDD	Power	-	Core power supply
40.	DATA22	Input	25K down	Pixel data input
41.	DATA4	Input	25K down	Pixel data input
42.	DATA23	Input	25K down	Pixel data input
43.	GND	Ground	-	Power and signal return
44.	DATA24	Input	25K down	Pixel data input
45.	DATA3	Input	25K down	Pixel data input
46.	DATA25	Input	25K down	Pixel data input
47.	VDD	Power	-	Core power supply
48.	DATA26	Input	25K down	Pixel data input
49.	DATA2	Input	25K down	Pixel data input
50.	DATA27	Input	25K down	Pixel data input

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

51.	GND	Ground	-	Power and signal return
52.	DATA28	Input	25K down	Pixel data input
53.	DATA1	Input	25K down	Pixel data input
54.	DATA29	Input	25K down	Pixel data input
55.	VDD	Power	-	Core power supply
56.	DATA30	Input	25K down	Pixel data input
57.	DATA0	Input	25K down	Pixel data input
58.	DATA31	Input	25K down	Pixel data input
59.	GND	Ground	-	Power and signal return
60.	SOUT	Output	-	Serial interface data output
61.	SCK	Input	25K up	Serial interface clock input
62.	SDAT	Input	25K down	Serial interface data input
63.	SEN	Input	25K up	Serial interface chip select
64.	GND	Ground	-	Power and signal return
65.	NRESET	Input	25K up	Reset input
66.	GND	Ground	-	Power and signal return
67.	VDD	Power	-	Core power supply

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Electrical Requirements

Table 6 and Table 7 show the HDP-1280-2's voltage and current requirements.

Table 6: DC Characteristics

Item	Symbol	Measurement Conditions		Min	Typ	Max	Unit
Input High Voltage	V_{IH}			1.7		VDD + 0.3	V
Input Low Voltage	V_{IL}			-0.3		0.7	V
Input Leakage Current	I_{IL}	$V_I = V_{IL}$		-10			uA
	I_{IH}	$V_I = V_{IH}$				10	uA
Pull up/down	R_P			10K	25K	120K	Ohms
Output High Voltage	V_{OH}	I_{OH} = 2mA		2.0			V
Output Low Voltage	V_{OL}	I_{OL} = 2mA				0.4	V
Supply Voltage	VDD			2.3	2.5	2.7	V
Supply Voltage	AVCC			5.0	5.25	5.5	V
Supply Current	I_{VDD}	2.3V<VDD<2.7V	Normal Mode			250	mA
			Sleep Mode			25	mA
Supply Current	I_{AVCC}	5.0V < AVCC < 5.5V	Normal Mode			25	mA
			Sleep Mode			100	uA

Table 7: Absolute Maximum Ratings

Item	Min	Max	Unit
VDD to GND		3	V
AVCC to GND		6	V
Voltage on any Input Pin to GND	GND-0.4	VDD+0.4	V

Theory of Operation

The HDP-1280-2 is operated by storing one or two frames of data to the frame buffers and then commanding the HDP to display those frames. An update command results in the copying of a frame buffer to the pixels. The dual frame buffers allow the HDP to actively display one page while the other is reloaded. The HDP can additionally be commanded to display the inverse of the data stored in the frame buffers.

Data for the frame buffers is transferred to the HDP through the DATA bus. Each bit of the DATA bus represents the desired state for a pixel. Figure 2 shows the location of the first data word and bus bit order for the HDP in the default orientation and bus order. Data on the bus is captured according to the state of the VALID signal. The DATA and VALID signal are sampled according to the CLOCK signal. To write one line of data to the HDP, the VALID signal is held active for 40 clock periods, during which 40 data words are captured and stored (32bits*40words= 1280 pixels). A transfer of less than 20 data words is considered incomplete and the data is not stored.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

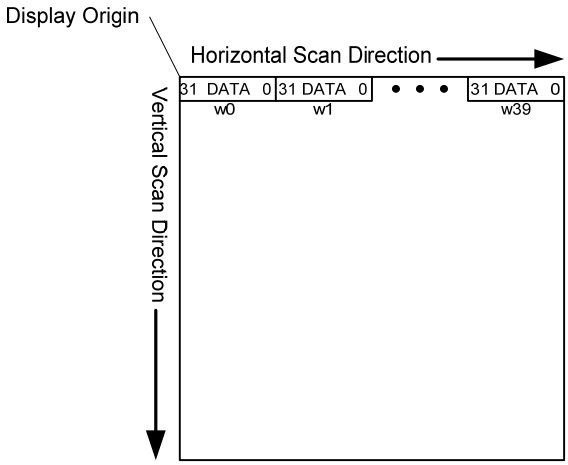


Figure 2: HDP-1280-2 Array showing location of first data word to the HDP panel

The frame buffer can be loaded top to bottom or bottom to top according to the Vertical Direction bit of the HDP Mode Register. Similarly, the horizontal loading direction of the input data can also be controlled by the Horizontal Direction Mode bit of a serial register. The frame buffer to which the data will be stored is automatically switched at each panel update without the INVERT signal asserted, or set when a panel update is commanded through the serial interface.

On startup the HDP will be in the *Sleep* state. After the CLOCK is present the serial interface must be inactive for a period of t_{WAKE}. To begin operation, the HDP should then be transitioned to the *Standby* state, during which the HDP will activate the voltage fields for the liquid crystal. After the serial transfer to set the HDP into *Standby state*, a time period of t_{STBY} must be observed before the HDP may be transitioned to the *Normal* state to begin display of input data frames. While in the *Standby* state, the HDP can accept input data and store it into the frame buffers; however, the UPDATE signal and serial update command will be ignored. Once in the *Normal* state, the host causes the HDP to copy frame buffer data to the HDP pixels by writing to the Update register or activating the UPDATE signal pin. The copy function will require a period of t_{SET} to copy the frame buffer data to the pixels. Additional writes to the Update register, or activations of the UPDATE pin, can be used to load the HDP pixels with the contents of the other frame buffer.

The HDP is programmed using the Update Mode configuration bit to be in either external update mode or serial update mode. While in external update mode, the serial update command is ignored, also in serial update mode transitions on the UPDATE and INVERT pins are ignored. While in serial update mode, the update command is also used to select the Frame_Source and Frame_Destination. Updates to the HDP via the UPDATE pin automatically cause the Frame_Source and Frame_Destination buffers to switch, unless the INVERT pin is high, thus facilitating transfers with the minimal amount of control overhead. Activation of the UPDATE pin causes the buffers to switch and the contents from the new Frame_Source buffer are copied to the pixels.

In order to DC balance the HDP, the host may wish to display the inverse contents of the Frame_Source buffer. This can be accomplished by making the INVERT pin high while activating the UPDATE pin. This will not switch the Frame_Source and Frame_Destination buffers. Successive updates with INVERT high will cause the pixels to toggle states.

Updates of the HDP pixel data are performed by copying of the frame buffer data to the pixels on a row by row basis. Update times of the HDP can be accurately controlled via the serial interface or UPDATE pin. If the host writes to the Update register, the copying process will begin when the rising edge of SEN is detected at the end of the serial transfer. Alternately, the rising edge of the UPDATE pin is detected to begin the copying process.

In the *Normal* state the HDP is holding a DC voltage field across each pixel according to the values stored in each pixel. It is the host's responsibility to ensure that the DC field of each pixel is maintained at 0V. This is accomplished by ensuring that the time each pixel is kept in the *On* state is equal to the time that pixel is kept in the *Off* state. These equal time periods can be enforced by explicitly setting each pixel to its inverse logic state or by statistical knowledge of the contents of successive frames of data.

When the HDP is in *Standby* state, the HDP will actively update the contents of pixels and the apron area to ensure DC balance is maintained. Once the first transition from the *Sleep* state to the *Standby* state has been completed, observing the wait time of t_{STBY}, the HDP can be transitioned from the *Standby* state to the *Normal* state, or vice versa, as required, without any wait time between operations.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

At the time when the HDP operations are complete, the HDP must be transitioned to the *Sleep* state by writing the HDP Mode Register. This ensures that all voltage fields are properly removed from the HDP's liquid crystal. The HDP can be transitioned from either the *Normal* or *Standby* states to the *Sleep* state. After writing the serial register to put the panel into sleep mode, no further data transfers should be sent. Sleep mode power levels cannot be guaranteed unless this restriction is observed.

The HDP pixels are surrounded by a large conductor referred to as the apron. The apron controls the electric field for the liquid crystal outside the active pixel region. The apron in the region immediately adjacent to the active area is pixelated and connected in a checkerboard pattern to two drivers of alternate polarity. When using the UPDATE pin to control the HDP, the *On/Off* state of the apron is switched automatically following each update invoked by the UPDATE pin. It is the host's responsibility to maintain a 0V DC field on the apron.

After initial power-up, when the system clock is applied the HDP goes through a process of loading default serial register values from its EEPROM. The HDP additionally places itself in a *Sleep* state wherein all voltage fields are removed from the liquid crystal. The HDP is then ready to receive the first transfer of frame data.

The HDP contains an on-silicon temperature sensor which may be read serially through the Temperature Register. The temperature sensor provides an accuracy of +/- 3º C. The temperature is only continually read when the panel is being driven. For conversion from temperature sensor reading to degrees Celsius see the detailed register description.

Frame buffer data can be retrieved from the HDP for testing purposes. When in the *Test* state, the Serial Command register can be written so as to cause one line to be read from the frame buffer to a shift register. The data row address from which to read is set via the Serial Row Address register, the buffer to be read from is the Frame_Destination buffer, which may be set using the Serial Command SetDestBuffer. The contents of the shift register are accessed by performing a polling read of the Test Data Read Register, where each byte will be shifted out in sequence while the SEN pin is held low.

Data Interface

The HDP has several registers used to control and monitor panel addressing. The Current Address Pointer Registers contain the currently active data row address. The Row Address Start Pointer Registers contain the address of the starting row address for each frame of data. The Row Address Start Pointer Registers are loaded using the serial command SetStartAddr, from the row address set in the Serial Row Address Registers. When an Update occurs (without INVERT asserted) the Current Row Address Pointer will be reset to the Row Address Start Pointer, along with the switching of the Frame_Destination pointer such that the HDP is ready to receive the next frame of data. When a valid line has been transferred to the HDP, the Current Panel Address Pointer will automatically increment, such that the HDP may be used without sending data row address information for each line.

The Current Row Address Pointer may also be set using external signals. A SYNC pulse high with VALID low signifies that Row Address information is present on the data bus. This address will be stored as the Current Panel Address Pointer. Figure 3 shows the operation of the row addressing in the HDP. Note that the Current Panel Address Pointer is incremented after each line of data is received, if no additional VALID line is received, the last line stored will be the Current Panel Address Pointer minus one.

If the Current Row Address Pointer is incremented past 1279, the pointer will stay at 1280, and if valid lines continue to be sent, the data will not be written to the panel. The Current Row Address Pointer may be reset to a valid address at any time using external addressing (SYNC), or serial transfer.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

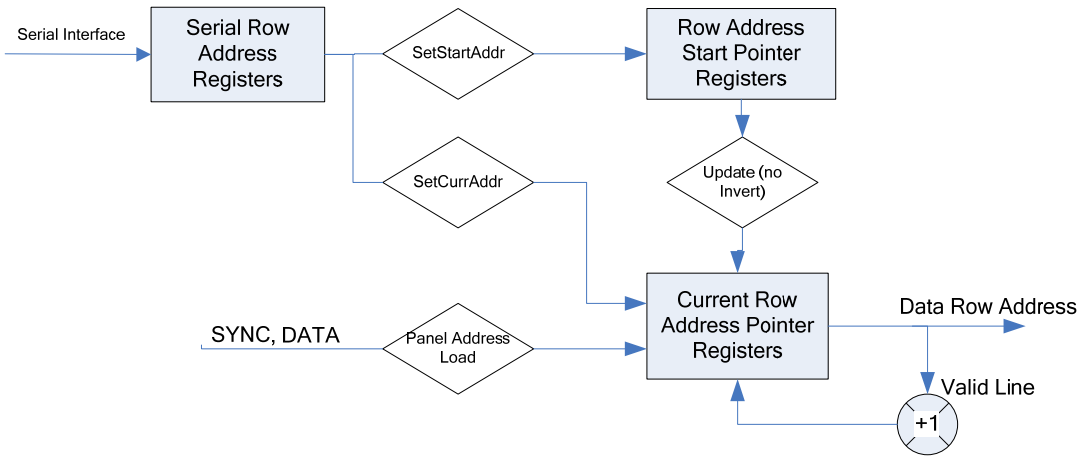


Figure 3: Data Row Addressing

Figure 4 illustrates the use of SYNC to load the Row Address register to an arbitrary address followed by transfer of data lines. Table 8 specifies the required line timing for loading of data to the HDP.

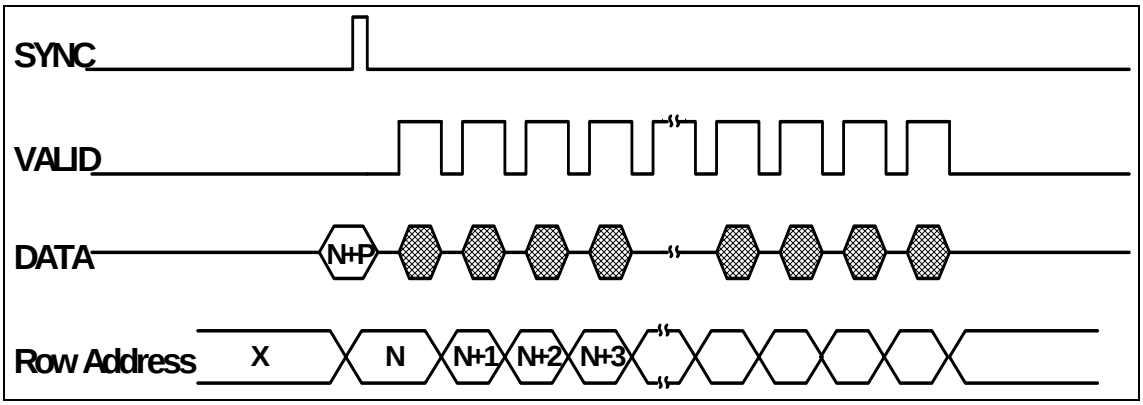


Figure 4: Frame Buffer Load Illustration, SYNC with VALID

Table 8: AC Characteristics, Frame Buffer Load Timing

Item	Symbol	Min	Typ	Max	Unit
VALID high time period	t_{ACT}	40	40	40	Clocks
Time between VALID periods	t_{BLANK}	4	-	-	Clocks
Delay time from VALID↓ to SYNC↑	t_{SD}	4	-	-	Clocks
Setup time from SYNC↓ to VALID↑	t_{SS}	3	-	-	Clocks
Pulse Width of SYNC	t_{SYNC}	1	-	1	Clocks

The DATA, VALID, and CLOCK input signals must meet the timing requirements shown in Figure 5 and Table 9.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

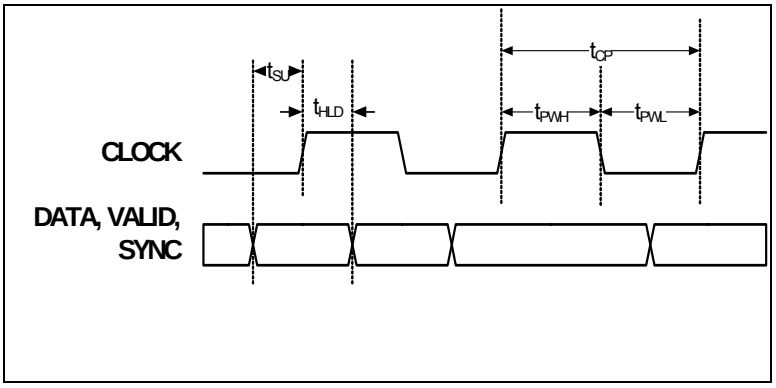


Figure 5: Input/Output Signal Timing

Table 9: AC Characteristics, Input/Output Signal Timing

Item	Symbol	Min	Typ	Max	Unit
CLOCK, average rate (average ≥ 100 cycles)	100/ 100*t_{CP}	25	-	140	MHz
CLOCK, rate including jitter (for 1 cycle)	1/t_{CP}	25	-	140	MHz
CLOCK, pulse width high	t_{PWH}	45% t_{CP}	50% t_{CP}	55% t_{CP}	NA
CLOCK, pulse width low	t_{PWL}	45% t_{CP}	50% t_{CP}	55% t_{CP}	NA
DATA, VALID, SYNC setup time	t_{SU}	1.5			ns
DATA, VALID, SYNC hold time	t_{HLD}	2.5			ns

Quarter-page Tiling Mode

The HDP-1280-2 can be operated in a quarter page tiling mode that allows the user to send one-fourth the data for each display frame. In this mode, the data will be replicated (subject to an inversion specified in the TileMode register) in each quadrant of the active display area, as shown below in Figure 6.

In this mode, VALID must be asserted for a minimum of 20 clock cycles to transfer a 640 pixel line. The data will be replicated in each quadrant of the active display area. When UPDATE is asserted or the UPDATE serial command is sent, the current TileMatrix is used to determine the inversion state of each quadrant of the panel with a 1 indicating the corresponding quadrant should be inverted. The current TileMatrix can be specified in two ways. When TileMatrixSrc is set to 0, the TileMatrix value in the TileMode register is used at the time the update begins. When TileMatrixSrc is set to 1, The TileMatrix is indicated by DATA[19:16] while SYNC is high and VALID is low (same time as updating CurrentAddress). The TileMatrix will be associated with the destination buffer active at the time of the SYNC pulse, with the most recent value overriding any previously set value. All subsequent updates using this buffer will use the last set TileMatrix.

When inverting while updating, each quadrant of the HDP will be inverted from the state specified by the currently active TileMatrix.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

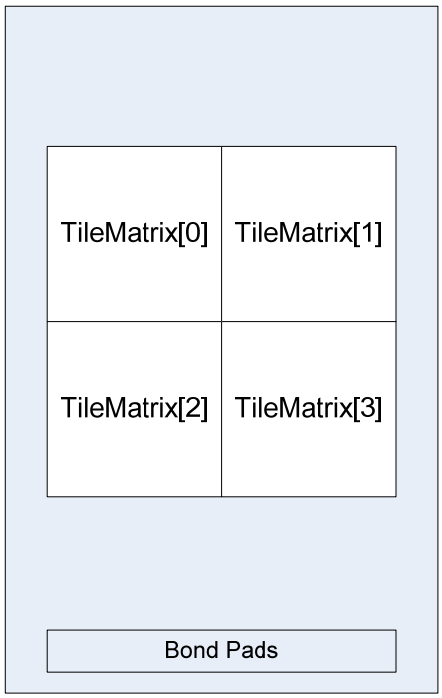


Figure 6: Tiling Mode Quadrants

Control Interface

The HDP pixels are controlled by causing the pixel values to be copied from one of the two frame buffers. The commands to cause the pixels to be updated are provided by the host. The host can either control the HDP via two discrete signals, UPDATE and INVERT, or by writing to the HDP's Command Register via the serial interface. After an Update has been initiated, the HDP requires a time period t_{SET} for the pixel electrodes to be updated, and a time period t_{BLNK} for the pixels to become optically stable.

Figure 7 and Figure 8 illustrate the use of the discrete control signals to control the data driving the HDP pixels. No restriction exists on the timing of the UPDATE signal to VALID when the INVERT pin is high (the Frame_Destination buffer is not switching). Also no restriction exists between SYNC and UPDATE. The INVERT signal is used to toggle the inversion of the panel update, i.e. successive updates with INVERT asserted will toggle the state of the pixel electrodes. An update without INVERT asserted will reset the toggle value such that the first update with INVERT asserted after an update without INVERT asserted will always update the panel with inverted data from the source buffer. Thus one can fully DC balance the panel by using an even number of updates (with identical refresh rate), the first without INVERT asserted, and all subsequent updates with INVERT asserted.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

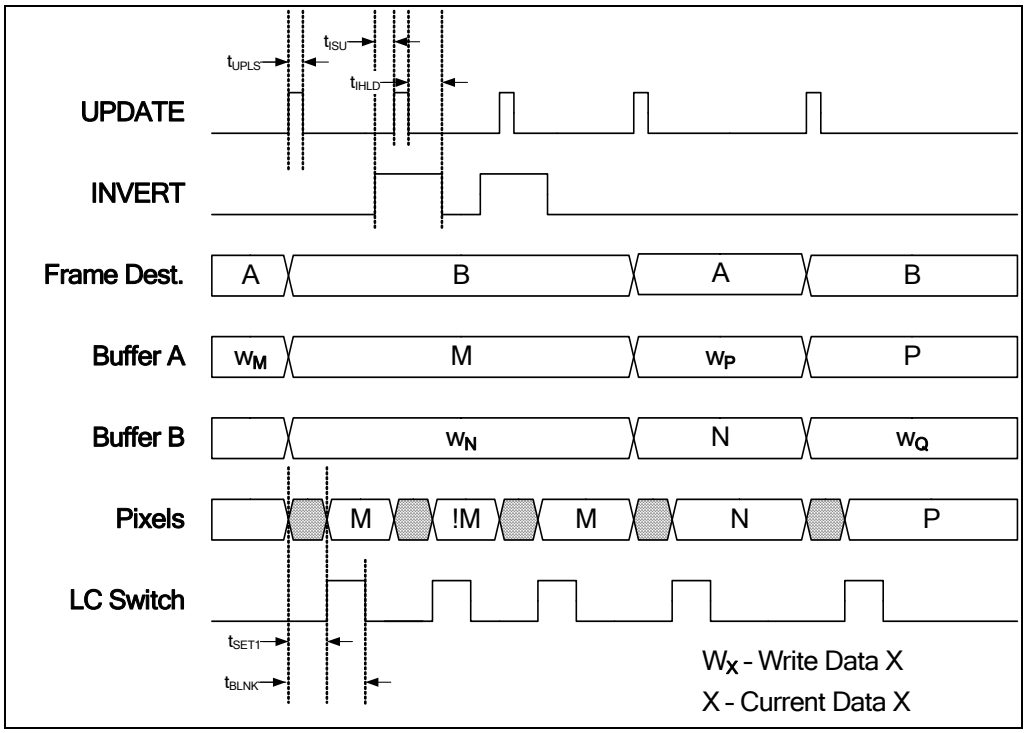


Figure 7: HDP Display Control by Discrete Signals
(Time period t_{blnk} is referred to in Table 2)

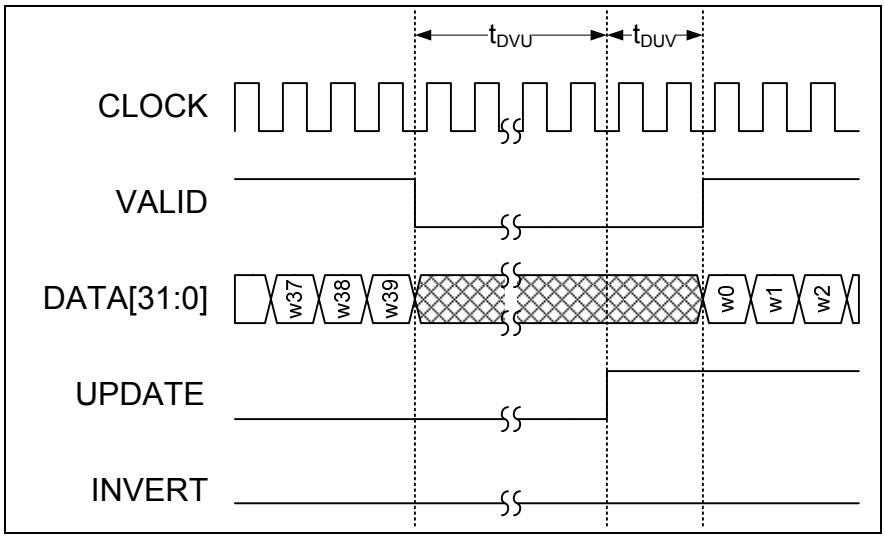


Figure 8: HDP External Update Control Timing

Table 10 specifies the timing requirements for use of the discrete control signals and provides the time the HDP requires to write all pixels following the use of the UPDATE control signal. The time the HDP requires to update the panel depends on the input data rate. The max specification of t_{SET1} should be used if data is being written to the panel while the update occurs.

Table 10: AC Characteristics, HDP Display Control by Discrete Signals

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Item	Symbol	Min	Typ	Max	Unit
UPDATE high time period	t_{UPLS}	24	48	-	Clocks
Setup time from INVERT to UPDATE↑	t_{ISU}	12	24	-	Clocks
Hold time from UPDATE↓ to INVERT	t_{IHLD}	12	24	-	Clocks
Time period for copying frame buffer to pixels (UPDATE ↑ to last copy) [1]	t_{SET1}	-	2500	2804	Clocks
Time period from end of VALID assertion to UPDATE assert with INVERT de-asserted	t_{DVU}	16	-	-	Clocks
Time period from start of UPDATE pulse to VALID assertion	t_{DUV}	0	-	-	Clocks

[1]Typical specification applies only when data bus is not active for the duration of the update time period

Figure 9 and Figure 10 illustrate the use of the serial interface to control the data driving the HDP pixels. When the HDP is updated using the serial interface without changing the Frame_Destination and Frame_Source buffers, no restriction exists on the timing of the serial interface signals with reference to the VALID signal. It should be noted that the Data Polarity bit set in the serial command PanelUpdate is directly the inversion state used to update the panel, it does not toggle the inversion state on each successive PanelUpdate command as does the discrete INVERT signal.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

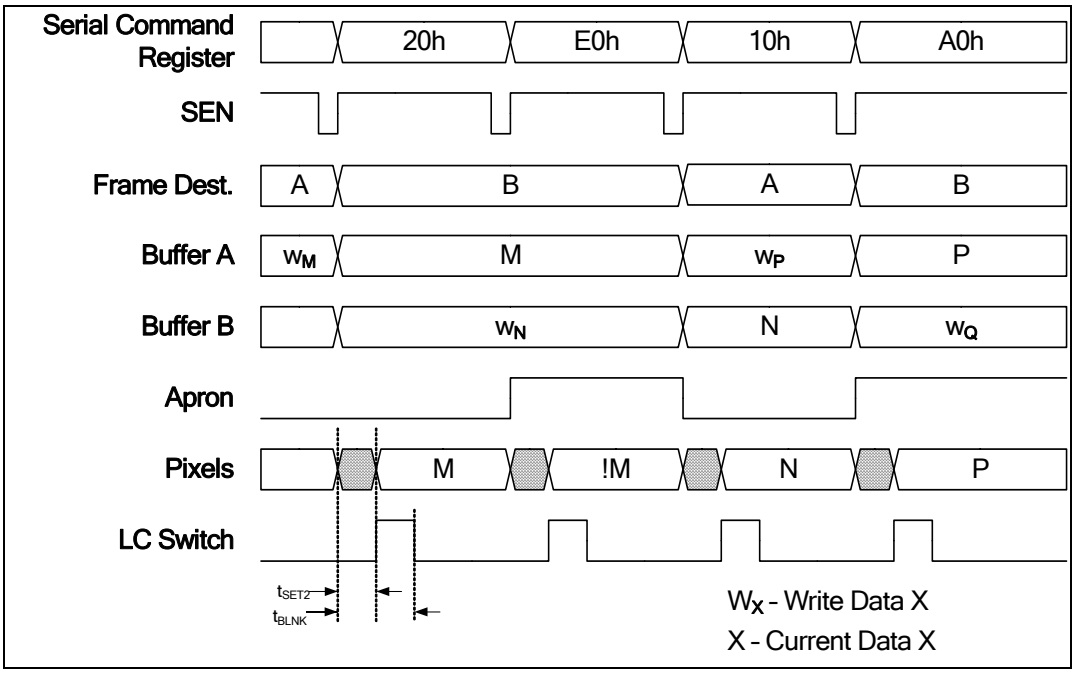


Figure 9: HDP Display Control by Serial Interface Signals
(Time period t_{blnk} is referred to in Table 2)

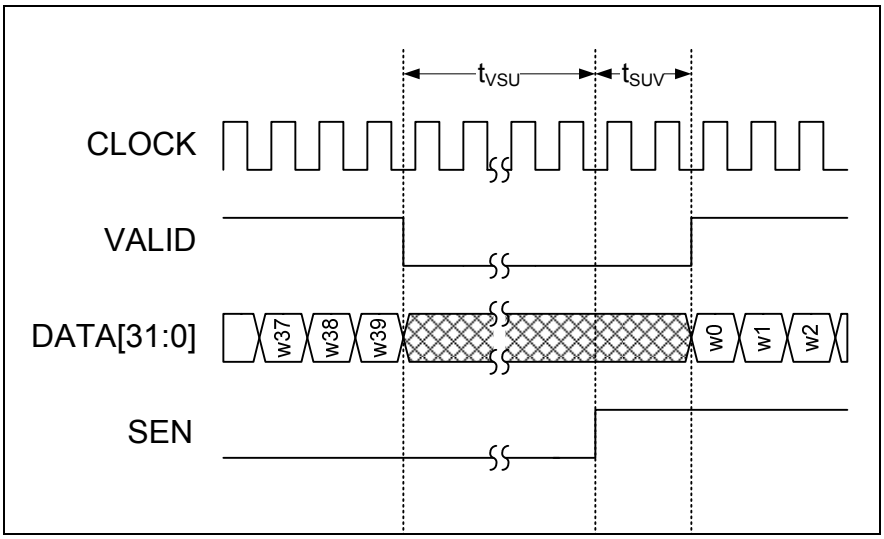


Figure 10: HDP Serial Update Timing

Table 10 provides the timing requirements for using the serial interface and provides the time the HDP requires to write all pixels following a PanelUpdate command using the Serial Command Register.

The HDP performs edge detection of the discrete control signals and the SEN signal assuming that these signals are asynchronous to the CLOCK. Additional clock cycles are provided in the required timing to allow for the detection of ambiguity and metastability protection circuits.

Table 11: AC Characteristics, HDP Display Control by Serial Interface Control

Item	Symbol	Min	Typ	Max	Unit

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Time period for copying frame buffer to pixels (SEN ↑ to last copy)[1]	t_{SET2}	-	2500	2804	Clocks
Time period from end of VALID assertion to rising edge of SEN[2]	t_{VSU}	60	-	-	Clocks
Time period from rising edge of SEN[1] to assertion of VALID	t_{SUV}	0	-	-	Clocks

[1] Typical specification applies only when data bus is not active for the duration of the update time period

[2] Rising edge of SEN for Serial Command Update with Destination Buffer Change

Serial Interface

The serial interface uses the signals SDAT, SCK, SEN, and SOUT. Through this interface, the HDP's registers can be both written and read. For a time period of t_{SDLY} after the power, CLOCK, and NRESET are present, the serial interface is not accessible.

The serial interface is activated by pulling the SEN input low. Then the SDAT input is sampled on each rising edge of the SCK input. A transfer is begun with the transfer of a read/write command bit and a 7-bit address. For a write command, this is followed by an 8-bit data word to store to that register address. For a read command, the HDP will output the addressed register's data to the SOUT output. The data is changed on the falling edge of the SCK input and can be sampled on each rising edge of the SCK input. The SOUT pin is a full level driver, which will be driven low when the serial interface is not accessed.

The HDP facilitates a multi-byte or polling read operation for certain registers. Only the HDP Status Register and Test Data Register support multi-byte reading. For the HDP Status Register, the contents of the register will be continually output until the SEN pin is pulled high. The Test Data Register will output a line of data in one read when the proper Test operations have been performed.

Figure 11 shows the required serial interface signal timing. Table 12 provides the serial interface timing requirements. Figure 12 and Figure 13 show examples of write and read transfers respectively.

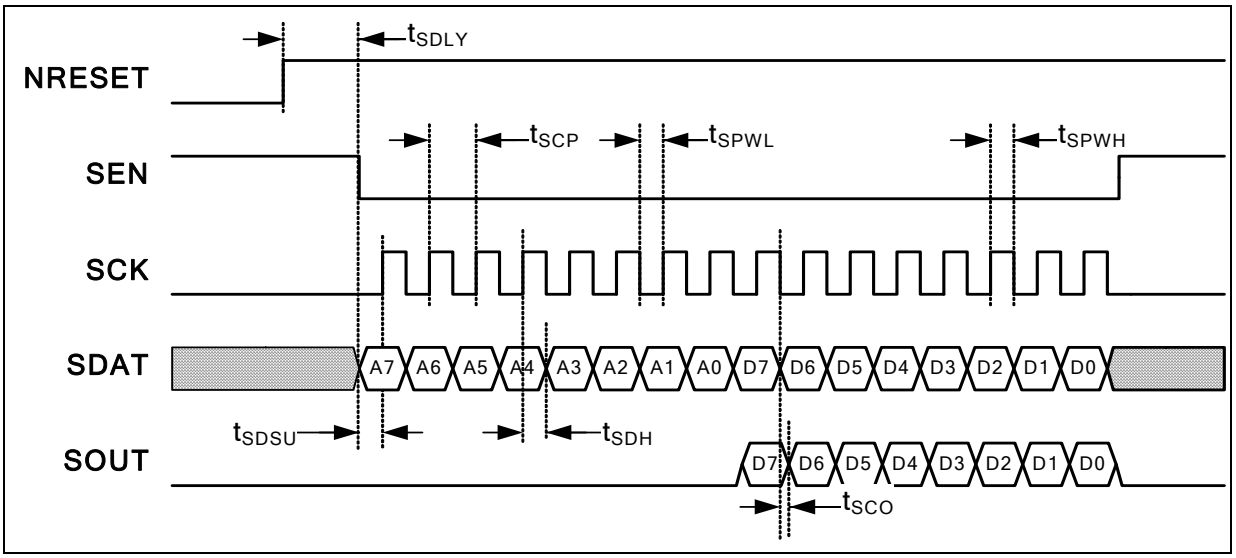


Figure 11: Serial Interface Signal Timing

Table 12: AC Characteristics, Serial Interface Signal Timing

Item	Symbol	Min	Typ	Max	Unit
Delay from reset to serial transfer	t_{SDLY}	8	-	-	ms

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

SCK, rate	$1/t_{SCP}$	-	-	2000	KHz
SCK, pulse width high	t_{SPWH}	45% t_{SCP}	50% t_{SCP}	55% t_{SCP}	
SCK, pulse width low	t_{SPWL}	45% t_{SCP}	50% t_{SCP}	55% t_{SCP}	
SDAT and SEN, setup time	t_{SDSU}	10	-	-	ns
SDAT and SEN, hold time	t_{SDH}	10	-	-	ns
SDO, falling edge of SCK to SDOUT valid	t_{SCO}	-	-	50	ns

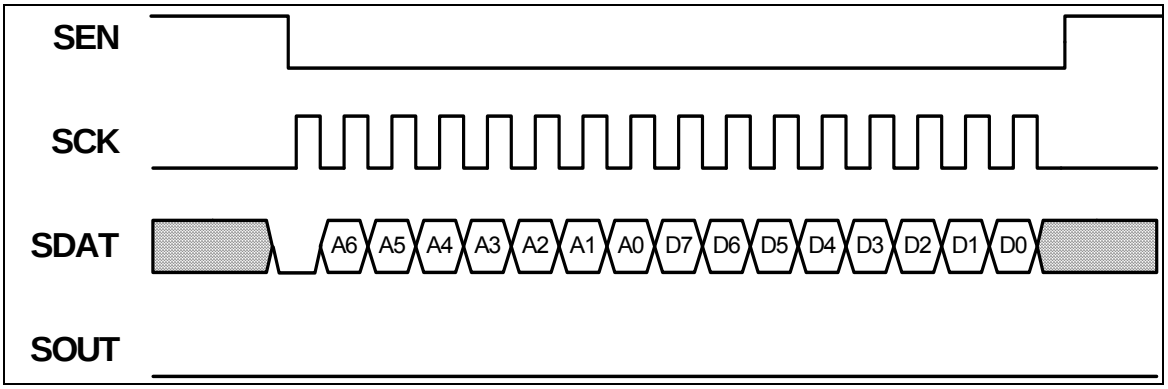


Figure 12: Serial Interface Write Example

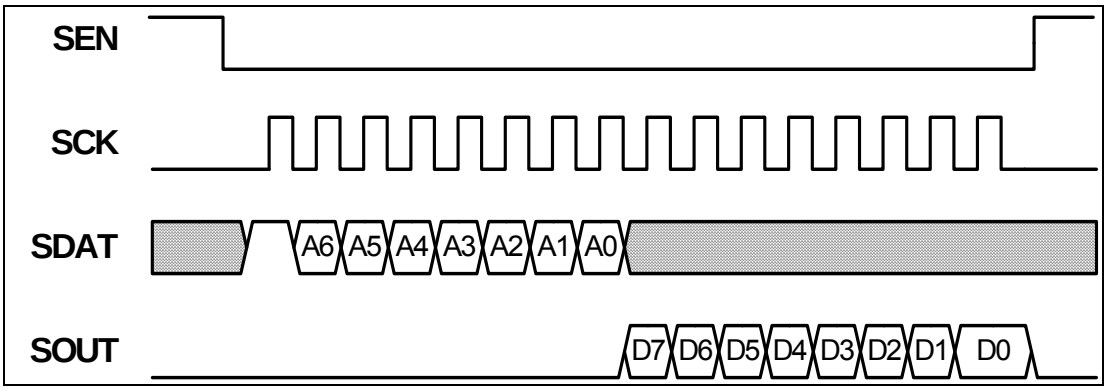


Figure 13: Serial Interface Read Example

Startup and Shutdown Sequence Requirements

In order to assure DC balance and protection of the HDP-1280-2, a particular control sequence is required.

Following the application of the power supplies, the NRESET input may be held low and remain low for a period of t_{RESET} in order to reset the HDP to a known state. The HDP incorporates its own Power-On-Reset circuit which may be sufficient for some systems.

Following the application of power and NRESET, the HDP is in a *Reset* state. During the *Reset* state the HDP pixels are not actively driven. When the CLOCK signal is applied the HDP will go through an initialization sequence, including loading the HDP configuration settings from the EEPROM. During this initialization time, the serial interface cannot be accessed.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

If needed the HDP's GPIO register can be written in the absence of the CLOCK signal. This is intended to allow the control of a SERDES chip or other device using only the serial interface signals. As soon as the CLOCK becomes active, the HDP will begin its initialization process.

Following the initialization process, the HDP is in the *Sleep* state. During the *Sleep* state the HDP pixels are not actively driven. After time period t_{SDLY} the serial interface may be accessed and the HDP can be set to the *Standby* state with the serial interface. Prior to entering the *Standby* state the HDP Clock Frequency Register should be set with the operating clock frequency. After a period of t_{STBY}, during which the HDP is initializing the pixel voltages, the HDP may be set to the *Normal* state.

Once the HDP-1280-2 has been set to the *Normal* or *Standby* states, the device must be returned to the *Sleep* state, using the serial interface, for a time period t_{PWRD} prior to the removal of any power supply, during which time CLOCK must remain present and NRESET be maintained high. After writing the serial register to put the panel into sleep mode, no further data transfers should be sent. Sleep mode power levels cannot be guaranteed unless this restriction is observed. The required startup and shutdown sequence for the HDP is shown in Figure 14. The control sequence timing requirements are given in Table 13.

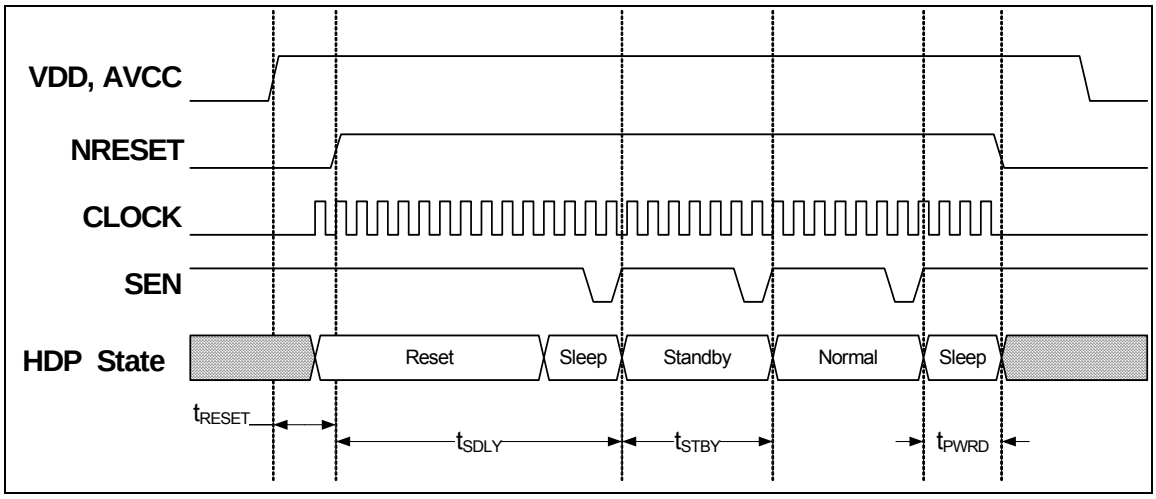


Figure 14: HDP Startup and Shutdown Sequence

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Table 13: AC Characteristics, HDP Startup and Shutdown Sequence Timing

Item	Symbol	Min	Typ	Max	Unit
Time from last power supply until NRESET high	t_{RESET}	100	-	-	ns
Delay from NRESET high and CLOCK asserted to complete initialization	t_{SDLY}	960,000	-	-	CLOCK cycles
Delay from transition to Standby state to pixel voltage initialization complete	t_{STBY}	960,000			CLOCK cycles
Time from *Sleep* mode entered to removal of CLOCK or assertion of NRESET	t_{PWRD}	1500	-	-	µs

Test Operations

The HDP-1280-2 contains test features that may be used to determine if data is being written correctly. A line of Test data may be loaded into the buffer memory or a line of buffer memory may be read using the serial interface. The HDP must be put into the *Test* state prior to using the test operations.

Load Line Operation

The Load Line operation is used to write a line of the frame buffer memory. The frame buffer may be selected by setting the Frame_Destination pointer using serial commands. Running the LoadData command while the HDP is in the *Test* state will load the currently addressed buffer row with data from the Test Data Registers. The 128-bits of TestData will be replicated 10 times to produce one line of input data.

Data Read Operation

The Data Read operation is designed to assist in debug of a system using the HDP-1280-2. Both page buffers may be read using the serial interface one line of data at a time. The Data Read operation consists of setting the row address and Frame_Destination pointer using serial commands, running the data read serial command, then using a multi-byte or polling read of the Data Register to capture the line of page data.

To set up the Data Read operation, the Serial Row Address registers are set with the data row address, then the SetCurAddr command is used to load the serial row address into the HDP row address pointer. The SetDestBuffer serial command is used to set the desired buffer from which to read data. The SetDestBuffer requires "Serial update mode" to be set. The ReadData command sets up the data read, followed by reading data out through the Read Data Register.

Once the ReadData command is executed, the data is read out using a polling read operation of the Test Read Data Register. The full line is 160 bytes of data, which is read out starting from the last data word in the row first. If the input line is considered as 32-bit words starting at word 0 as the first word sent, the least significant byte of data word 39 is read first, followed by the next 3 bytes of data word 39, then the least significant byte of data word 38, etc. Figure 15 shows the serial read operation used to read out a line of data. One should note that if HFlip was set when the data was received while the HDP was in the Normal state, the data will be not only read out from first data word to last, but will be swizzled as well, meaning that the bit and byte order will be reversed, i.e. the first byte read will be the MSB of the first data word, swizzled.

After Test operations are completed, the HDP should be returned to the *Standby* state prior to entering the *Normal* state. The *Standby* state timing specification (t_{STBY}) must be met when transitioning from the *Standby* state to the *Normal* state.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

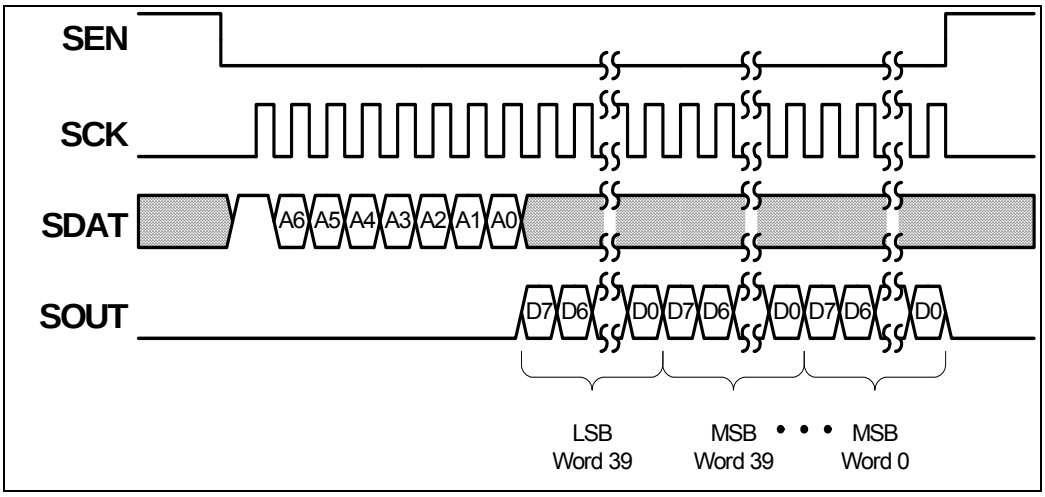


Figure 15: Serial read of Test Read Data Register

Mechanical Stress and Reliability Specification

The performance of the HDP panel in regards to shipping-induced stresses and reliability will be based on the known performance of Displaytech's viewfinder products.

Table 14: Mechanical Stress and Reliability Specifications

Parameter	Specification
Mean Time Before Failure	TBD hours at nominal operating conditions. Continuous operation within the limits specified in this document.
Shock, Non-operating (bench handling)	Acceleration = 300 g Shock Pulse = 2 ms
Vibration, Non-operating	Acceleration = 10 g Frequency = 20 Hz – 2 kHz

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Appendix A: General Device Handling

This appendix describes the handling requirements for Displaytech Holographic Display Panel (HDP), Model HDP-1280-2.

General Handling

The HDP should be treated carefully, as any other precision device. This section provides guidelines for the proper handling and integration of the module. Following these guidelines ensures the best opportunity for a smooth, defect-free integration process.

Cleanliness

The HDP should be handled and assembled in a class 10,000 clean-room (or cleaner) or under a positive pressure, laminar flow bench filtering to 0.5 μm. Use dry air, filtered to 0.5 μm particle size to remove dust or debris from the HDP. Do not blow directly onto the HDP cover glass with high pressure.

Electro Static Discharge (ESD)

Personnel who handle the HDP should always be fully grounded and follow electronics industry standard ESD procedures. All work areas where unpackaged HDPs are processed must have grounded, conductive flooring (or mats) and a grounded, conductive work surface. Personnel handling unprotected HDP components (outside of ESD protective packaging) should wear a grounding heel strap or a grounded, conductive wristband.

Radiation

Limit the exposure of HDP to unfiltered ultraviolet (UV) radiation. Long periods of exposure may degrade HDP performance and have negative effects on the device materials.

Mechanical

It is important to avoid touching or contacting the HDP cover glass which may degrade optical performance. It is recommended to handle the HDP at the edges of the FR4 substrate.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Appendix B: Registers

Configuration Registers

The configuration registers are set following power-up by the configuration EEPROM, subsequently they can be read and written with the four-wire serial interface.

HDP Mode Register, with Default Settings

Register Index: 01h. Register may be read and written.

7	6	5	4	3	2	1	0
TileEnable	Vertical Flip	Horizontal Flip	BitOrder	RES	Update Mode	HDP Mode	
0	0	0	0	0	0	00	

TileEnable: 0 = Tile Disable, 1 = Tile Enable

Vertical Flip: Controls input data fill direction
0=Top to Bottom
1=Bottom to Top

Horizontal Flip: Controls input data fill direction.
0=Left to Right
1=Right to Left

Bit Order: Data bus bit ordering
0 = Normal data bus bit ordering. DATA[31] of the first word in each row corresponds to pixel column 0, when Horizontal Flip is not asserted.
1 = Swizzled data bus bit ordering

Update Mode 0=Update using external signals
1=Update using serial command

HDP Mode: 00 = Sleep Mode
01 = Standby Mode
10 = Normal Mode
11 = Test Mode

HDP Status Register, with Default Settings

Register Index: 03h. Register is Read Only.

7	6	5	4	3	2	1	0
RES	LC Switch	Apron	RES	RES	RES	Destination Buffer	Source Buffer
0	1	0	0	0	0	0	0

LC Switch: 0=LC state is transitioning
1=LC is stable

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Apron: 0=Apron is currently low
1=Apron is currently high

Destination Buffer:
0=Current destination buffer is A
1=Current destination buffer is B

Source Buffer: 0=Current source buffer is A
1=Current source buffer is B

Tile Mode Register, with Default Settings

Register Index: 05h. Register may be read and written.

7	6	5	4	3	2	1	0
RES	RES	RES	TileSrc	TileMatrix			
0	0	0	0	0h			

TileSrc: 0=TileMatrix, 1=DATA[19:16] during SYNC

TileMatrix: Inversion state of each quadrant when TileSrc = 0

Serial Row Address Registers, with default settings.

Register Index: 06h-07h. Register may be read and written

Index	Default	7	6	5	4	3	2	1	0
06h	00h	Reserved					SerialAddress[10..8]		
07h	00h	SerialAddress[7..0]							

SerialAddress: Serial Address Register, used to load Address information to either the Row Address Start Pointer, or the Current Row Address Pointer.

Serial Command Register, with default settings

Register Index: 08h. Register may be read and written.

7	6	5	4	3	2	1	0
Command Options[3:0]				Serial Command[3:0]			
0h				0h			

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Table 15: HDP-1280-2 Serial Commands

Mnemonic	Code	Function	Command Options	
			Bit	Function
PanelUpdate	0h	Update Pixels from frame buffer memory	3	Apron Polarity
			2	Data Polarity
			1	Destination Buffer[1]
			0	Source Buffer[1]
SetDestBuffer[3]	1h	Set Destination Buffer	0	Destination Buffer[1]
SetStartAddr	3h	Load Row Address Start Pointer from Serial Address		
SetCurAddr	4h	Load Current Row Address Pointer from Serial Address		
IncRowAddr	5h	Increment Row Address (Current Row Address)		
DecRowAddr	6h	Decrement Row Address (Current Row Address)		
LoadLine[2]	7h	Load a line of data from Data registers at current row address		
ReadData[2]	8h	Read current row address using serial interface		

[1] 0=Buffer A, 1=Buffer B

[2] Panel must be in the Test state to use this command

[3] The SetDestBuffer requires "Serial update mode" to be set

HDP Clock Frequency Register, with default settings.

Register Index: 09h. Register may be read and written

7	6	5	4	3	2	1	0
HDP Clock Frequency							
120d							

HDP Clock Frequency: HDP clock frequency in MHz, used to determine internal timing (Blanking interval, etc.). Note: this register needs to be set by the user to the input CLOCK frequency before the HDP is taken out of the *Sleep* state.

Row Address Start Pointer Registers, with default settings.

Register Index: 0Ah-0Bh. Registers are read only

Index	Default	7	6	5	4	3	2	1	0
0Ah	00h	Reserved					StartAddress[10..8]		
0Bh	00h	StartAddress[7..0]							

StartAddress: The Row Address Start Pointer is set serially using the SetStartAddr serial command. The Current Address Pointer will be reset to the Row Address Start Pointer when an UPDATE occurs (with page buffer toggle), either using the external signals or through the serial interface.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Current Row Address Pointer, with default settings.

Register Index: 0Ch-0Dh. Registers are read only

Index	Default	7	6	5	4	3	2	1	0
0Ch	00h	Reserved					CurrentAddress[10..8]		
0Dh	00h	CurrentAddress[7..0]							

CurrentAddress: The Current Address Pointer contains the row address of the current data transfer. A SYNC with VALID low signals that a valid row address is on the DATA bus. This address will be loaded into the Current Address Pointer. The Current Address Pointer will be incremented after each valid data line. The Current Address Pointer will not increment past 1280, and all data received after address 1279 will be ignored by the HDP.

Temperature Register, with default settings

Register Index: 13h. Register is read only.

7	6	5	4	3	2	1	0
TSENSE[7..0]							
FFh							

TSENSE: HDP offset corrected temperature, automatically updated. To convert to degrees Celsius, the following equation is used. The temperature sensor is accurate to +/- 3°C. The temperature is only continually read when the panel is being driven.

$$Temperature(^{\circ}C) = -46.261 + 0.578105 * \text{TemperatureRegisterCodeInDecimal}$$

Test Data Registers, with default settings

Register Index: 2Ch-3Bh. Registers may be read and written

Index	Default	7	6	5	4	3	2	1	0
2Ch	00h	TestData[7:0]							
2Dh	00h	TestData[15:8]							
2Eh	00h	TestData[23:16]							
2Fh	00h	TestData[31:24]							
30h	00h	TestData[39:32]							
31h	00h	TestData[47:40]							
32h	00h	TestData[55:48]							
33h	00h	TestData[63:56]							
34h	00h	TestData[71:64]							
35h	00h	TestData[79:72]							

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

36h	00h	TestData[87:80]
37h	00h	TestData[95:88]
38h	00h	TestData[103:96]
39h	00h	TestData[111:104]
3Ah	00h	TestData[119:112]
3Bh	00h	TestData[127:120]

TestData: Test data value used for LoadLine test command.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Test Read Data Register, with default settings

Register Index: 3Ch. Register is read only

7	6	5	4	3	2	1	0
Data[7:0]							
00h							

Data: 8 bits if Data read from frame buffer

* Each read of the Data Register will automatically update the register to the next 8 bits of the shift register

Hardware Configuration Register, with default settings

Register Index: 78h. Register is read only

7	6	5	4	3	2	1	0
Model[3:0]				Revision[3:0]			
2h				0h			

Model: The HDP-1280-2 is model 2h.

Revision: Revision A is 0h.

ID Code Registers, with default settings.

Register Index: 79h-7Bh. Registers are read only

Index	7	6	5	4	3	2	1	0
79h	ID Code[7:0]							
7Ah	ID Code[15:8]							
7Bh	ID Code[23:16]							

ID Code: The ID Code is programmed during manufacturing to a unique code for identification purposes. These registers should not be changed by the user to prevent loss of traceability for HDP panels.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com

Appendix C: Environmental Compliance

Table 16: Banned Substances

Substance	Threshold Level (ppm)
Lead	Per RoHS*
Mercury	Per RoHS
Cadmium	Per RoHS
Hexavalent Chromium	Per RoHS
PBDE	Per RoHS
PBB	Per RoHS

* Restriction of Hazardous Substances (EU DIRECTIVE 2002/95/EC)

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
sales@displaytech.com