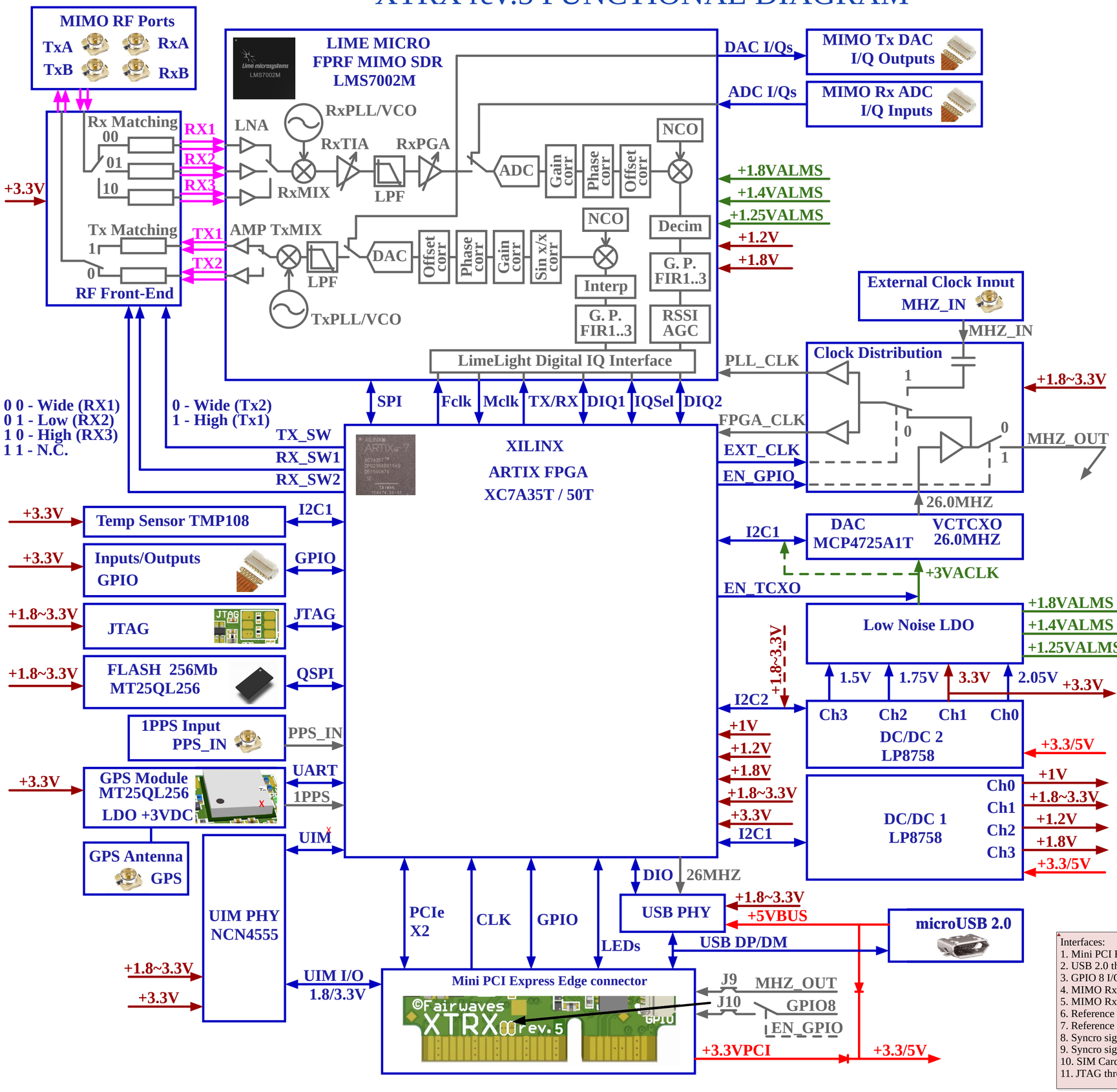
XTRX rev.5 FUNCTIONAL DIAGRAM



FPGA INNER GPIO PIN ASSIGNMENT

BANK 14 (1.83.3V)	I/O	PIN FUNCTION
E19	Out	26MHZ to USB PHY
N18	Out	LED
R19	Out	EN_TCXO LDO +3V ctrl
M18	Out	USB PHY nRESET
V17	Out	EXT_CLK Switch ctrl
U15	I/O	I2C2 SDA
U14	Out	I2C2 SCL
V14	I/O	PCB Assembly Variant Identification
D17	Out	EN_GPIO (MHz/GPIO8 switch ctrl)
T17	I/O	GPIO13 (for DAC/ADC connectors)
L18	Out	EN_GPS (GPS module/Antenna LDO ctrl)
V19	Out	VCC_SEL (BANK35 Vcc Switch ctrl)

BANK 16 (1.83.3V)		
B17, A17, B16, A16	I/O	USB PHY D0, D1, D2, D3
B15, A15, A14, C15	I/O	USB PHY D4, D5, D6, D7
C16	Out	USB PHY CLK
C17	I/O	USB PHY STP
B18	Out	USB PHY DIR
A18	Out	USB PHY NXT

BANK 34 (1.83.3V)		
R2	Out	SIM_RST
T2	I/O	SIM_DIO
R3	Out	SIM_MOD
T1	Out	SIM_CLK
U1	Out	SIM_ENA
T3	In	PCIe PERST#

BANK 35 (1.83.3V)		
M3	I/O	GPIO1 or 1_N (1PPS Ext In)
L3	I/O	GPIO2 or 1_P (1PPS Ext Out)
J2	I/O	GPIO3 or 3_N
H2	I/O	GPIO4 or 3_P (Ext TDD control)
G3	I/O	GPIO5 (LED WWAN#, need resistor)
M2	I/O	GPIO6 (LED WLAN#, need resistor)
G2	I/O	GPIO7 (LED WPAN#, need resistor)
N3	I/O	GPIO8 (to mPCIe via GPIO Switch)
J1	I/O	GPIO9 or 9_N
H1	I/O	GPIO10 or 9_P
L2	I/O	GPIO11 or 11_N
K2	I/O	GPIO12 or 11_P
L1	Int	GPS UART Rx
N2	Out	GPS UART Tx
P3	In	GPS 1PPS
N1	I/O	I2C1 SDA
M1	Out	I2C1 SCL
K3, J3	Out	Rx Band Select SW1, SW2
P1	Out	Tx Band Select SW

Interfaces:
1. Mini PCI Express 2 lanes (2nd uses reserved pins)
2. USB 2.0 through microUSB or edge connector pins
3. GPIO 8 I/Os or 4 ballanced pairs, FFC connector
4. MIMO Rx/Tx RF Inputs/Outputs, U.FL connectors
5. MIMO Rx ADC I/Q Inputs, FFC connector
6. Reference Clock Input, U.FL connector
7. Reference Clock Output, edge connector
8. Syncro signal 1PPS Input, U.FL connector
9. Syncro signal 1PPS Output, edge connector
10. SIM Card 1.8/3.3V I/O lines, edge connector
11. JTAG through board-to-board spring connector

Title	XTRX. SDR mini PCIe Transceiver.		
Size	Number		Revision 5
A2	Func Diagram.SchDoc		
Date:	06.08.2019	Fairwaves Inc.	Sheet 1 of 5
File:	C:\Git\..\Func Diagram.SchDoc		Drawn By: Andrey Sviyazov