

## LimeSDR-XTRX\_v1.3

CONTROLLED IMP	-DANCE			STACKUP	AND LAYE	R DES	SCRIPTI	UN	
GENERAL PARAI	METERS								
Parameter	Layer/Layers	Value							
Copper foil thickness	Тор	17.5um							
Dielectric thickness between layers	T 10	102um (4 mils)	1						
Dielectric permittivity between layers (Er)	Top-L2	4.2							
Copper foil thickness	Bottom	17.5um	1		Via type #2		Via type #1		
Dielectric thickness between layers		102um (4 mils)	GERBER LAYER NAMES:		<b>Micro via</b> L7-Bot		<b>d via TH via</b> Bot Top-Bo		
Dielectric permittivity between layers (Er)	Bottom-L7	4.2	GTP Top solder paste GTO Silkscreen				•		
CALCULATIONS			GTS Soldermask (halogen free) GTL 0.5oz+plating						CAL LAYERS: F/Signal/PWR/GND
			G1 1oz (35um) PP 4mil (1	17180A: 3313				L2: GNE	
Target impedance	Single-ended	50R	G2 1oz (35um) CORE 4mil (1						gnal/PWR/GND
Additional comments		side GND plane	G3 1oz (35um) PP 4.6mil					L4: Siç	gnal/PWR/GND
Top layer copper foil thickness		5um	CORE 4mil (1)  G4 1oz (35um)  PP 4.6mil					L5: GNE	D
Track width		8mm	G5 1oz (35um) = 7.5miii					L6: CLk	K/PWR/GND
Distance to reference plane  Dielectric thickness between lawers		3h	G6 1oz (35um) = 00K2					L7: GNE	
Dielectric trickress between ragers	Top-L2	102um (4 mils)	GBL 0.5oz+plating GBS Soldermask (halogen free)						RF/Signal/PWR/GND
Dielectric permittivity between layers (Er)		4.2	GBO Silkscreen  GBP Bottom solder paste						IONAL LAYERS:  thanical 1: Board cutout
Approximate microstrip line impedance		10% tolerance>		knes: 1mm +/- 10%	0.15mm drill 0.5mm ring	0.2mm 0.35mm	drill 0.2mm dri ring 0.35mm ri	ill ing ASM	TOP: Assembly top
Target impedance	Differential	100R	_		H via type must be	resin fi	lled with meta	al cap ASM	BOT: Assembly bottom thanical 13: Component 3D bo
Additional comments	Top layer, no	side GND plane	_		lind and micro via opper	type can	be coated wi	t h	es: Board shape and frame
Top layer copper foil thickness	17.	5um							
Track width	O.1 mm (3	3.93 mils>	_						
Track spacing	O.1 mm (3	3.93 mils>							
Distance to reference plane	>:	3h							
Dielectric thickness between layers	Top-L2	102um (4 mils)							
Dielectric permittivity between layers (Er)		4.2							
Approximate microstrip line impedance	100 Ohms (+/-	10% tolerance)	_						
Approximate microstrip line impedance  Target impedance	100 Ohms (+/- Single-ended	10% tolerance) 50R							
	Single-ended								
Target impedance	Single-ended Bottom layer, no	50R			Y IMDODTA	NT N	NTFS		
Target impedance Additional comments  Top layer copper foil thickness	Single-ended  Bottom layer, no	50R o side GND plane			Y IMPORTA	NT N			
Target impedance Additional comments	Single-ended  Bottom layer, no  17.5	50R o side GND plane 5 um	GENERAL	VER PCB SPECS	YIMPORTA	ANT N		DDITIONAL	REQUIREMENTS
Target impedance Additional comments  Top layer copper foil thickness  Track width	Single-ended  Bottom layer, no  17.5  O.1	50R o side GND plane 5 um .8mm	GENERAL Minimum copper to copper spacing	PCB SPECS	Y IMPORTA (3.9mil)	A11 0.	2mm vias incl	uding 0.35mm	m ring and O.2mm drill via-i
Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane	Single-ended  Bottom layer, no  17.5	50R o side GND plane 5 um .8mm		PCB SPECS O.1mm (		A11 0.	2mm vias incl	uding 0.35mm	
Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers	Single-ended  Bottom layer, no  17.5  O.1  Single-ended  17.5  O.1	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2	Minimum copper to copper spacing	PCB SPECS  O.1mm ( O.1mm (	(3.9mil)	• All O. (IC1 a	2mm vias incluand IC7) must l	uding 0.35mm be resin fil	m ring and O.2mm drill via-in
Target impedance  Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, no  17.5  O.1  Single-ended  17.5  O.1	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2	Minimum copper to copper spacing Minimum track width  PCB thickness	PCB SPECS  O.1mm (  O.1mm (  1mm +  IT-180A preferred	(3.9mil) (3.9mil) /-10% or equivalent	All O. (IC1 a	2mm vias incluand IC7) must learned pad via	uding 0.35mm be resin fil	m ring and O.2mm drill via-i
Target impedance  Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance	Single-ended  Bottom layer, no  17.5  0.1  Single-ended  17.5  O.1  Differential	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance)	Minimum copper to copper spacing  Minimum track width	PCB SPECS  O.1mm ( O.1mm (  1mm +	(3.9mil) (3.9mil) /-10% or equivalent	All O. (IC1 a	2mm vias incluand IC7) must be nermal pad via filled with me and 0.2mm dril	uding 0.35mm be resin files with 0.4mm etal cap. IC	m ring and O.2mm drill via-in lled with metal cap. m ring and O.2mm drill must I thermal pad vias with O.5 eft open (NO resin fill with
Target impedance  Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance  Target impedance	Single-ended  Bottom layer, no  17.5  0.1  Single-ended  17.5  O.1  Political  Top/Bottom laye	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material	PCB SPECS  O.1mm (  O.1mm (  1mm +  IT-180A preferred RF-rated material	(3.9mil) (3.9mil) /-10% or equivalent	All O. (IC1 a	2mm vias incluand IC7) must described with me	uding 0.35mm be resin files with 0.4mm etal cap. IC	m ring and O.2mm drill via-in lled with metal cap. m ring and O.2mm drill must I thermal pad vias with O.5 eft open (NO resin fill with
Target impedance Additional comments  Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments  Top layer copper foil thickness	Single-ended  Bottom layer, no  17.5  O.1  Single-ended  17.5  O.1  Page 17.5  All Page 17.5  All Page 17.5	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND	Minimum copper to copper spacing Minimum track width  PCB thickness	PCB SPECS  O.1mm (  O.1mm (  1mm +  IT-180A preferred  RF-rated material  higher)	(3.9mil) (3.9mil) (7-10% or equivalent (up to 3 GHz or	All O. (IC1 at resin ring a cap).	2mm vias incluand IC7) must described with meand 0.2mm dril 4 vias in total	uding 0.35mm be resin files with 0.4mm etal cap. IC l must be leal, marked was	m ring and O.2mm drill via-index led with metal cap.  m ring and O.2mm drill must in the cap in the cap in the cap. It with o.5 with o.5 with o.5 with note.
Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance  Target impedance  Additional comments  Top layer copper foil thickness  Track width	Single-ended  Bottom layer, no  17.5  O.1  Single-ended  17.5  O.1  Political  Top/Bottom laye  17.5  O.14 mm (	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material	PCB SPECS  O.1mm ( O.1mm (  1mm +  IT-180A preferred RF-rated material higher)  External layer  Internal layer	(3.9mil) (3.9mil) (7-10% or equivalent (up to 3 GHz or  0.5 oz+plating	All O. (IC1 at resin ring a cap).	2mm vias incluand IC7) must be nermal pad via filled with me and 0.2mm dril	uding 0.35mm be resin files with 0.4mm etal cap. IC l must be leal, marked was	m ring and O.2mm drill via-index led with metal cap.  m ring and O.2mm drill must in the cap in the cap in the cap. It with o.5 with o.5 with o.5 with note.
Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance  Target impedance  Additional comments  Top layer copper foil thickness  Track width	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um (5.5 mils)	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight	PCB SPECS  O.1mm (  O.1mm (  1mm +  IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK	(3.9mil) (3.9mil) (7-10% or equivalent (up to 3 GHz or  0.5 oz+plating  1 oz	All O. (IC1 and resin ring a cap).	2mm vias incluand IC7) must defilled with meand 0.2mm dril 4 vias in total	uding 0.35mm be resin file  s with 0.4mm etal cap. IC l must be lo al, marked of	m ring and 0.2mm drill via-index with metal cap.  m ring and 0.2mm drill must cap thermal pad vias with 0.5 eft open (NO resin fill with with note.
Target impedance Additional comments  Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  >3	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils)	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm ( O.1mm (  1mm +  IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both	(3.9mil) (3.9mil) (7-10% or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE	All O. (IC1 and resin ring a cap).	2mm vias incluand IC7) must described with meand 0.2mm dril 4 vias in total	uding 0.35mm be resin file  s with 0.4mm etal cap. IC l must be lo al, marked of	m ring and 0.2mm drill via-index with metal cap.  m ring and 0.2mm drill must cap thermal pad vias with 0.5 eft open (NO resin fill with with note.
Target impedance Additional comments  Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ors, no side GND 5 um (5.5 mils) 3.93 mils)	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm ( O.1mm (  1mm +  IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge	(3.9mil) (3.9mil) (7-10% or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides	All O. (IC1 and resin ring a cap).  • Electrical PCB visits and ring a cap a c	2mm vias included IC7) must be and IC7) must be and 0.2mm dril 4 vias in total test: 10 sare to be intended to silks	uding 0.35mm be resin file  s with 0.4mm etal cap. IC  l must be le al, marked we  ndividually  screen UL ar	m ring and 0.2mm drill via-incled with metal cap.  m ring and 0.2mm drill must C1 thermal pad vias with 0.5 eft open (NO resin fill with with note.  bagged.  nd RoHS compliance marks, ve
Target impedance Additional comments  Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane Dielectric thickness between layers	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)  Top-L2  Bottom-L7	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3h	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm (  O.1mm (  1mm +  IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge  Glossy finish	(3.9mil) (3.9mil) (7-10% or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides en free	All O. (IC1 a  IC1 th resin ring a cap).  Board  PCB va logo a	2mm vias included IC7) must be and IC7) must be and 0.2mm dril 4 vias in total test: 10 sare to be intended to silks	uding 0.35mm be resin file as with 0.4mm etal cap. IC l must be le al, marked u  ndividually screen UL ar on bottom w	m ring and 0.2mm drill via-index with metal cap.  m ring and 0.2mm drill must cap with 0.5 with 0.5 with 0.5 with open (NO resin fill with with note.
Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance  Target impedance  Additional comments  Top layer copper foil thickness  Track width  Track spacing  Distance to reference plane  Dielectric thickness between layers  Dielectric thickness between layers  Dielectric permittivity between layers  Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)  Top-L2  Bottom-L7	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3h 173um (6.8 mils) 4.2	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm ( O.1mm (  1mm +  IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge  Glossy finish  White ep	(3.9mil) (3.9mil) (7-10% or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides en free h (NOT matte)	All O. (IC1 a  IC1 th resin ring a cap).  Board  PCB va logo a info u Assem	2mm vias included IC7) must be filled with me and 0.2mm dril 4 vias in total test: 10 s are to be intended and date code will be placed bly note: Asset	uding 0.35mm be resin file as with 0.4mm etal cap. IC l must be le al, marked contained creen UL and on bottom we on PCB) embly house	m ring and 0.2mm drill via-incled with metal cap.  m ring and 0.2mm drill must continued thermal pad vias with 0.5 eft open (NO resin fill with with note.  bagged.  d RoHS compliance marks, verallers shown (ignore if none MUST provide notes in paper
Target impedance Additional comments Top layer copper foil thickness Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance Target impedance Additional comments Top layer copper foil thickness Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric thickness between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)  Top-L2  Bottom-L7	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3h 173um (6.8 mils) 4.2	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm ( O.1mm (  Imm +  IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge  Glossy finish  White ep	(3.9mil) (3.9mil) (7-10% or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides en free h (NOT matte) poxy ink	All O. (IC1 a  IC1 th resin ring a cap).  Board  PCB v logo a info u Assem shippe	2mm vias included IC7) must be and IC7) must be and 0.2mm dril 4 vias in total test: 10 and date code will be placed bly note: Assembled board if the and date code will be placed bly note: Assembled board if the and if t	uding 0.35mm be resin file as with 0.4mm etal cap. IC. I must be le al, marked of al, marked of creen UL ar on bottom w on PCB) embly house here were an	m ring and 0.2mm drill via-incled with metal cap.  m ring and 0.2mm drill must continued the continu
Target impedance Additional comments  Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments  Top layer copper foil thickness  Track width  Track spacing Distance to reference plane Dielectric thickness between layers  Dielectric thickness between layers  Dielectric permittivity between layers  Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)  Top-L2  Bottom-L7	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3h 173um (6.8 mils) 4.2	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm ( O.1mm (  Imm +  IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge  Glossy finish  White ep	(3.9mil) (3.9mil) (7-10% or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides en free h (NOT matte) poxy ink sides en free	All O. (IC1 a  IC1 th resin ring a cap).  Board  PCB v logo a info u Assem shippe board	2mm vias incluand IC7) must hermal pad via filled with me and 0.2mm dril 4 vias in total test: 10 sare to be in endor to silks and date code will be placed bly note: Assemble bly note assemble example:	uding 0.35mm be resin file as with 0.4mm etal cap. IC l must be le al, marked a  on bottom we on PCB) embly house here were and oled 100% ac	m ring and 0.2mm drill via-incled with metal cap.  m ring and 0.2mm drill must continued thermal pad vias with 0.5 eft open (NO resin fill with with note.  bagged.  d RoHS compliance marks, verallers shown (ignore if none MUST provide notes in paper
Target impedance Additional comments Top layer copper foil thickness Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance Target impedance Additional comments Top layer copper foil thickness Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric thickness between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)  Top-L2  Bottom-L7	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3h 173um (6.8 mils) 4.2	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm ( O.1mm (  Imm +  IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge  Glossy finish  White ep  Both  Haloge	(3.9mil) (3.9mil) (7-10% or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides en free h (NOT matte) poxy ink sides en free	All O. (IC1 a  IC1 th resin ring a cap).  Board  PCB v logo a info u Assem shippe board	2mm vias included IC7) must be and IC7) must be and 0.2mm dril 4 vias in total test: 10 and date code will be placed bly note: Assembled board if the is not assembled.	uding 0.35mm be resin file  s with 0.4mm etal cap. IC  l must be le al, marked of  ndividually  screen UL and on bottom we on PCB)  embly house here were and oled 100% according to the content of the c	m ring and 0.2mm drill via-incled with metal cap.  m ring and 0.2mm drill must on the cap of the ca
Target impedance Additional comments Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric thickness between layers Dielectric permittivity between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)  Top-L2  Bottom-L7	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3h 173um (6.8 mils) 4.2 10% tolerance)	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm ( O.1mm ( Imm + IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge  Glossy finish  White ep  Both  Haloge  No silkscree	3.9mil) 3.9mil) 7-10% or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides on free ch (NOT matte) poxy ink sides on free cen on pads Non-plated are final ameters INCLUDING	All O. (IC1 a  IC1 th resin ring a cap).  Board PCB v logo a info a Assem shippe board Note a Part	2mm vias included IC7) must be and IC7) must be and 0.2mm dril 4 vias in total test: 10 and date code will be placed bly note: Assembled board if the is not assemble and lateral test in IC4 assemble and lateral test is not assemble and lateral BOM	uding 0.35mm be resin file  s with 0.4mm etal cap. IC  l must be le al, marked of  ndividually  screen UL and on bottom we on PCB)  embly house here were and oled 100% according to the content of the c	m ring and 0.2mm drill via-incled with metal cap.  m ring and 0.2mm drill must on the cap of the ca
Target impedance Additional comments  Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments  Top layer copper foil thickness  Track width  Track spacing Distance to reference plane Dielectric thickness between layers  Dielectric thickness between layers  Dielectric permittivity between layers  Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)  Top-L2  Bottom-L7	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3h 173um (6.8 mils) 4.2 10% tolerance)	Minimum copper to copper spacing Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask  Silkscreen	O.1mm ( O.1mm ( O.1mm (  IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge  Glossy finish  White ep  Both  Haloge  No silkscree  Plated  Hole diameters  manufactured diameters	3.9mil) 3.9mil) 7-10% or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides on free ch (NOT matte) poxy ink sides on free cen on pads Non-plated are final ameters INCLUDING ON.  Tab route	All O. (IC1 and resin ring a cap).  Electron  PCB voltage info to a shippe board Note a part R1 IC5	A 2mm vias included IC7) must be and IC7) must be and 0.2mm dril 4 vias in total test: 10 sare to be incended by note: Assemble and date code by note: Assemble and the assemble assemb	uding 0.35mm be resin file  as with 0.4mm etal cap. IC  I must be lead, marked undividually  screen UL and on bottom whom PCB  embly housemere were and oled 100% accompled	m ring and 0.2mm drill via-incled with metal cap.  m ring and 0.2mm drill must class and the class with 0.5 eft open (NO resin fill with with note.  bagged.  d RoHS compliance marks, vershere shown (ignore if none of the compliance marks) are cording to BOM and P&P file comment.  Not mounted due to bad foo
Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance  Target impedance  Additional comments  Top layer copper foil thickness  Track width  Track spacing  Distance to reference plane  Dielectric thickness between layers  Dielectric thickness between layers  Dielectric permittivity between layers  Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)  Top-L2  Bottom-L7	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3h 173um (6.8 mils) 4.2 10% tolerance)	Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask  Silkscreen  Hole types on the PCB and informat:	PCB SPECS  O.1mm ( O.1mm (  1mm +  IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge  Glossy finish  White ep  Both  Haloge  No silkscree  Plated  Hole diameters  manufactured diameters	3.9mil) 3.9mil) 7-10% or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides on free ch (NOT matte) poxy ink sides on free cen on pads Non-plated are final ameters INCLUDING ON.  Tab route	All O. (IC1 a  IC1 the resin ring a cap).  Electrical ring a cap).  Board  PCB visual ring a cap).  Assemble board Note a cap ring a	2mm vias included IC7) must be and IC7) must be and 0.2mm dril 4 vias in total test: 10 and date code will be placed bly note: Assemble and the assemble ass	uding 0.35mm be resin file  as with 0.4mm etal cap. IC. I must be lead, marked of  on bottom won PCB)  embly house here were and oled 100% accompled 100% ac	m ring and 0.2mm drill via-incled with metal cap.  m ring and 0.2mm drill must on the cap of the ca
Target impedance Additional comments  Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric thickness between layers Dielectric permittivity between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)  Top-L2  Bottom-L7	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3h 173um (6.8 mils) 4.2 10% tolerance)	Minimum copper to copper spacing Minimum track width PCB thickness  PCB material  Copper weight  Solder mask  Silkscreen  Hole types on the PCB and informat: Route process  Panel	O.1mm ( O.1mm ( O.1mm ( Imm + IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge  Glossy finish  White ep  Both  Haloge  No silkscre  Plated  Plated  One  Hole diameters  manufactured diameters  manufactured diameters  Tyes  HASL lead free  HASL lead free  HASL with lead	(3.9mil) (3.9mil) (7.10%  or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides en free h (NOT matte) poxy ink sides en free een on pads Non-plated are final ameters INCLUDING ON.  Tab route  Oute  No	All O. (IC1 a  IC1 th resin ring a cap).  Board  PCB va logo a info a Assem shippe board Note a  Part  R1 IC5  PCIe a micro  PCIe a chamfe	And IC7) must be and IC7) must be and 0.2mm dril 4 vias in total test: 10 and date code will be placed bly note: Assemble and the assemble	uding 0.35mm be resin file  as with 0.4mm etal cap. IC. I must be leal, marked us  on with 0.4mm etal cap. IC. I must be leal, marked us  on bottom us on PCB) embly house here were and oled 100% acc  Current PCB status  NF NF NF  I: PCI EXPRE d over 50 m  2: Board edo n). Edges must  2: Board edo n). Edges must	m ring and 0.2mm drill via-incled with metal cap.  m ring and 0.2mm drill must on the cap with 0.5 and the cap with 0.5 and cap with 0.5 and cap with note.  bagged.  md RoHS compliance marks, very bare shown (ignore if none of the cap with
Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance  Target impedance  Additional comments  Top layer copper foil thickness  Track width  Track spacing  Distance to reference plane  Dielectric thickness between layers  Dielectric thickness between layers  Dielectric permittivity between layers  Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, no  17.5  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom laye  17.5  O.14 mm (3)  O.1 mm (3)  Top-L2  Bottom-L7	50R o side GND plane 5 um 8mm 3h 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3h 173um (6.8 mils) 4.2 10% tolerance)	Minimum copper to copper spacing Minimum track width PCB thickness  PCB material  Copper weight  Solder mask  Silkscreen  Hole types on the PCB and informat: Route process	O.1mm ( O.1mm ( O.1mm ( Imm + IT-180A preferred RF-rated material higher)  External layer  Internal layer  DARK  Both  Haloge  Glossy finish  White ep  Both  Haloge  No silkscree  Plated  Plated  On Hole diameters  manufactured diameters	(3.9mil) (3.9mil) (7.10%  or equivalent (up to 3 GHz or  0.5 oz+plating 1 oz  BLUE sides en free h (NOT matte) poxy ink sides en free een on pads Non-plated are final ameters INCLUDING ON.  Tab route  Oute  No	All O. (IC1 a  IC1 th resin ring a cap).  Board  PCB va logo a info a Assem shippe board Note a  Part  R1 IC5  PCIe a micro  PCIe a chamfe	And IC7) must be and IC7) must be and 0.2mm dril 4 vias in total test: 10 and date code will be placed bly note: Assemble and the assemble	uding 0.35mm be resin file  as with 0.4mm etal cap. IC. I must be leal, marked us  on with 0.4mm etal cap. IC. I must be leal, marked us  on bottom us on PCB) embly house here were and oled 100% acc  Current PCB status  NF NF NF  I: PCI EXPRE d over 50 m  2: Board edo n). Edges must  2: Board edo n). Edges must	m ring and 0.2mm drill via—in led with metal cap.  m ring and 0.2mm drill must it thermal pad vias with 0.5 eft open (NO resin fill with with note.  bagged.  d RoHS compliance marks, very here shown (ignore if none of the mode)  MUST provide notes in paper my changes during assembly a coording to BOM and P&P file  Comment  Not mounted due to bad foo Not mounted due to part shown increased in paper and the mounted due to part should be not to inches nickel plating ge below PCI pads must be ust be free of cutting burrs



