

CONTROLLED IMPEDANCE

LimeSDR-XTRX_v1.0

STACKUP AND LAYER DESCRIPTION

CONTROLLED IN		JIIICKOF		.R DL	SCRIF IION					
GENERAL PARAMETERS										
Parameter Layer/Layers Value		1								
Copper foil thickness	Тор	17.5um	1							
Dielectric thickness between layers	<u>'</u>	102um (4 mils)	-							
Dielectric permittivity between layers (Er)	Top-L2	4.2	1							
Copper foil thickness	Pottom	17.5um	-		Via type #2		Via type #1			
	Bottom		GERBER LAYER NAMES:		Micro via		d via TH via			
Dielectric thickness between layers	Bottom-L7	102um (4 mils)	GTP Top solder paste		L7-Bot		Bot Top-Bot			
Dielectric permittivity between layers (Er)		4.2	GTO Silkscreen GTS Soldermask (halogen free)				E	ELECTRIC	AL LAYERS:	
CALCULATIONS			GTL 0.5oz+plating	(102um) IT180A: 3313				Top: RF/	/Signal/PWR/GND	
Target impedance	Single-ended	50R	G1 1oz (35um)	(102um) IT180A: 3313				L2: GND		
Additional comments	Top layer, no	side GND plane		l (117um) IT180A: 2116			_	_	nal/PWR/GND	
Top layer copper foil thickness	17.5um			(102um) IT180A: 3313			_		nal/PWR/GND	
Track width	O.18mm		PP 4.6mi]	G4 1oz (35um) PP 4.6mil (117um) IT180A: 2116 C5 1oz (35um) L6: CLK/PWR/GND						
Distance to reference plane	+	3h	CORE 4mil 0	(102um) IT180A: 3313			_			
<u> </u>		102um (4 mils)		(102um) IT180A: 3313			_	L7: GND		
bretectife thickness between ragers	Top-L2		GBL 0.5oz+plating GBS Soldermask (halogen free)						RF/Signal/PWR/GND ONAL LAYERS:	
Dielectric permittivity between layers (Er)		4.2	GBO Silkscreen GBP Bottom solder paste						anical 1: Board cutout	
Approximate microstrip line impedance	+	10% tolerance)		icknes: 1mm +/- 10%	0.15mm dril 0.5mm ring		drill 0.2mm drill n ring 0.35mm ring	ASM	TOP: Assembly top	
Target impedance	Differential	100R	_	Ųi	ia types #1 and #2		lled with metal cap		BOT: Assembly bottom anical 13: Component 3D body	
Additional comments	Top layer, no	side GND plane							s: Board shape and frame	
Top layer copper foil thickness	17.	5um								
Track width	O.1 mm (3	3.93 mils>								
Track spacing	O.1 mm <3	3.93 mils>	1							
Distance to reference plane	>:	3h	1							
Dielectric thickness between layers		102um (4 mils)	1							
Dielectric permittivity between layers (Er)	Top-L2	4.2	1							
	100 Ohne (+		-							
Approximate microstrip line impedance	<u> </u>	10% tolerance)	-							
Target impedance	Single-ended	50R	-							
Additional comments		o side GND plane								
Top layer copper foil thickness	17.	5 um	VERY IMPORTANT NOTES							
Track width	O.18mm									
Distance to reference plane	>:	3h	GENERA	AL PCB SPECS			ADDITI	IONAL R	EQUIREMENTS	
Dielectric thickness between layers	Dotton 17	102um (4 mils)	Minimum copper to copper spacing	O.1mm <	O.1mm (3.9mil) O.1mm (3.9mil)				g 0.35mm ring and 0.2mm drill via-in-pads	
Dielectric permittivity between layers (Er)	Bottom-L7	4.2	Minimum track width	O.1mm <			(IC1 and IC7) must be resin filled with metal cap.			
Approximate microstrip line impedance	49.99 Ohms (+/-	- 10% tolerance)	PCB thickness	1mm +	·/-10%					
Target impedance	Differential	85R		·	IT-180A preferred or equivalent		IC1 thermal pad vias with 0.4mm ring and 0.2mm drill must be resin filled with metal cap. IC1 thermal pad vias with 0.5m			
Additional comments		rs, no side GND	- PCB material	RF-rated material higher)	(up to 3 GHz or	ring and 0.2mm drill must be left open (NO resin fill with me			ft open (NO resin fill with metal	
Top layer copper foil thickness		j um	 	External layer	0.5 oz+plating	cap).	4 vias in total, ma	narked wi	ith note.	
			Copper weight	Internal layer		 				
Track width		(5.5 mils)	-		1 oz	• Electrical test : 100 % netlist.				
Track spacing	0.1 mm (3.93 mils) >3h		-		DARK BLUE					
Distance to reference plane			- Solder mask		Both sides		 Boards are to be individually bagged. 		agged.	
Dielectric thickness between layers	Top-L2	173um (6.8 mils)			Halogen free					
Dielectric permittivity between layers (Er)	Bottom-L7	4.2		Glossy finis	Glossy finish (NOT matte)		PCB vendor to silkscreen UL and RoHS compliance marks, vendor • logo and date code on bottom where shown (ignore if none of the			
Approximate microstrip line impedance	85 Ohms (+/- 10% tolerance)			White e	White epoxy ink		info will be placed on PCB)			
			Silkeeroop	Both	Both sides				MUST provide notes in paper with	
			Silkscreen	Haloge	Halogen free			changes during assembly and the rding to BOM and P&P files.		
				No silkscre	No silkscreen on pads Plated 🗙 Non-plated 💢		example:			
				Plated 🔀			Initial BOM Cur asm. note PCB	Current CB status Comment		
			Hole types on the PCB and informa				 		Not mounted due to bad footprint	
				• manufactured di HOLE METALIZATI	ameters INCLUDING	R1 IC5			Not mounted due to part shortage	
						500	DEOLITECTION TO THE			
	Route process		V-score			I EXPRESS pads (top and bottom) - 30 er 50 micro inches nickel plating				
To the second se			D = = 1		V-score and tab route		micro inches of gold over 50 micro inches nickel plating			
			Panel	Yes	No 🔀			_	below PCI pads must be	
				HASL lead free		Chamt	ereu (as snown). Eo	uyes mus	t be free of cutting burrs	
				HASL with lead	HASL with lead Immersion gold 0.05-0.10um of gold over 2.50-5.00um of nickel		● PCIe REQUIREMENT #3: PCIe finger leader lines are acceptable			
			Surface finish (both sides)	Immersion gold 0.05						
				OSP						
				Hard gold PCIe fing	jers 🔀					



