# LimeSDR-XTRX_v1.3

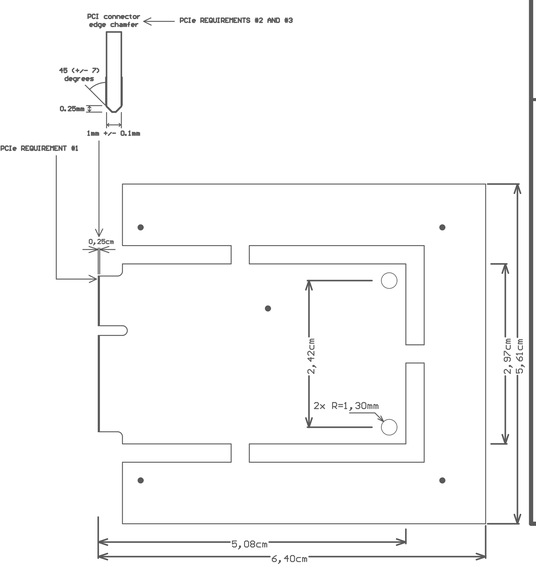
## CONTROLLED IMPEDANCE

GENERAL PARAMETERS

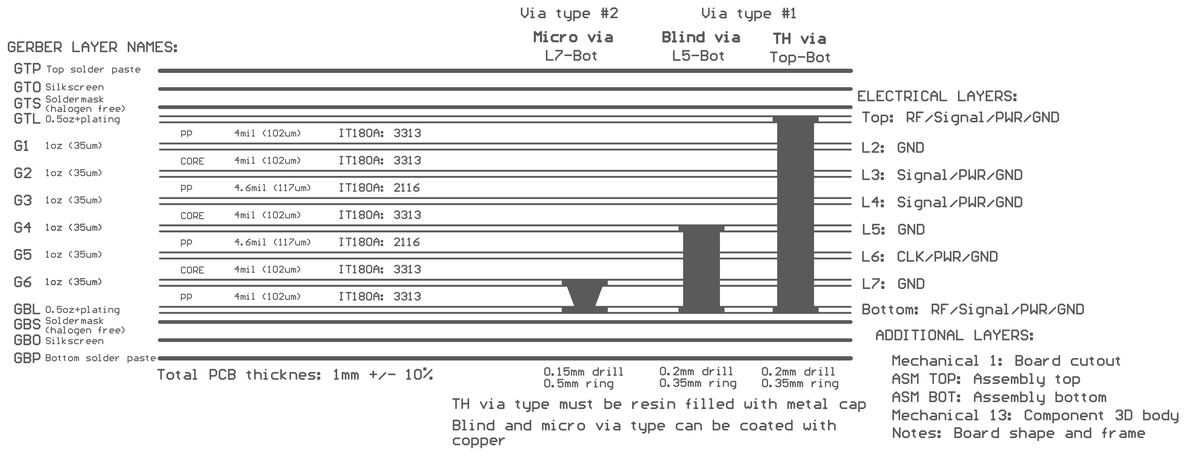
| Parameter | Layer/Layers | Value |
|---|---|---|
| Copper foil thickness | Top | 17.5um |
| Dielectric thickness between layers | Top-L2 | 102um (4 mils) |
| Dielectric permittivity between layers (Er) | | 4.2 |
| Copper foil thickness | Bottom | 17.5um |
| Dielectric thickness between layers | Bottom-L7 | 102um (4 mils) |
| Dielectric permittivity between layers (Er) | | 4.2 |

CALCULATIONS

| | | | |
|---|---|---|---|
| RF (Top) | Target impedance | Single-ended | 50R |
| | Additional comments | Top layer, no side GND plane | |
| | Top layer copper foil thickness | 17.5um | |
| | Track width | 0.18mm | |
| | Distance to reference plane | >3h | |
| | Dielectric thickness between layers | Top-L2 | 102um (4 mils) |
| | Dielectric permittivity between layers (Er) | | 4.2 |
| | Approximate microstrip line impedance | 50 Ohms (+/- 10% tolerance) | |
| RF (Top) | Target impedance | Differential | 100R |
| | Additional comments | Top layer, no side GND plane | |
| | Top layer copper foil thickness | 17.5um | |
| | Track width | 0.1 mm (3.93 mils) | |
| | Track spacing | 0.1 mm (3.93 mils) | |
| | Distance to reference plane | >3h | |
| | Dielectric thickness between layers | Top-L2 | 102um (4 mils) |
| | Dielectric permittivity between layers (Er) | | 4.2 |
| | Approximate microstrip line impedance | 100 Ohms (+/- 10% tolerance) | |
| RF (Bottom) | Target impedance | Single-ended | 50R |
| | Additional comments | Bottom layer, no side GND plane | |
| | Top layer copper foil thickness | 17.5 um | |
| | Track width | 0.18mm | |
| | Distance to reference plane | >3h | |
| | Dielectric thickness between layers | Bottom-L7 | 102um (4 mils) |
| | Dielectric permittivity between layers (Er) | | 4.2 |
| | Approximate microstrip line impedance | 49.99 Ohms (+/- 10% tolerance) | |
| PCIe (Top and Bottom) | Target impedance | Differential | 85R |
| | Additional comments | Top/Bottom layers, no side GND | |
| | Top layer copper foil thickness | 17.5 um | |
| | Track width | 0.14 mm (5.5 mils) | |
| | Track spacing | 0.1 mm (3.93 mils) | |
| | Distance to reference plane | >3h | |
| | Dielectric thickness between layers | Top-L2<br>Bottom-L7 | 173um (6.8 mils) |
| | Dielectric permittivity between layers (Er) | | 4.2 |
| | Approximate microstrip line impedance | 85 Ohms (+/- 10% tolerance) | |




## STACKUP AND LAYER DESCRIPTION




## VERY IMPORTANT NOTES

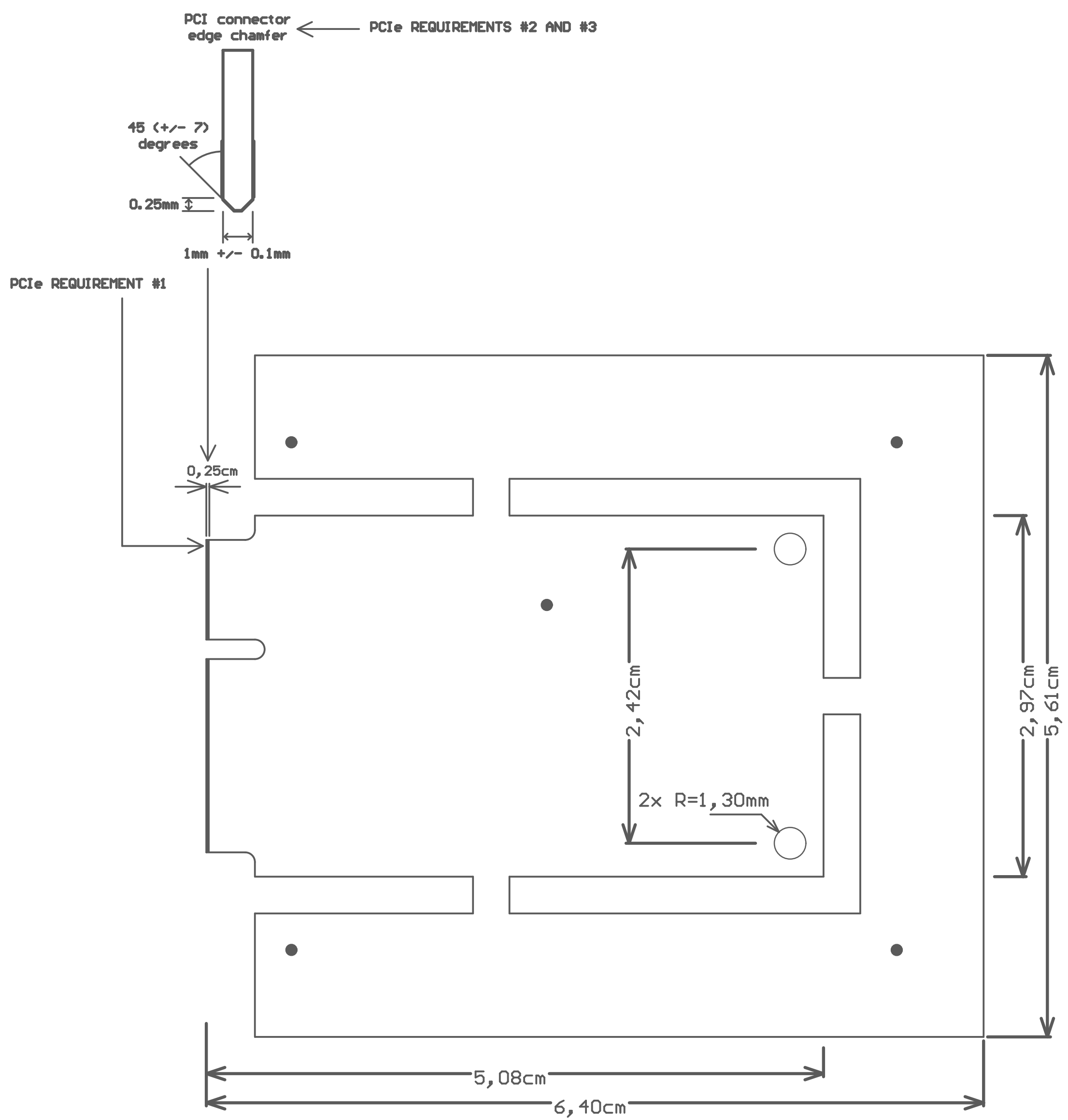
| GENERAL PCB SPECS | | |
|---|---|---|
| Minimum copper to copper spacing | 0.1mm (3.9mil) | |
| Minimum track width | 0.1mm (3.9mil) | |
| PCB thickness | 1mm +/-10% | |
| PCB material | IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher) | |
| Copper weight | External layer | 0.5 oz+plating |
| | Internal layer | 1 oz |
| Solder mask | DARK BLUE | |
| | Both sides | |
| | Halogen free | |
| | Glossy finish (NOT matte) | |
| Silkscreen | White epoxy ink | |
| | Both sides | |
| | Halogen free | |
| | No silkscreen on pads | |
| Hole types on the PCB and information | Plated ☒ | Non-plated ☒ |
| | ● Hole diameters are final manufactured diameters INCLUDING HOLE METALIZATION. | |
| Route process | V-score ☐ | Tab route ☒ |
| | V-score and tab route ☐ | |
| Panel | Yes ☐ | No ☒ |
| Surface finish (both sides) | HASL lead free ☐ | |
| | HASL with lead ☐ | |
| | Immersion gold 0.05-0.10um of gold over 2.50-5.00um of nickel ☒ | |
| | OSP ☐ | |
| | Hard gold PCIe fingers ☒ | |

ADDITIONAL REQUIREMENTS

- All 0.2mm vias including 0.35mm ring and 0.2mm drill via-in-pads (IC1 and IC7) must be resin filled with metal cap.
- IC1 thermal pad vias with 0.4mm ring and 0.2mm drill must be resin filled with metal cap. IC1 thermal pad vias with 0.5mm ring and 0.2mm drill must be left open (NO resin fill with metal cap). 4 vias in total, marked with note.
- Electrical test : 100 % netlist.
- Boards are to be individually bagged.
- PCB vendor to silkscreen UL and RoHS compliance marks, vendor logo and date code on bottom where shown (ignore if none of the info will be placed on PCB)
- Assembly note: Assembly house MUST provide notes in paper with shipped board if there were any changes during assembly and the board is not assembled 100% according to BOM and P&P files.
  Note example:

| Part | Initial BOM asm. note | Current PCB status | Comment |
|---|---|---|---|
| R1 | FIT | NF | Not mounted due to bad footprint |
| IC5 | FIT | NF | Not mounted due to part shortage |

- PCIe REQUIREMENT #1: PCI EXPRESS pads (top and bottom) - 30 micro inches of gold over 50 micro inches nickel plating
- PCIe REQUIREMENT #2: Board edge below PCI pads must be chamfered (as shown). Edges must be free of cutting burrs
- PCIe REQUIREMENT #3: PCIe finger leader lines are acceptable
- Blind vias can be coated with copper


PCI connector
edge chamfer
PCIe REQUIREMENTS #2 AND #3
45 (+/- 7)
degrees
0.25mm
1mm +/- 0.1mm
PCIe REQUIREMENT #1
0,25cm
2,42cm
2x R=1,30mm
2,97cm
5,61cm
5,08cm
6,40cm