

## LimeSDR-XTRX\_v1.2

	CONTROLLED IMPI	EDANCE			STACKUP AND LAYE	ER DES	SCRIPTION	N	
	GENERAL PARAI	METERS							
	Parameter	Layer/Layers	Value	1					
Copi	per foil thickness	Тор	17.5um	1					
Diel	ectric thickness between layers		102um (4 mils)	1					
Diel	ectric permittivity between layers (Er)	Top-L2	4.2	1					
Сорі	per foil thickness	Bottom	17.5um	1	Via type #2		Via type #1		
Diel	ectric thickness between layers		102um (4 mils)	GERBER LAYER NAMES:	Micro via L7-Bot		d via TH via Bot Top-Bot		
Diel	ectric permittivity between layers (Er)	Bottom-L7	4.2	GTP Top solder paste GTO Silkscreen				— — <sub>ELECTDIA</sub>	CAL LAYERS:
Г	CALCULATIONS			GTS Soldermask (halogen free) GTL 0.5oz+plating					Signal/PWR/GND
$\vdash$	Target impedance	Single-ended	50R	G1 1oz (35um) PP 4mil (102)				= L2: GND	
	Additional comments		side GND plane	G2 1oz (35um) CORE 4mil (102c) PP 4.6mil (11				= L3: Sig	nal/PWR/GND
	Top layer copper foil thickness		.5um	G3 1oz (35um) CORE 4mil (102)				= L4: Sig	nal/PWR/GND
go	Track width		18mm	G4 1oz (35um) — — — — — — — — — — — — — — — — — — —	117um) IT180A: 2116		_	= L5: GND	
	Distance to reference plane		>3h	G5 1oz (35um)  CORE 4mil (102)  G6 1oz (35um)	2um) IT180A: 3313		_	= L6: CLK	
<b>L</b>	Dielectric thickness between layers		102um (4 mils)	GBL 0.5oz+plating ————————————————————————————————————	2um) IT180A: 3313		_	= L7: GND - Bottom:	RF/Signal/PWR/GND
	Dielectric permittivity between layers (Er)	Top-L2	4.2	GBS Soldermask (halogen free) GBO Silkscreen					IONAL LAYERS:
	Approximate microstrip line impedance	50 Nhms (+/-	10% tolerance)	GBP Bottom solder paste	knes: 1mm +/- 10% 0.15mm dril	11 0 2 ~~	drill 0.2mm drill	<b>-</b> Mech	hanical 1: Board cutout
$\vdash$	Target impedance	Differential	100R	Total PCB thick	0.5mm ring	0.35mm	ring 0.35mm ring	HSM	TOP: Assembly top BOT: Assembly bottom
	Additional comments		side GND plane	1	TH via type must be Blind and micro via			Mech	hanical 13: Component 3D body
	Top layer copper foil thickness		.5um	1	copper			NOTE	es: Board shape and frame
	Track width		3.93 mils)	1					
	Track spacing		3.93 mils>	1					
	Distance to reference plane		>3h	1					
	Dielectric thickness between layers		102um (4 mils)	-					
	Dielectric permittivity between layers (Er)	Top-L2	4.2	-					
l ŀ		100 01 11		-					
	IApproximate microstrip line impedance	I III IIDMC (+/-	, III, INIAFANCAI						
$\vdash$	Approximate microstrip line impedance  Target impedance	100 Ohms (+/-		-					
Г	Target impedance	Single-ended	50R						
	Target impedance Additional comments	Single-ended Bottom layer, n	50R no side GND plane						
tom>	Target impedance Additional comments  Top layer copper foil thickness	Single-ended  Bottom layer, n  17.	50R no side GND plane 5 um		VERY IMPORT	ANT N	OTES		
Sottom)	Target impedance Additional comments Top layer copper foil thickness Track width	Single-ended  Bottom layer, n  17.	50R no side GND plane 5 um	GENERAL	VERY IMPORTA PCB SPECS	ANT N		ITIONAL F	REQUIREMENTS
(Bottom)	Target impedance Additional comments Top layer copper foil thickness Track width Distance to reference plane	Single-ended  Bottom layer, n  17.	50R no side GND plane 5 um	GENERAL  Minimum copper to copper spacing			ADDI		
RF (Bottom)	Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers	Single-ended  Bottom layer, n  17.	50R no side GND plane 5 um 18mm 3h 102um (4 mils)		PCB SPECS	All 0.	ADDI	ing 0.35mm	REQUIREMENTS  n ring and 0.2mm drill via-in-led with metal cap.
RF (Bottom)	Target impedance Additional comments Top layer copper foil thickness Track width Distance to reference plane	Single-ended  Bottom layer, n  17.  0.1	50R no side GND plane 5 um 18mm 3h 102um (4 mils) 4.2	Minimum copper to copper spacing	PCB SPECS  O.1mm (3.9mil)	All 0.	ADDI	ing 0.35mm	n ring and O.2mm drill via-in-
RF (Bottom)	Target impedance  Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-	50R no side GND plane 5 um 18mm 3h 102um (4 mils) 4.2 10% tolerance)	Minimum copper to copper spacing  Minimum track width	PCB SPECS  O.1mm (3.9mil)  O.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent	All O. (IC1 a	ADDI 2mm vias includi and IC7) must be nermal pad vias w	ing 0.35mm resin fil	n ring and O.2mm drill via-in- led with metal cap.
m) RF (Bottom)	Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential	50R no side GND plane 5 um 18mm 3h 102um (4 mils) 4.2	Minimum copper to copper spacing  Minimum track width	PCB SPECS  0.1mm (3.9mil)  0.1mm (3.9mil)  1mm +/-10%	All O. (IC1 a	ADDI 2mm vias includi and IC7) must be nermal pad vias w filled with metal and 0.2mm drill m	ing 0.35mm resin fil with 0.4mm al cap. IC: must be le	n ring and O.2mm drill via-in- led with metal cap. n ring and O.2mm drill must be 1 thermal pad vias with O.5mm eft open (NO resin fill with me
ttom) RF (Bottom)	Target impedance Additional comments Top layer copper foil thickness Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance Target impedance	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer	50R no side GND plane 18mm 3h 102um (4 mils) 4.2 7-10% tolerance) 85R	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material	PCB SPECS  O.1mm (3.9mil)  O.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or	All O. (IC1 a resin ring a cap).	ADDI 2mm vias includi and IC7) must be nermal pad vias u filled with meta	ing 0.35mm resin fil with 0.4mm al cap. IC: must be le	n ring and O.2mm drill via-in- led with metal cap. n ring and O.2mm drill must be 1 thermal pad vias with O.5mm eft open (NO resin fill with me
Bottom> RF (Bottom)	Target impedance  Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance  Target impedance  Additional comments	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.	50R no side GND plane 5 um 18mm 3h 102um (4 mils) 4.2 7-10% tolerance) 85R ers, no side GND	Minimum copper to copper spacing  Minimum track width  PCB thickness	PCB SPECS  O.1mm (3.9mil)  O.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)	All O. (IC1 a  IC1 th  resin  ring a  cap).	ADDI 2mm vias includi and IC7) must be nermal pad vias u filled with metal and 0.2mm drill m 4 vias in total,	ing 0.35mm resin fil with 0.4mm al cap. IC: must be le , marked u	n ring and 0.2mm drill via-in-led with metal cap.  n ring and 0.2mm drill must be thermal pad vias with 0.5mm eft open (NO resin fill with metal note.
nd Bottom) RF (Bottom)	Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance  Target impedance  Additional comments  Top layer copper foil thickness	Single-ended  Bottom layer, n  17.  O.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm	50R no side GND plane 5 um 18mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material	PCB SPECS  O.1mm (3.9mil)  O.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer  O.5 oz+plating	All O. (IC1 a  IC1 th  resin  ring a  cap).	ADDI 2mm vias includi and IC7) must be nermal pad vias w filled with metal and 0.2mm drill m	ing 0.35mm resin fil with 0.4mm al cap. IC: must be le , marked u	n ring and 0.2mm drill via-in-led with metal cap.  n ring and 0.2mm drill must be thermal pad vias with 0.5mm eft open (NO resin fill with metal note.
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Top and Bottom) RF (Bottom)	Target impedance Additional comments Top layer copper foil thickness Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance Target impedance Additional comments Top layer copper foil thickness Track width Track spacing	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm  0.1 mm (3)	50R no side GND plane 5 um 18mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils)	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm (3.9mil)  O.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer  O.5 oz+plating  Internal layer  1 oz  DARK BLUE	All O. (IC1 a resin ring a cap).	ADDI 2mm vias includi and IC7) must be nermal pad vias u filled with metal and 0.2mm drill m 4 vias in total,	ing 0.35mm resin fill with 0.4mm al cap. IC: must be le must be le , marked u % netlist.	n ring and 0.2mm drill via-in- led with metal cap.  n ring and 0.2mm drill must be 1 thermal pad vias with 0.5mm eft open (NO resin fill with me
Top and Bottom)  RF (Bottom)	Target impedance Additional comments  Top layer copper foil thickness  Track width  Distance to reference plane  Dielectric thickness between layers  Dielectric permittivity between layers (Er)  Approximate microstrip line impedance  Target impedance  Additional comments  Top layer copper foil thickness  Track width  Track spacing  Distance to reference plane	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm  0.1 mm (3)	50R no side GND plane 5 um 18mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils)	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm (3.9mil)  O.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer	All O. (IC1 a  IC1 th resin ring a cap).  Boards  PCB ve	ADDI 2mm vias includi and IC7) must be nermal pad vias we filled with metal and 0.2mm drill metal 4 vias in total, rical test: 100 services are to be individual.	ing 0.35mm resin fill with 0.4mm al cap. IC: must be le must be le marked w reen UL an	n ring and 0.2mm drill via-in- led with metal cap.  n ring and 0.2mm drill must be 1 thermal pad vias with 0.5mm eft open (NO resin fill with me with note.  bagged.  nd RoHS compliance marks, vend
CIe (Top and Bottom) RF (Bottom)	Target impedance Additional comments  Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments  Top layer copper foil thickness  Track width  Track spacing Distance to reference plane Dielectric thickness between layers	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm  0.1 mm (3)  Top-L2  Bottom-L7	50R no side GND plane 5 um 18mm 3h 102um (4 mils) 4.2 - 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 31h	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm (3.9mil)  O.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer	All O. (IC1 a  IC1 th resin ring a cap).  Boards  PCB ve logo a	ADDI 2mm vias includi and IC7) must be nermal pad vias we filled with metal and 0.2mm drill metal 4 vias in total, rical test: 100 services are to be individual.	ing O.35mm resin fil  with O.4mm al cap. IC: must be le marked w  netlista  vidually b reen UL and bottom w	n ring and 0.2mm drill via-in-led with metal cap.  n ring and 0.2mm drill must be thermal pad vias with 0.5mm eft open (NO resin fill with me with note.
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CIe (Top and Bottom) RF (Bottom)	Target impedance Additional comments Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm  0.1 mm (3)  Top-L2  Bottom-L7	50R no side GND plane 18mm 18mm 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3.173um (6.8 mils) 4.2	Minimum copper to copper spacing  Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm (3.9mil)  O.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer	All O. (IC1 a  IC1 th resin ring a cap).  Boards  PCB va logo a info u Assemb	ADDI- 2mm vias includicand IC7) must be nermal pad vias unfilled with metal and 0.2mm drill mand vias in total,  rical test: 100 includications are to be individually and date code on will be placed on bly note: Assembled board if there	ing 0.35mm resin fil  with 0.4mm al cap. IC: must be le marked w  netlista  vidually b  een UL and n bottom w  n PCB)  ly house e were and	n ring and 0.2mm drill via-in- led with metal cap.  n ring and 0.2mm drill must be 1 thermal pad vias with 0.5mm eft open (NO resin fill with me with note.  bagged.  d RoHS compliance marks, venc where shown (ignore if none of MUST provide notes in paper way changes during assembly and
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CIe (Top and Bottom) RF (Bottom)	Target impedance Additional comments Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm  0.1 mm (3)  Top-L2  Bottom-L7	50R no side GND plane 18mm 18mm 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3.173um (6.8 mils) 4.2	Minimum copper to copper spacing Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask	PCB SPECS  O.1mm (3.9mil)  O.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer	All O. (IC1 a  IC1 th resin ring a cap).  Board  PCB va logo a info u Assemble shippe board Note a Part R1	ADDI- 2mm vias includicand IC7) must be nermal pad vias unfilled with metal and 0.2mm drill mand vias in total,  rical test: 100 in the second date code on will be placed on bly note: Assembled board if there is not assembled example:   Initial BOM   1	ing 0.35mm resin fil  with 0.4mm al cap. IC: must be le marked w reen UL an h bottom w n PCB)  oly house e were an ed 100% acc  Current	n ring and 0.2mm drill via-in- led with metal cap.  n ring and 0.2mm drill must be 1 thermal pad vias with 0.5mm eft open (NO resin fill with me with note.  bagged.  d RoHS compliance marks, vence where shown (ignore if none of MUST provide notes in paper us by changes during assembly and cording to BOM and P&P files.
CIe (Top and Bottom) RF (Bottom)	Target impedance Additional comments Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm  0.1 mm (3)  Top-L2  Bottom-L7	50R no side GND plane 18mm 18mm 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3.173um (6.8 mils) 4.2	Minimum copper to copper spacing Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask  Silkscreen	PCB SPECS  0.1mm (3.9mil)  0.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer	All O. (IC1 and IC1 the resin ring and Cap).  Board:  PCB volume of the resin ring and cap).  Board:  PCB volume of the resin ring and cap).  PCB volume of the resin ring and cap).	ADDI  2mm vias includicand IC7) must be nermal pad vias unfilled with metal and 0.2mm drill must be and the code on will be placed on will be placed on bly note: Assembled board if there is not assembled example:  Initial BOM of asm. note  FIT FIT  REQUIREMENT #1: F	ing 0.35mm resin fil  with 0.4mm al cap. IC: must be le marked u  neen UL an hottom win PCB)  ly house e were an ed 100% ac  Current CB status  NF NF PCI EXPRES	m ring and 0.2mm drill via-in- led with metal cap.  m ring and 0.2mm drill must be thermal pad vias with 0.5mm eft open (NO resin fill with me with note.  bagged.  d RoHS compliance marks, vene where shown (ignore if none of MUST provide notes in paper us cording to BOM and P&P files.  Comment  Not mounted due to bad footp Not mounted due to part shor
CIe (Top and Bottom) RF (Bottom)	Target impedance Additional comments Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm  0.1 mm (3)  Top-L2  Bottom-L7	50R no side GND plane 18mm 18mm 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3.173um (6.8 mils) 4.2	Minimum copper to copper spacing Minimum track width PCB thickness  PCB material  Copper weight  Solder mask  Silkscreen  Hole types on the PCB and information	PCB SPECS  O.1mm (3.9mil)  O.1mm (3.9mil)  1mm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer	All O. (IC1 and IC1 the resin ring a cap).  Board:  PCB voltage a info under the shipped board Note and Note and Note and IC5  PCIe Femicro  PCIe Femicro	ADDI  2mm vias includicand IC7) must be nermal pad vias we filled with metal and 0.2mm drill mand 0.2mm drill mand 0.2mm drill mand the code on will be placed on will be placed on will be placed on bly note: Assembled board if there is not assembled example:  Initial BOM of the code on will be placed on the code on will be placed on bly note: Assembled is not assembled board if there is not assembled example:  Initial BOM of the code on the point is not assembled board if there is not assembled example:  Initial BOM of the point is note point in the sof gold of the code of o	ing O.35mm resin fil  with O.4mm el cap. IC: must be le marked w reen UL an h bottom w h PCB)  ly house e were an ed 100% ac  Current CB status  NF NF  PCI EXPRES over 50 m  Board edg	n ring and 0.2mm drill via-in- led with metal cap.  n ring and 0.2mm drill must be 1 thermal pad vias with 0.5mm eft open (NO resin fill with m with note.  bagged.  nd RoHS compliance marks, ven where shown (ignore if none of MUST provide notes in paper us cording to BOM and P&P files.  Comment  Not mounted due to bad footp Not mounted due to part shor  SS pads (top and bottom) - 30
CIe (Top and Bottom) RF (Bottom)	Target impedance Additional comments Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm  0.1 mm (3)  Top-L2  Bottom-L7	50R no side GND plane 18mm 18mm 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3.173um (6.8 mils) 4.2	Minimum copper to copper spacing Minimum track width PCB thickness  PCB material  Copper weight  Solder mask  Silkscreen  Hole types on the PCB and information Route process  Panel	D.1mm (3.9mil)  O.1mm (3.9mil)  Imm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer	All O. (IC1 all resin ring a cap).  Electr Board: PCB vologo a info under the cap board Note a cap board Not	ADDI  2mm vias includi and IC7) must be  nermal pad vias u filled with metal and 0.2mm drill m 4 vias in total,  rical test: 100 i s are to be indiv endor to silkscre and date code on will be placed on bly note: Assemble ed board if there is not assemble example:     Initial BOM     asm. note     PO  FIT FIT  REQUIREMENT #1: F inches of gold of REQUIREMENT #2: F ered (as shown).	ing 0.35mm resin fil  with 0.4mm al cap. IC: must be le must be le marked u  neen UL and bottom win PCB)  ly house e were and d 100% acc  Current CB status  NF NF  PCI EXPRES over 50 m  Board edg Edges mu  Board edg Edges mu	ring and 0.2mm drill via-in- led with metal cap.  ring and 0.2mm drill must be 1 thermal pad vias with 0.5mm eft open (NO resin fill with me with note.  bagged.  d RoHS compliance marks, vene there shown (ignore if none of MUST provide notes in paper us y changes during assembly and coording to BOM and P&P files.  Comment  Not mounted due to bad footp Not mounted due to part shor  SS pads (top and bottom) - 30 icro inches nickel plating  ge below PCI pads must be est be free of cutting burrs
CIe (Top and Bottom) RF (Bottom)	Target impedance Additional comments Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm  0.1 mm (3)  Top-L2  Bottom-L7	50R no side GND plane 18mm 18mm 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3.173um (6.8 mils) 4.2	Minimum copper to copper spacing Minimum track width  PCB thickness  PCB material  Copper weight  Solder mask  Silkscreen  Hole types on the PCB and information  Route process	O.1mm (3.9mil)  O.1mm (3.9mil)  Imm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer	All O. (IC1 all resin ring a cap).  Electr Board: PCB vologo a info under the cap board Note a cap board Not	ADDI  2mm vias includi and IC7) must be  nermal pad vias u filled with metal and 0.2mm drill m 4 vias in total,  rical test: 100 i s are to be indiv endor to silkscre and date code on will be placed on bly note: Assemble ed board if there is not assemble example:     Initial BOM     asm. note     PO  FIT FIT  REQUIREMENT #1: F inches of gold of REQUIREMENT #2: F ered (as shown).	ing 0.35mm resin fil  with 0.4mm al cap. IC: must be le must be le marked u  neen UL and bottom win PCB)  ly house e were and d 100% acc  Current CB status  NF NF  PCI EXPRES over 50 m  Board edg Edges mu  Board edg Edges mu	ring and 0.2mm drill via-in- led with metal cap.  n ring and 0.2mm drill must be 1 thermal pad vias with 0.5mm eft open (NO resin fill with me with note.  bagged.  nd RoHS compliance marks, veno where shown (ignore if none of MUST provide notes in paper us y changes during assembly and coording to BOM and P&P files.  Comment  Not mounted due to bad footp Not mounted due to part shor  SS pads (top and bottom) - 30 icro inches nickel plating  ge below PCI pads must be
CIe (Top and Bottom) RF (Bottom)	Target impedance Additional comments Top layer copper foil thickness  Track width Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers (Er) Approximate microstrip line impedance  Target impedance Additional comments Top layer copper foil thickness  Track width Track spacing Distance to reference plane Dielectric thickness between layers Dielectric permittivity between layers Dielectric permittivity between layers (Er)	Single-ended  Bottom layer, n  17.  0.1  Bottom-L7  49.99 Ohms (+/-  Differential  Top/Bottom layer  17.  0.14 mm  0.1 mm (3)  Top-L2  Bottom-L7	50R no side GND plane 18mm 18mm 102um (4 mils) 4.2 10% tolerance) 85R ers, no side GND 5 um (5.5 mils) 3.93 mils) 3.173um (6.8 mils) 4.2	Minimum copper to copper spacing Minimum track width PCB thickness  PCB material  Copper weight  Solder mask  Silkscreen  Hole types on the PCB and information Route process  Panel	D.1mm (3.9mil)  O.1mm (3.9mil)  Imm +/-10%  IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)  External layer	All O. (IC1 a resin ring a cap).  Electr Board: PCB vologo a info u rinfo u ri	ADDI  2mm vias includi and IC7) must be  nermal pad vias u filled with metal and 0.2mm drill m 4 vias in total,  rical test: 100 i s are to be indiv endor to silkscre and date code on will be placed on bly note: Assemble ed board if there is not assemble example:     Initial BOM     asm. note     PO  FIT FIT  REQUIREMENT #1: F inches of gold of REQUIREMENT #2: F ered (as shown).	ing 0.35mm resin fil  with 0.4mm al cap. IC: must be le must be le must be le must be le reen UL an bottom win PCB)  ly house e were an ed 100% ac  Current CB status  NF NF  PCI EXPREs over 50 m  Board edg Edges must  PCIe finge	ring and 0.2mm drill via-in- led with metal cap.  In ring and 0.2mm drill must be 1 thermal pad vias with 0.5mm eft open (NO resin fill with me with note.  In the manage of the marks, vent where shown (ignore if none of MUST provide notes in paper un the cording to BOM and P&P files.  Comment  Not mounted due to bad footp Not mounted due to part shor  SS pads (top and bottom) - 30 icro inches nickel plating  ge below PCI pads must be set be free of cutting burrs  er leader lines are acceptable



