

LimeSDR-XTRX_v1.1

CONTROLLED IMPEDANCE				STACKUP AND LAYER DESCRIPTION							
H											
L	GENERAL PARA										
Parameter		Layer/Layers	Value								
Cop	oper foil thickness	Тор	17.5um								
Dielectric thickness between layers		TI 2	102um (4 mils)								
Die	electric permittivity between layers (Er)	Top-L2	4.2								
Cor	oper foil thickness	Bottom	17.5um			Via type #2		Via type #1			
Dielectric thickness between layers			102um (4 mils)	GERBER LAYER NAMES:		Micro via L7-Bot		Bot Top-Bot			
-		Bottom-L7		GTP Top solder paste				Top-Bot			
DIE	electric permittivity between layers (Er)		4.2	GTO Silkscreen GTS Soldermask (halogen free)						AL LAYERS:	
	CALCULATIONS			GTL 0.5oz+plating PP 4mil (02um) IT1 80A: 3313				Top: RF/	/Signal/PWR/GND	
	Target impedance	Single-ended	50R	G1 1oz (35um) CORE 4mil (02um) IT180A: 3313				L2: GND		
	Additional comments	Top layer, no	side GND plane		(117um) IT180A: 2116			_	-	nal/PWR/GND	
	Top layer copper foil thickness	17.5um		G3 1oz (35um) CORE 4mil (02um) IT180A: 3313				L4: Signal.	II/PWR/GND	
Top	Track width	O.18mm			(117um) IT180A: 2116					L5: GND	
	Distance to reference plane			G5 1oz (35um) CORE 4mil (02um) IT180A: 3313				L6: CLK/PWF	'WR/GND	
RF.	<u> </u>		Sh	G6 1oz (35um) — — — — — — — — — — — — — — — — — — —	02um) IT1 80A: 3313	IT180A: 3313		_	_7: GND		
	Dielectric thickness between layers	Top-L2	102um (4 mils)	GBL 0.5oz+plating GBS Soldermask (halogen free)					Bottom: RF/Signal/PWR/GND		
	Dielectric permittivity between layers (Er)		4.2	GBO Silkscreen						ADDITIONAL LAYERS:	
	Approximate microstrip line impedance	50 Ohms (+/-	10% tolerance)	GBP Bottom solder paste Total PCB thi	zknes: 1mm +/- 10%	0.15mm drill 0.5mm ring TH via type must be			Mechanical 1: Board cutout ASM TOP: Assembly top		
	Target impedance	Differential	100R		TH				ASM E	BOT: Assembly bottom	
	Additional comments	o layer copper foil thickness 17.5um		Blind and micro via type can be coated with Mechanical 13: Component copper							_
	Top layer copper foil thickness										
<u>a</u>											
(Top)	Track spacing	-									
١.		-									
ద	Distance to reference plane	>:	3h								
	Dielectric thickness between layers	Top-L2	102um (4 mils)								
	Dielectric permittivity between layers (Er)										
	Approximate microstrip line impedance	100 Ohms (+/-	10% tolerance)								
Г	Target impedance	Single-ended	50R	1							
	Additional comments	Bottom layer. no	side GND plane	1							
2	Top layer copper foil thickness	17.5 um									
t O	2			VERY IMPORTANT NOTES							
		0.18mm		GENERAL PCB SPECS ADDITIONAL REQUIREMENTS							
B B		>3h							. J. WILL KL		
꿈		Bottom-L7	102um (4 mils)	Minimum copper to copper spacing		0.1mm (3.9mil)		All 0.2mm vias including (IC1 and IC7) must be res		0.35mm ring and 0.2mm drill via-in-pac	
	Dielectric permittivity between layers (Er)		4.2	Minimum track width	O.1mm <	3.9mil>	1101 6	and town mast be te	SIII TIII6		
L	Approximate microstrip line impedance	49.99 Ohms (+/-	10% tolerance)	PCB thickness		/-10%	IC1 thormal and wine with		b O 4mm wine and O 2mm duill accet be		
ê	Target impedance	Differential	85R	DCR matorial	·	IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher) External layer 0.5 oz+plating		resin filled with metal cap. IC1 thermal pad vias with tring and 0.2mm drill must be left open (NO resin fill wicap). 4 vias in total, marked with note.			
ton	Additional comments	Top/Bottom laye	rs, no side GND	- PCB material							th metal
Bot		17.5	ium		External layer			T VIAS IN TOTAL, MA	arked W1	tti ilote.	
			5.5 mils)	Copper weight	Internal layer	1 oz					
Pue	Track spacing			 				rical test : 100 % i	netlist.		
	·		93 mils)	-		DARK BLUE					
Top		>:	3h	- Solder mask		Halogen free Glossy finish (NOT matte)		● Boards are to be individually bagged.			
~		Top-L2	173um (6.8 mils)								
CIe	Dielectric permittivity between layers (Er)	Bottom-L7	4.2		Glossy finish					d RoHS compliance marks, Here shown (ignore if non-	
PC	Approximate microstrip line impedance	85 Ohms (+/-	10% tolerance)		White ep	White epoxy ink		will be placed on P			_ = (11
Г				Both	Both sides Halogen free No silkscreen on pads				UST provide notes in pap		
			Silkscreen	Haloge			shipped board if there were any changes during assemble board is not assembled 100% according to BOM and P&P Note example:				
				No silkscre							
					Plated 💢	Non-plated 💢	Part	Initial BOM Cur asm. note PCB		Comment	
				Hole types on the PCB and informat			R1		_	Not mounted due to bad fo	notorio
				Hore (abes on the LCD and Thitohilla)	• manufactured di	ameters INCLUDING				Not mounted due to bad to Not mounted due to part :	•
					HOLE METALIZATI	<u> </u>					
				Route process	V-score	Tab route 🔀				S pads (top and bottom) -	
				V-score and tab r	V-score and tab route		micro inches of gold over 50 micro inches nickel plating				
Pa			Panel	Yes	Yes No 🔀		PCIe REQUIREMENT #2: Board edge below PCI pads must be				
			HASL lead free	HASL lead free HASL with lead Immersion gold 0.05-0.10um of gold over 2.50-5.00um of nickel		chamfered (as shown). Edges must be free of cutting burrs • PCIe REQUIREMENT #3: PCIe finger leader lines are acceptable					
	Su										HASL with lead
										Surface finish (both sides)	
										og igce itilizii (DO(II 21062)	2.50
			USP								
					Hard gold PCIe fing	ers					



