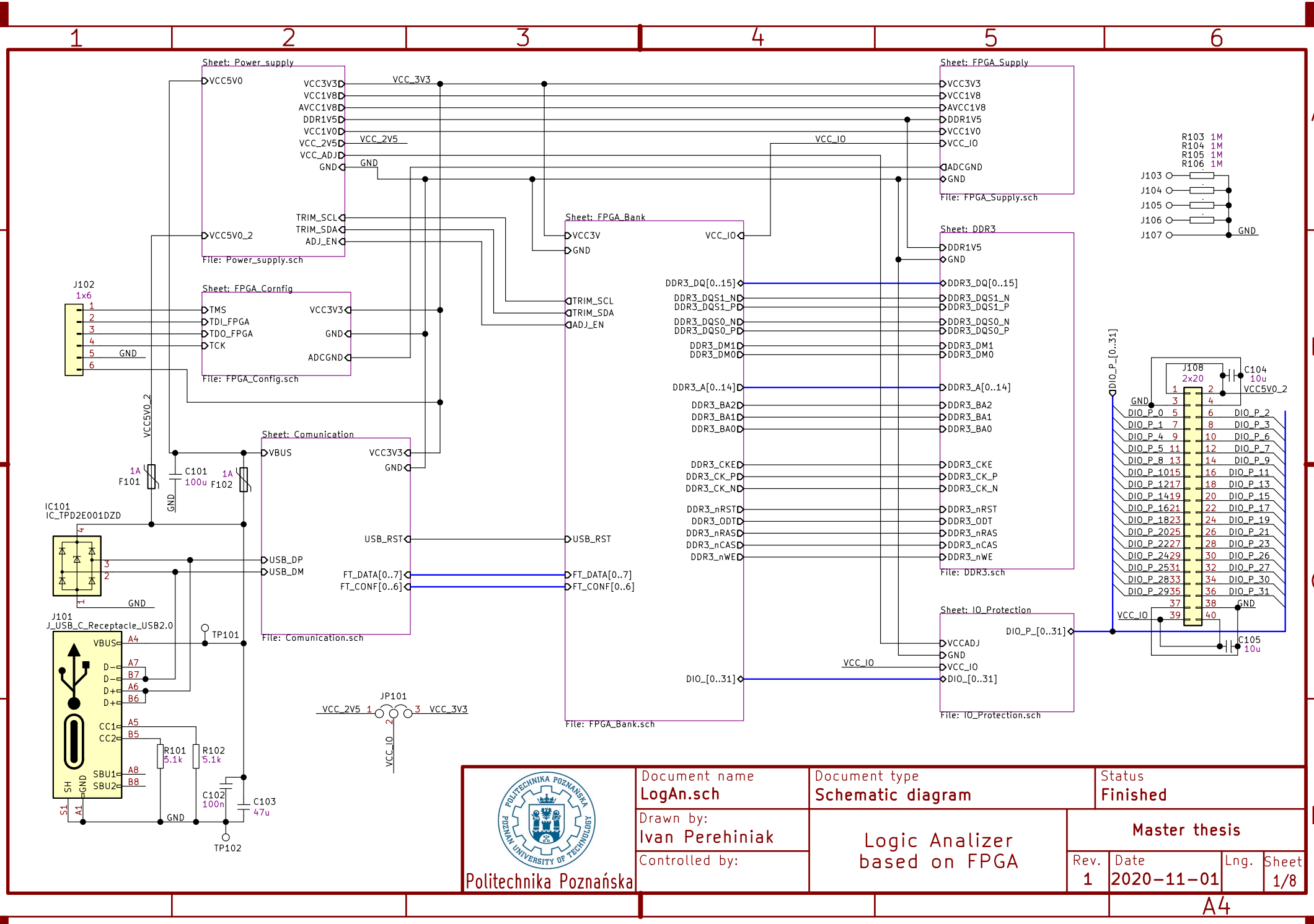
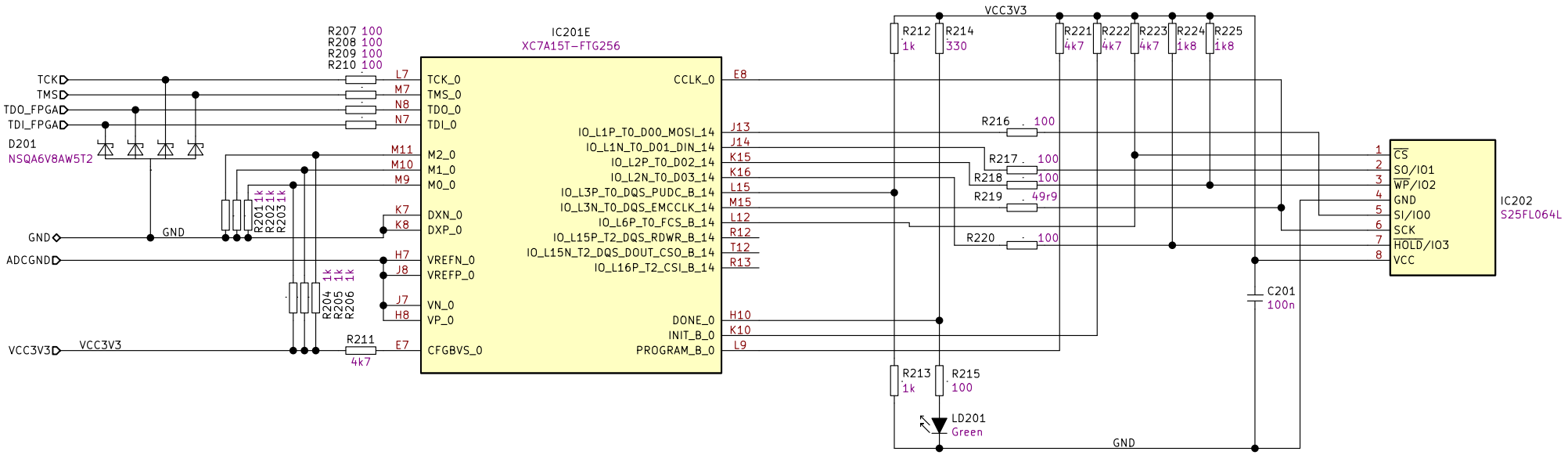

Sheet: Power_supply
VCC5V0
VCC3V3
VCC1V8
AVCC1V8
DDR1V5
VCC1V0
VCC_2V5
VCC_ADJ
GND
VCC5V0_2
TRIM_SCL
TRIM_SDA
ADJ_EN
File: Power_supply.sch
Sheet: FPGA_Supply
VCC_IO
ADCGND
File: FPGA_Supply.sch
R103 1M
R104 1M
R105 1M
R106 1M
J103
J104
J105
J106
J107
J102
1x6
TMS
TDI_FPGA
TDO_FPGA
TCK
Sheet: FPGA_Cornfig
File: FPGA_Config.sch
Sheet: FPGA_Bank
VCC3V
File: FPGA_Bank.sch
Sheet: DDR3
DDR3_DQ[0..15]
DDR3_DQS1_N
DDR3_DQS1_P
DDR3_DQS0_N
DDR3_DQS0_P
DDR3_DM1
DDR3_DM0
DDR3_A[0..14]
DDR3_BA2
DDR3_BA1
DDR3_BA0
DDR3_CKE
DDR3_CK_P
DDR3_CK_N
DDR3_nRST
DDR3_ODT
DDR3_nRAS
DDR3_nCAS
DDR3_nWE
File: DDR3.sch
J108
2x20
C104
10u
C105
10u
DIO_P_[0..31]
Sheet: IO_Protection
VCCADJ
DIO_[0..31]
File: IO_Protection.sch
Sheet: Comunication
VBUS
USB_DP
USB_DM
USB_RST
FT_DATA[0..7]
FT_CONF[0..6]
File: Comunication.sch
F101
F102
C101
100u
IC101
IC_TPD2E001DZD
J101
J_USB_C_Receptacle_USB2.0
TP101
TP102
R101
5.1k
R102
5.1k
C102
100n
C103
47u
JP101
VCC_2V5
VCC_3V3
VCC_IO
Politechnika Poznańska
Document name
LogAn.sch
Document type
Schematic diagram
Status
Finished
Drawn by:
Ivan Perehiniak
Controlled by:
Logic Analizer
based on FPGA
Master thesis
Rev.
1
Date
2020-11-01
Lng.
Sheet
1/8
A4



Politechnika Poznańska	Document name: FPGA_Config.sch	Document type: Schematic diagram	Status: Finished
	Drawn by: Ivan Perehiniak	Logic Analizer based on FPGA	Master thesis
	Controlled by:		Rev. 1 · Date 2020-11-01 · Lng. · Sheet 2/8

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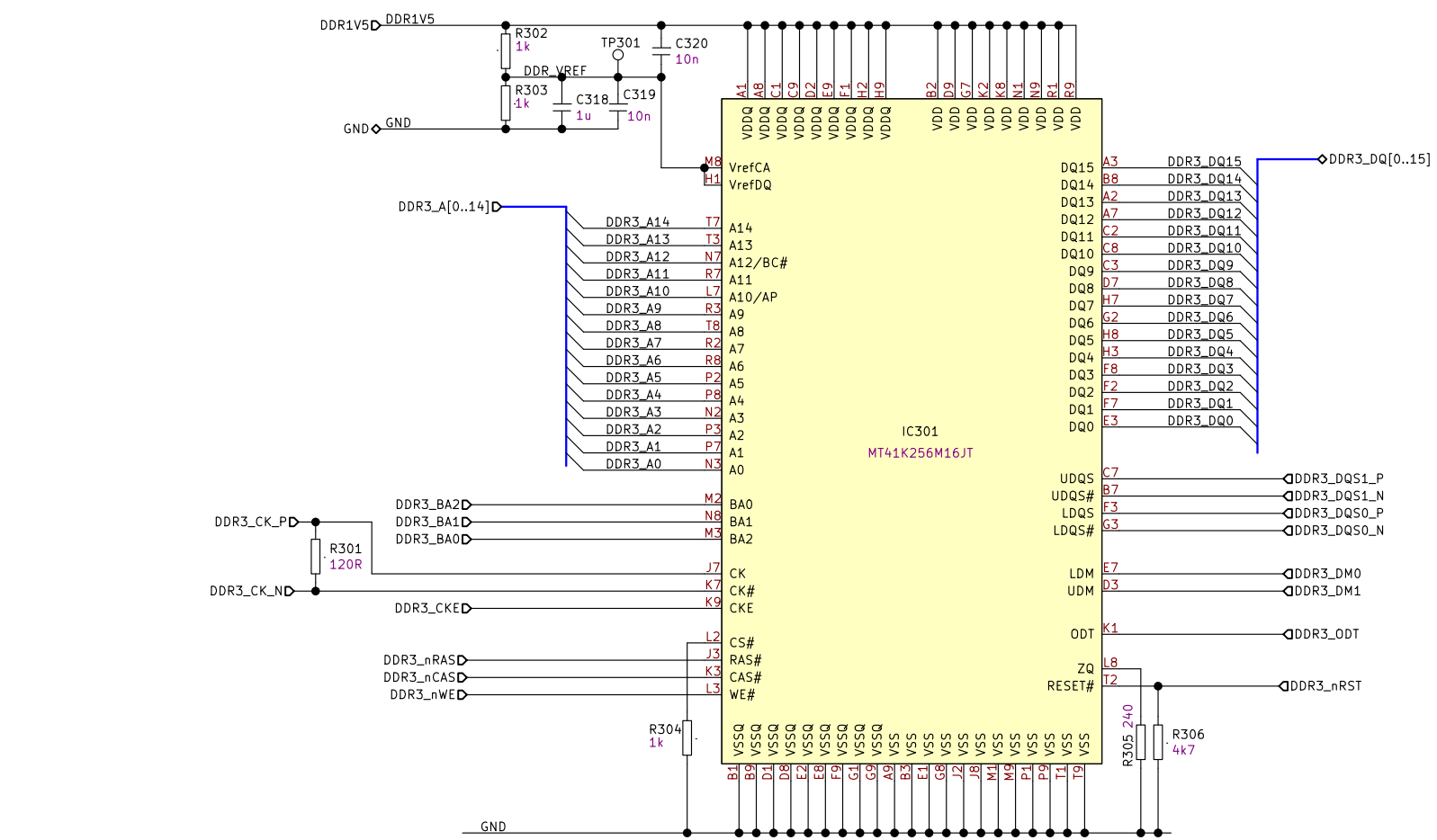
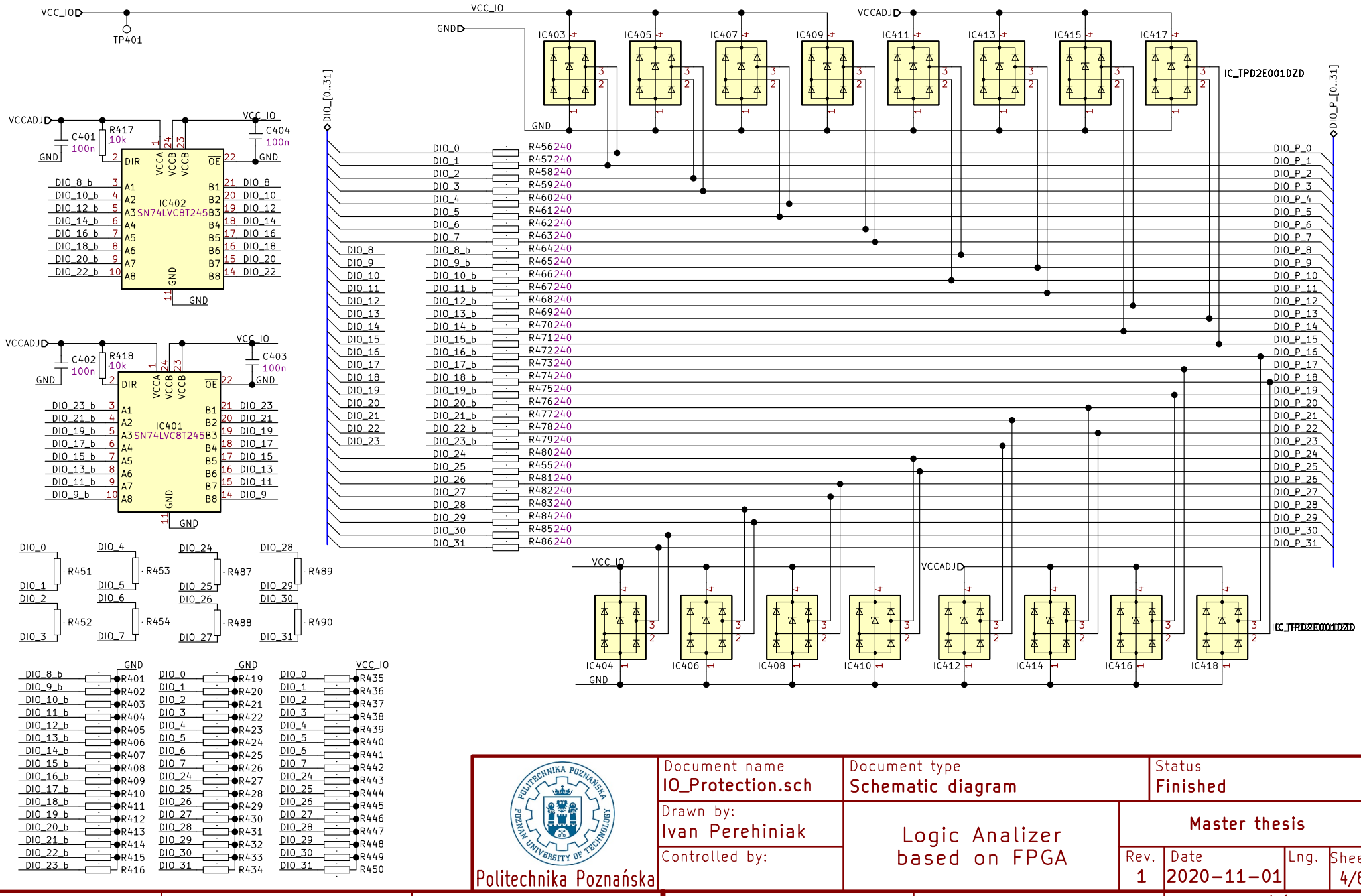


Politechnika Poznańska	Document name: DDR3.sch	Document type: Schematic diagram	Status: Finished
	Drawn by: Ivan Perehiniak	Logic Analizer based on FPGA	Master thesis
	Controlled by:		Rev. 1 · Date 2020-11-01 · Lng. · Sheet 3/8

A4



Politechnika Poznańska	Document name: IO_Protection.sch	Document type: Schematic diagram	Status: Finished
	Drawn by: Ivan Perehiniak	Logic Analizer based on FPGA	Master thesis
	Controlled by:		Rev. 1 · Date 2020-11-01 · Lng. · Sheet 4/8

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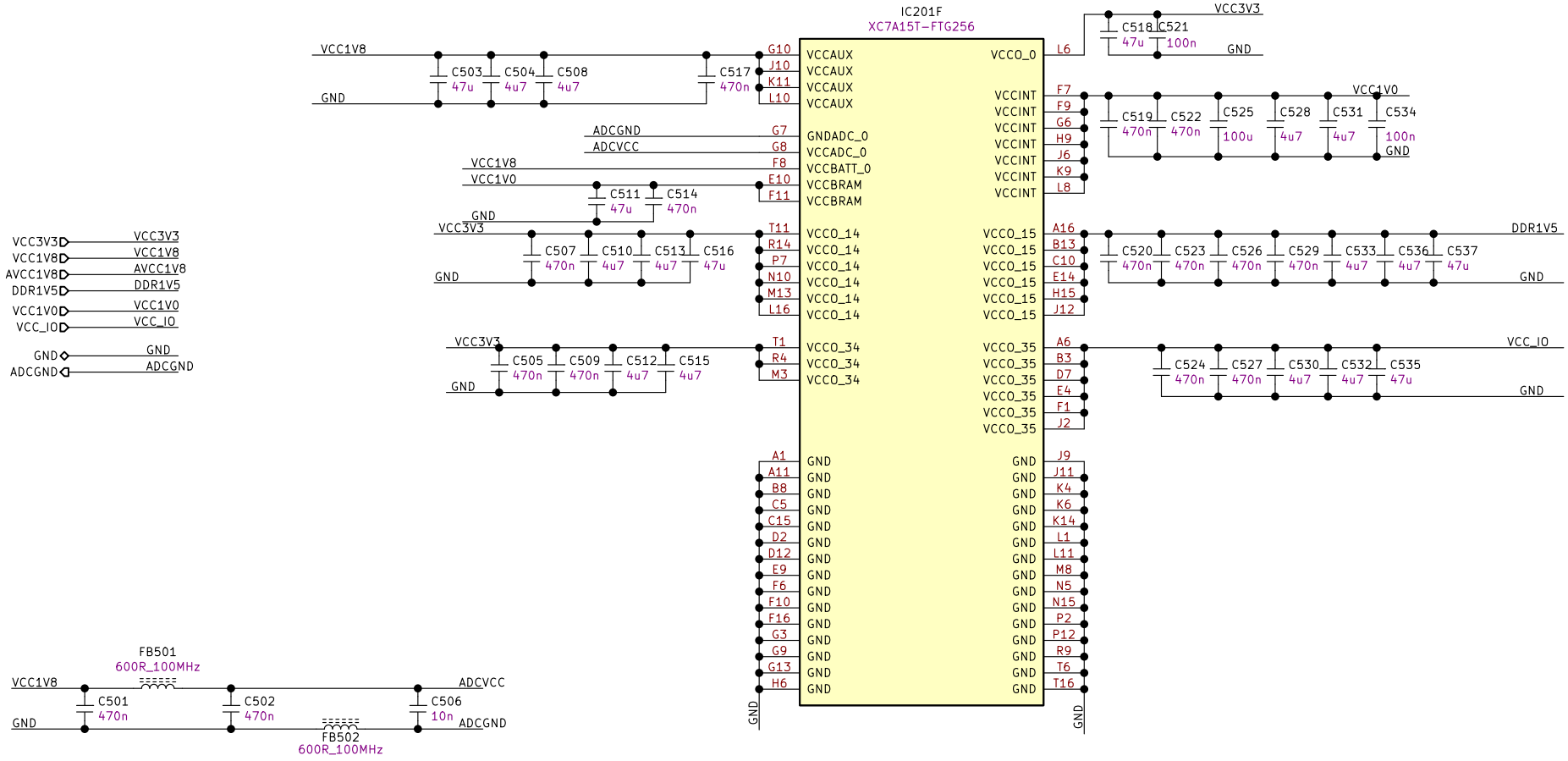
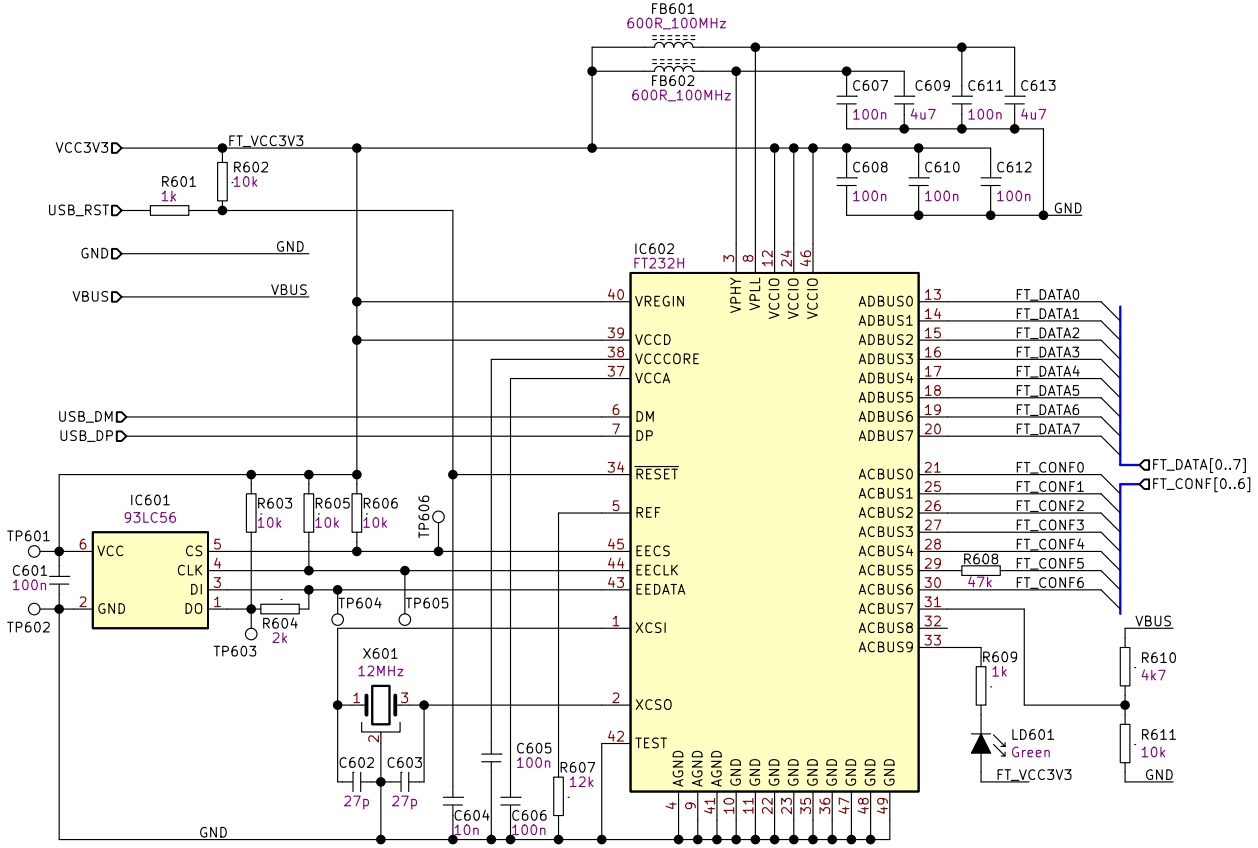


Politechnika Poznańska	Document name: FPGA_Supply.sch	Document type: Schematic diagram	Status: Finished
	Drawn by: Ivan Perehiniak	Logic Analizer based on FPGA	Master thesis
	Controlled by:		Rev. 1 · Date 2020-11-01 · Lng. · Sheet 5/8

A4



Politechnika Poznańska	Document name: Comunication.sch	Document type: Schematic diagram	Status: Finished
	Drawn by: Ivan Perehiniak	Logic Analizer based on FPGA	Master thesis
	Controlled by:		Rev. 1 · Date 2020-11-01 · Lng. · Sheet 6/8

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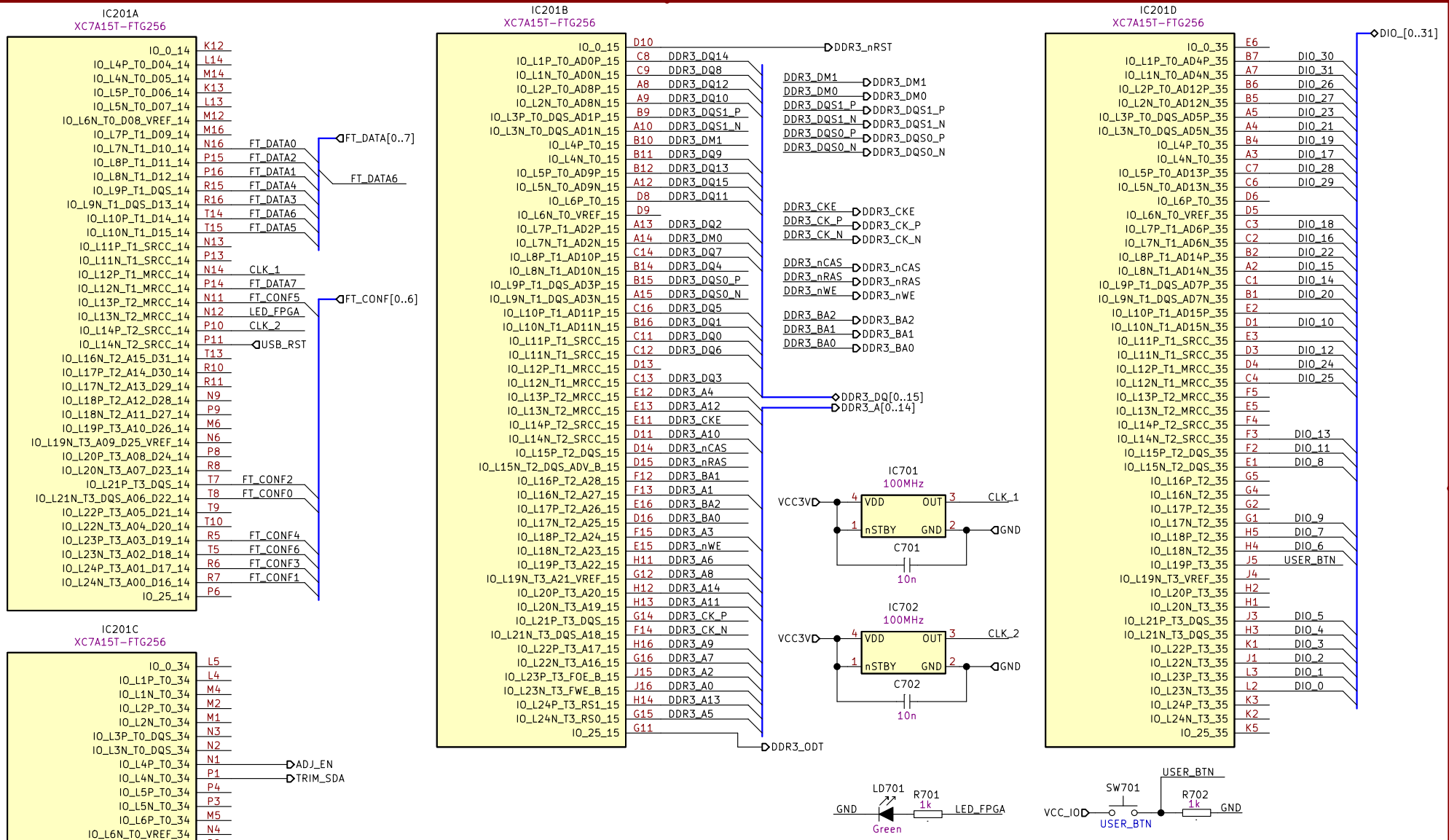
IC201A
XC7A15T-FTG256
IO_0_14 K12
IO_L4P_T0_D04_14 L14
IO_L4N_T0_D05_14 M14
IO_L5P_T0_D06_14 K13
IO_L5N_T0_D07_14 L13
IO_L6N_T0_D08_VREF_14 M12
IO_L7P_T1_D09_14 M16
IO_L7N_T1_D10_14 N16 FT_DATA0
IO_L8P_T1_D11_14 P15 FT_DATA2
IO_L8N_T1_D12_14 P16 FT_DATA1
IO_L9P_T1_DQS_14 R15 FT_DATA4
IO_L9N_T1_DQS_D13_14 R16 FT_DATA3
IO_L10P_T1_D14_14 T14 FT_DATA6
IO_L10N_T1_D15_14 T15 FT_DATA5
IO_L11P_T1_SRCC_14 N13
IO_L11N_T1_SRCC_14 P13
IO_L12P_T1_MRCC_14 N14 CLK_1
IO_L12N_T1_MRCC_14 P14 FT_DATA7
IO_L13P_T2_MRCC_14 N11 FT_CONF5
IO_L13N_T2_MRCC_14 N12 LED_FPGA
IO_L14P_T2_SRCC_14 P10 CLK_2
IO_L14N_T2_SRCC_14 P11 USB_RST
IO_L16N_T2_A15_D31_14 T13
IO_L17P_T2_A14_D30_14 R10
IO_L17N_T2_A13_D29_14 R11
IO_L18P_T2_A12_D28_14 N9
IO_L18N_T2_A11_D27_14 P9
IO_L19P_T3_A10_D26_14 M6
IO_L19N_T3_A09_D25_VREF_14 N6
IO_L20P_T3_A08_D24_14 P8
IO_L20N_T3_A07_D23_14 R8
IO_L21P_T3_DQS_14 T7 FT_CONF2
IO_L21N_T3_DQS_A06_D22_14 T8 FT_CONF0
IO_L22P_T3_A05_D21_14 T9
IO_L22N_T3_A04_D20_14 T10
IO_L23P_T3_A03_D19_14 R5 FT_CONF4
IO_L23N_T3_A02_D18_14 T5 FT_CONF6
IO_L24P_T3_A01_D17_14 R6 FT_CONF3
IO_L24N_T3_A00_D16_14 R7 FT_CONF1
IO_25_14 P6
FT_DATA[0..7]
FT_DATA6
FT_CONF[0..6]
IC201C
XC7A15T-FTG256
IO_0_34 L5
IO_L1P_T0_34 L4
IO_L1N_T0_34 M4
IO_L2P_T0_34 M2
IO_L2N_T0_34 M1
IO_L3P_T0_DQS_34 N3
IO_L3N_T0_DQS_34 N2
IO_L4P_T0_34 N1 ADJ_EN
IO_L4N_T0_34 P1 TRIM_SDA
IO_L5P_T0_34 P4
IO_L5N_T0_34 P3
IO_L6P_T0_34 M5
IO_L6N_T0_VREF_34 N4
IO_L7P_T1_34 R2
IO_L7N_T1_34 R1 TRIM_SCL
IO_L8P_T1_34 R3
IO_L8N_T1_34 T2
IO_L9P_T1_DQS_34 T4
IO_L9N_T1_DQS_34 T3
IO_L10P_T1_34 P5
IC201B
XC7A15T-FTG256
IO_0_15 D10 DDR3_nRST
IO_L1P_T0_AD0P_15 C8 DDR3_DQ14
IO_L1N_T0_AD0N_15 C9 DDR3_DQ8
IO_L2P_T0_AD8P_15 A8 DDR3_DQ12
IO_L2N_T0_AD8N_15 A9 DDR3_DQ10
IO_L3P_T0_DQS_AD1P_15 B9 DDR3_DQS1_P
IO_L3N_T0_DQS_AD1N_15 A10 DDR3_DQS1_N
IO_L4P_T0_15 B10 DDR3_DM1
IO_L4N_T0_15 B11 DDR3_DQ9
IO_L5P_T0_AD9P_15 B12 DDR3_DQ13
IO_L5N_T0_AD9N_15 A12 DDR3_DQ15
IO_L6P_T0_15 D8 DDR3_DQ11
IO_L6N_T0_VREF_15 D9
IO_L7P_T1_AD2P_15 A13 DDR3_DQ2
IO_L7N_T1_AD2N_15 A14 DDR3_DM0
IO_L8P_T1_AD10P_15 C14 DDR3_DQ7
IO_L8N_T1_AD10N_15 B14 DDR3_DQ4
IO_L9P_T1_DQS_AD3P_15 B15 DDR3_DQS0_P
IO_L9N_T1_DQS_AD3N_15 A15 DDR3_DQS0_N
IO_L10P_T1_AD11P_15 C16 DDR3_DQ5
IO_L10N_T1_AD11N_15 B16 DDR3_DQ1
IO_L11P_T1_SRCC_15 C11 DDR3_DQ0
IO_L11N_T1_SRCC_15 C12 DDR3_DQ6
IO_L12P_T1_MRCC_15 D13
IO_L12N_T1_MRCC_15 C13 DDR3_DQ3
IO_L13P_T2_MRCC_15 E12 DDR3_A4
IO_L13N_T2_MRCC_15 E13 DDR3_A12
IO_L14P_T2_SRCC_15 E11 DDR3_CKE
IO_L14N_T2_SRCC_15 D11 DDR3_A10
IO_L15P_T2_DQS_15 D14 DDR3_nCAS
IO_L15N_T2_DQS_ADV_B_15 D15 DDR3_nRAS
IO_L16P_T2_A28_15 F12 DDR3_BA1
IO_L16N_T2_A27_15 F13 DDR3_A1
IO_L17P_T2_A26_15 E16 DDR3_BA2
IO_L17N_T2_A25_15 D16 DDR3_BA0
IO_L18P_T2_A24_15 F15 DDR3_A3
IO_L18N_T2_A23_15 E15 DDR3_nWE
IO_L19P_T3_A22_15 H11 DDR3_A6
IO_L19N_T3_A21_VREF_15 G12 DDR3_A8
IO_L20P_T3_A20_15 H12 DDR3_A14
IO_L20N_T3_A19_15 H13 DDR3_A11
IO_L21P_T3_DQS_15 G14 DDR3_CK_P
IO_L21N_T3_DQS_A18_15 F14 DDR3_CK_N
IO_L22P_T3_A17_15 H16 DDR3_A9
IO_L22N_T3_A16_15 G16 DDR3_A7
IO_L23P_T3_FOE_B_15 J15 DDR3_A2
IO_L23N_T3_FWE_B_15 J16 DDR3_A0
IO_L24P_T3_RS1_15 H14 DDR3_A13
IO_L24N_T3_RS0_15 G15 DDR3_A5
IO_25_15 G11
DDR3_ODT
DDR3_DM1 DDR3_DM1
DDR3_DM0 DDR3_DM0
DDR3_DQS1_P DDR3_DQS1_P
DDR3_DQS1_N DDR3_DQS1_N
DDR3_DQS0_P DDR3_DQS0_P
DDR3_DQS0_N DDR3_DQS0_N
DDR3_CKE DDR3_CKE
DDR3_CK_P DDR3_CK_P
DDR3_CK_N DDR3_CK_N
DDR3_nCAS DDR3_nCAS
DDR3_nRAS DDR3_nRAS
DDR3_nWE DDR3_nWE
DDR3_BA2 DDR3_BA2
DDR3_BA1 DDR3_BA1
DDR3_BA0 DDR3_BA0
DDR3_DQ[0..15]
DDR3_A[0..14]
IC701
100MHz
VCC3V3
VDD
OUT
nSTBY
GND
CLK_1
C701
10n
IC702
100MHz
CLK_2
LD701
Green
R701
1k
LED_FPGA
SW701
USER_BTN
R702
VCC_IO
IC201D
XC7A15T-FTG256
IO_0_35 E6
IO_L1P_T0_AD4P_35 B7 DIO_30
IO_L1N_T0_AD4N_35 A7 DIO_31
IO_L2P_T0_AD12P_35 B6 DIO_26
IO_L2N_T0_AD12N_35 B5 DIO_27
IO_L3P_T0_DQS_AD5P_35 A5 DIO_23
IO_L3N_T0_DQS_AD5N_35 A4 DIO_21
IO_L4P_T0_35 B4 DIO_19
IO_L4N_T0_35 A3 DIO_17
IO_L5P_T0_AD13P_35 C7 DIO_28
IO_L5N_T0_AD13N_35 C6 DIO_29
IO_L6P_T0_35 D6
IO_L6N_T0_VREF_35 D5
IO_L7P_T1_AD6P_35 C3 DIO_18
IO_L7N_T1_AD6N_35 C2 DIO_16
IO_L8P_T1_AD14P_35 B2 DIO_22
IO_L8N_T1_AD14N_35 A2 DIO_15
IO_L9P_T1_DQS_AD7P_35 C1 DIO_14
IO_L9N_T1_DQS_AD7N_35 B1 DIO_20
IO_L10P_T1_AD15P_35 E2
IO_L10N_T1_AD15N_35 D1 DIO_10
IO_L11P_T1_SRCC_35 E3
IO_L11N_T1_SRCC_35 D3 DIO_12
IO_L12P_T1_MRCC_35 D4 DIO_24
IO_L12N_T1_MRCC_35 C4 DIO_25
IO_L13P_T2_MRCC_35 F5
IO_L13N_T2_MRCC_35 E5
IO_L14P_T2_SRCC_35 F4
IO_L14N_T2_SRCC_35 F3 DIO_13
IO_L15P_T2_DQS_35 F2 DIO_11
IO_L15N_T2_DQS_35 E1 DIO_8
IO_L16P_T2_35 G5
IO_L16N_T2_35 G4
IO_L17P_T2_35 G2
IO_L17N_T2_35 G1 DIO_9
IO_L18P_T2_35 H5 DIO_7
IO_L18N_T2_35 H4 DIO_6
IO_L19P_T3_35 J5 USER_BTN
IO_L19N_T3_VREF_35 J4
IO_L20P_T3_35 H2
IO_L20N_T3_35 H1
IO_L21P_T3_DQS_35 J3 DIO_5
IO_L21N_T3_DQS_35 H3 DIO_4
IO_L22P_T3_35 K1 DIO_3
IO_L22N_T3_35 J1 DIO_2
IO_L23P_T3_35 L3 DIO_1
IO_L23N_T3_35 L2 DIO_0
IO_L24P_T3_35 K3
IO_L24N_T3_35 K2
IO_25_35 K5
DIO_[0..31]
Politechnika Poznańska
Document name
FPGA_Bank.sch
Document type
Schematic diagram
Status
Finished
Drawn by:
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Logic Analizer
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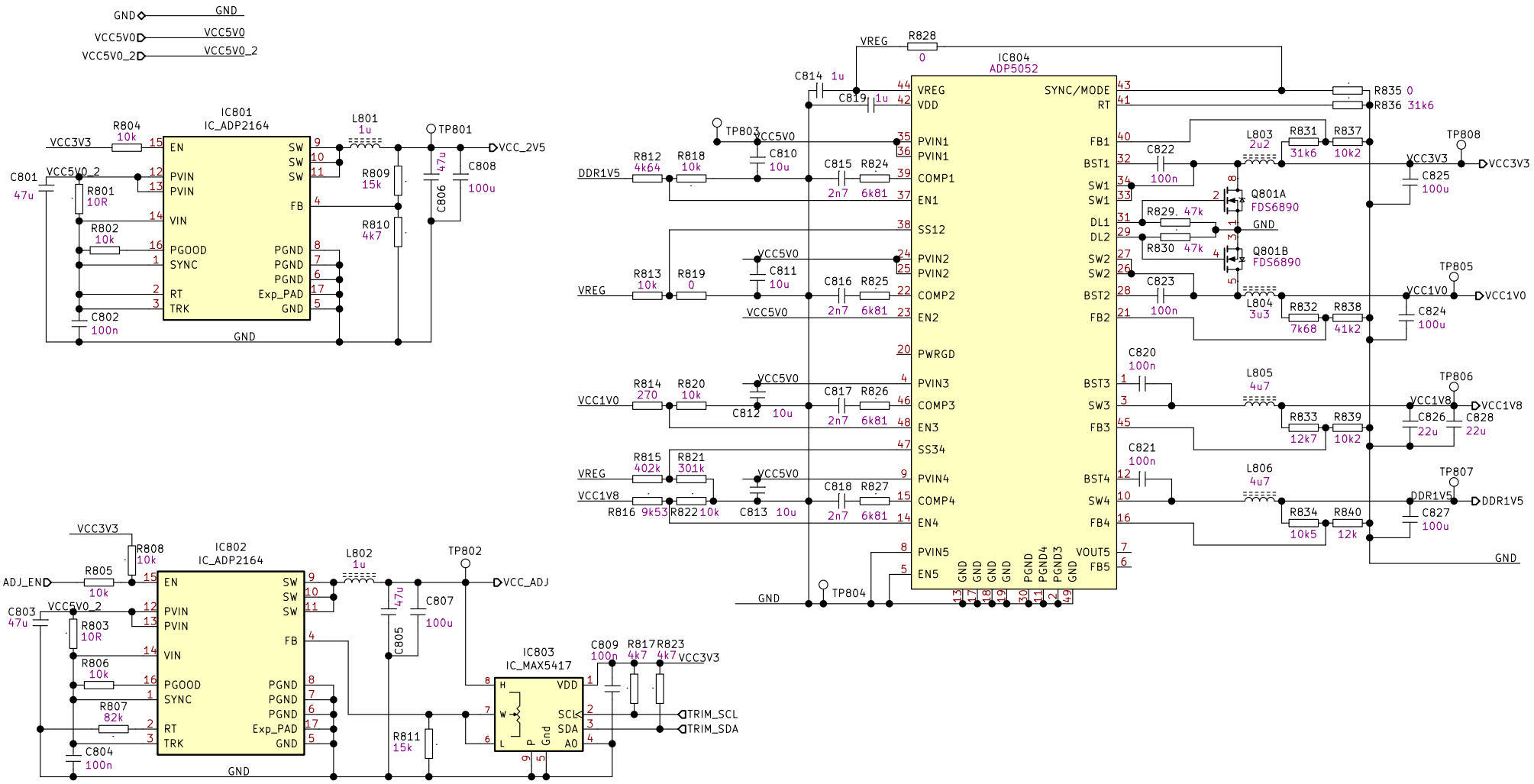

Politechnika Poznańska	Document name: Power_supply.sch	Document type: Schematic diagram	Status: Finished
	Drawn by: Ivan Perehiniak	Logic Analizer based on FPGA	Master thesis
	Controlled by:		Rev. 1 · Date 2020-11-01 · Lng. · Sheet 8/8

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