RK3588_HW_Test_Report_Summary

福州硬件开发中心

更改记录

版本	修改人	修改日期	修改说明	备注
V1.1	福州硬件开发中心	2022.03.31	首次发布	
V1.2	福州硬件开发中心	2022.08.29	1）电源稳波测试数据更新。---PAGE6 2）上电时序测试更新为RK806－1。---PAGE7 3） 更新核心模块的极限电流表。---PAGE12	
V1.3	福州硬件开发中心	2023.02.15	1）更新RGMII的测试表格。---PAGE44	

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01 电源纹波测试

测试条件：

测试环境：RK3588 EVB， 环境温度24℃，TSADC最高75℃。

测试场景：Antutu8.4.3,stressapptest。

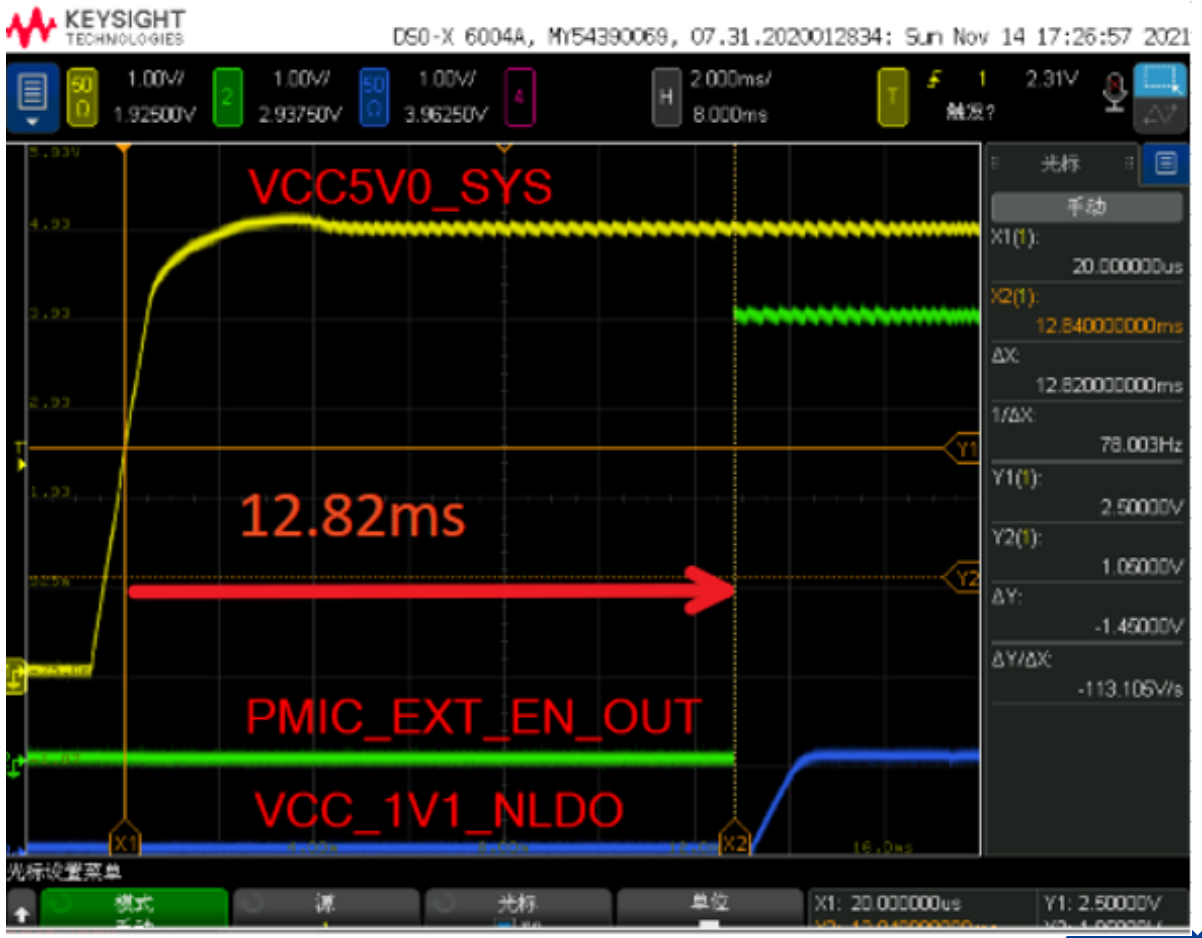
测试要求：打开余辉功能，示波器通道 50Ω，关闭带宽限制。

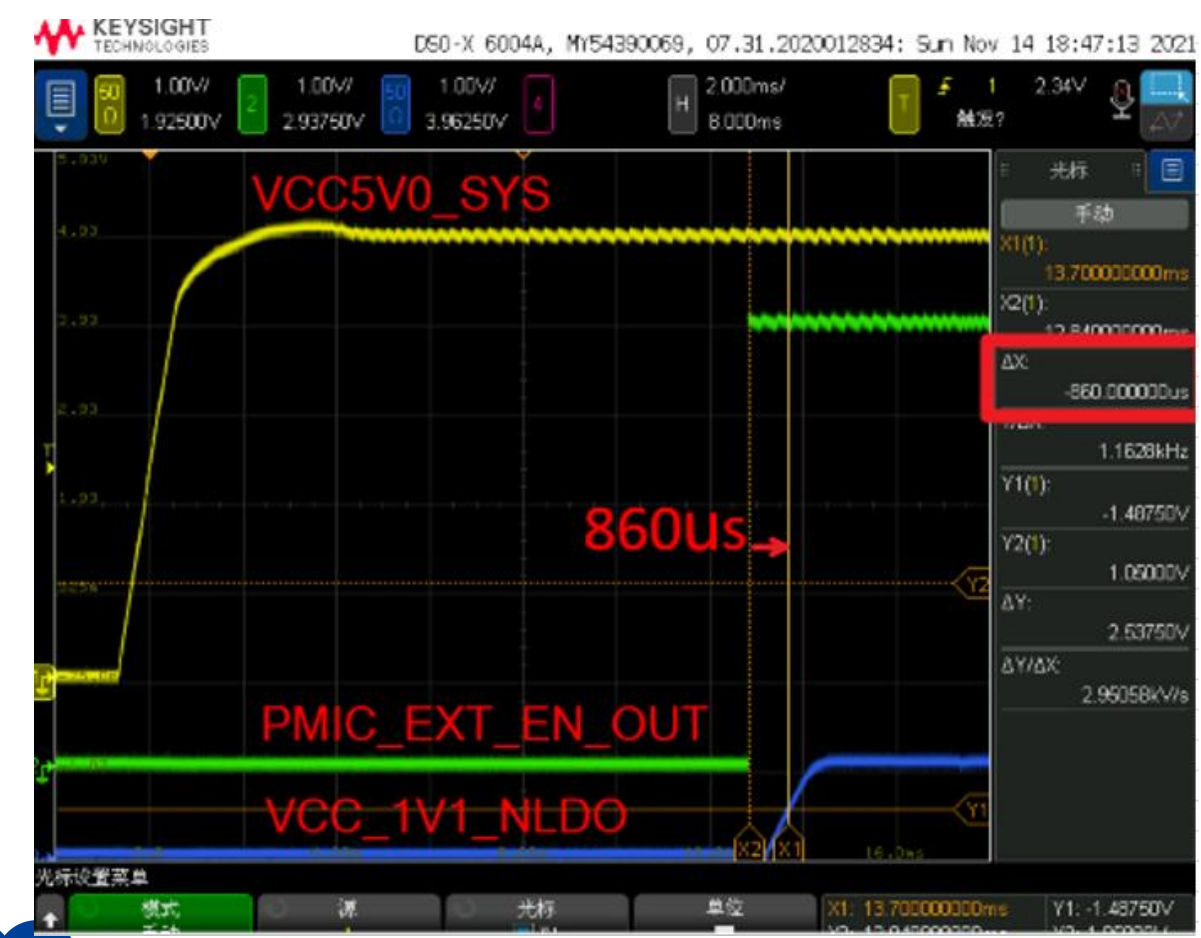
测试结果：

电源名称	Voltage Average(mV)	纹波（mV） 峰峰值	上冲	下陷	测试场场景/备注
VDD_CPU_BIG0	975.1	52.1	17.3	34.8	Antutu8.4.3
VDD_CPU_BIG1	975.47	46.2	15.63	30.57	Antutu8.4.3
VDD_CPU_LIT	875.87	30.6	12.53	18.07	Antutu8.4.3
VDD_GPU	796.07	71.9	34.13	37.77	Antutu8.4.3
VDD_NPU	771.23	35.6	18.37	17.23	mobilenet_v1模型(频率1GHz)
VDD_LOG	708.13	13.8	6.47	7.33	Antutu8.4.3
VDD_VDENC	723.35	15	6.96	8.04	编解码600M
VDD2_DDR_S3	1068.5	30	12.3	17.7	Antutu8.4.3
VDD_DDR_S0	815.41	45	24.39	20.61	Antutu8.4.3
VDDQ_DDR_S0	583.88	17.5	6.62	10.88	Antutu8.4.3
VCC_1V8_S3	1750.4	21.9	9.6	12.3	Antutu8.4.3
VCC_3V3_S3	3223.1	13.1	4.8	8.3	Antutu8.4.3
VCC_1V1_NLDO	1072	14.4	7.3	7.1	Antutu8.4.3
VCC_2V0_PLDO	1945.8	18.1	10.3	7.8	Antutu8.4.3
VCCA_1V8_S0	1752.5	9.4	可不填		stressapptest+USB30数据拷贝
VCC_1V8_S0	1761.6	11.3			stressapptest+两路HDMI TX显示
VDDA_1V2_S0	1162.8	11.3			stressapptest
VCCA_3V3_S0	3196.8	22.5			stressapptest+USB20数据拷贝
VDD_0V75_S3	723.05	19.4			stressapptest
VDDA_DDR_PLL_S0	820.46	7			stressapptest
VDDA_0V75_S0	740.8	7.9			stressapptest+两路HDMI TX显示 +USB20数据拷贝
VDDA_0V85_S0	812.45	6.3			stressapptest+USB30数据拷贝
VDD_0V75_S0	723.07	5.6			stressapptest+MIPI CSI显示

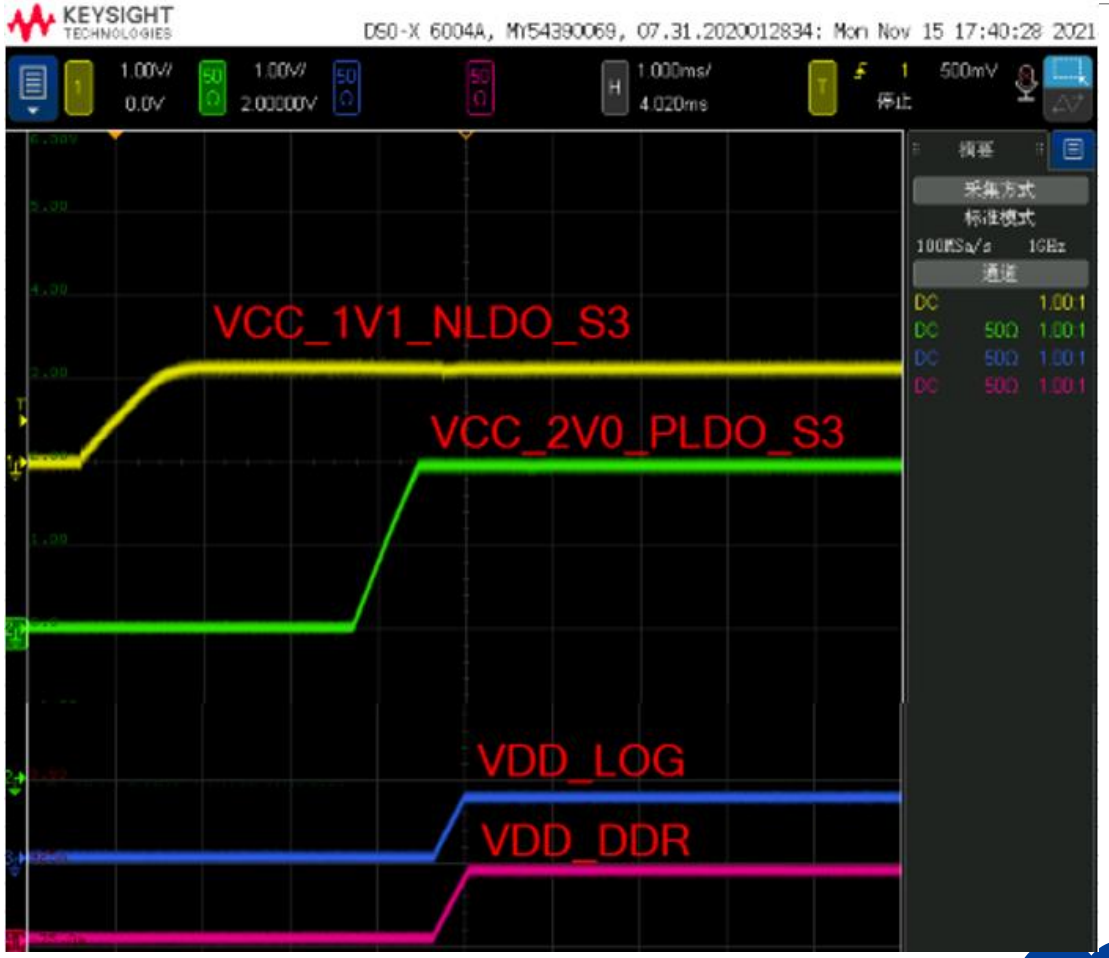
02.上电时序测试

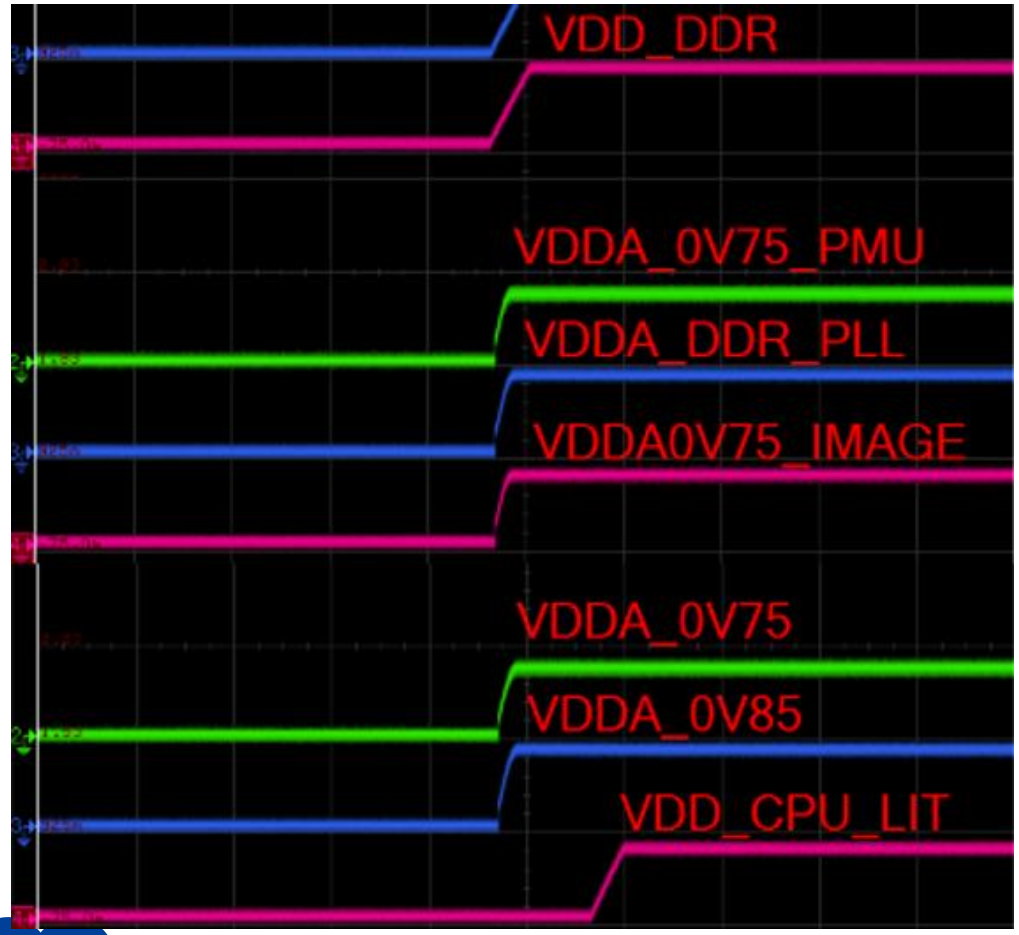
测试环境：RK3588 NVR DEMO，单RK806－1



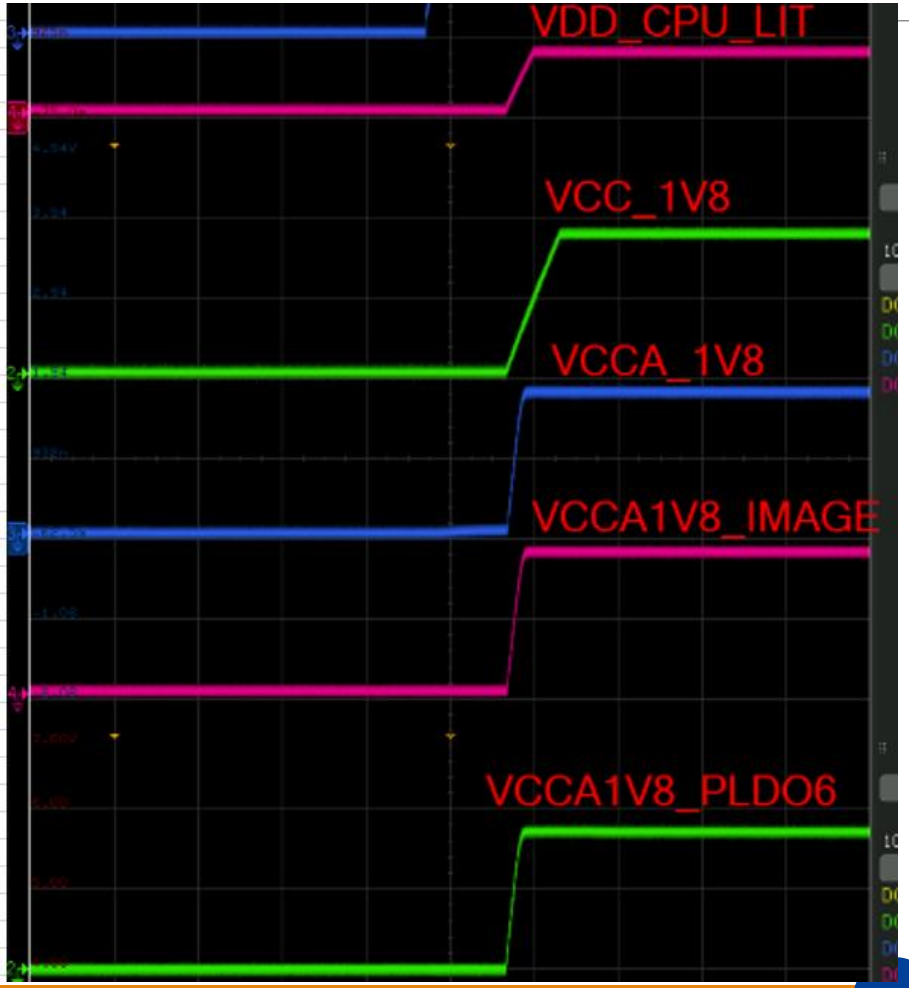


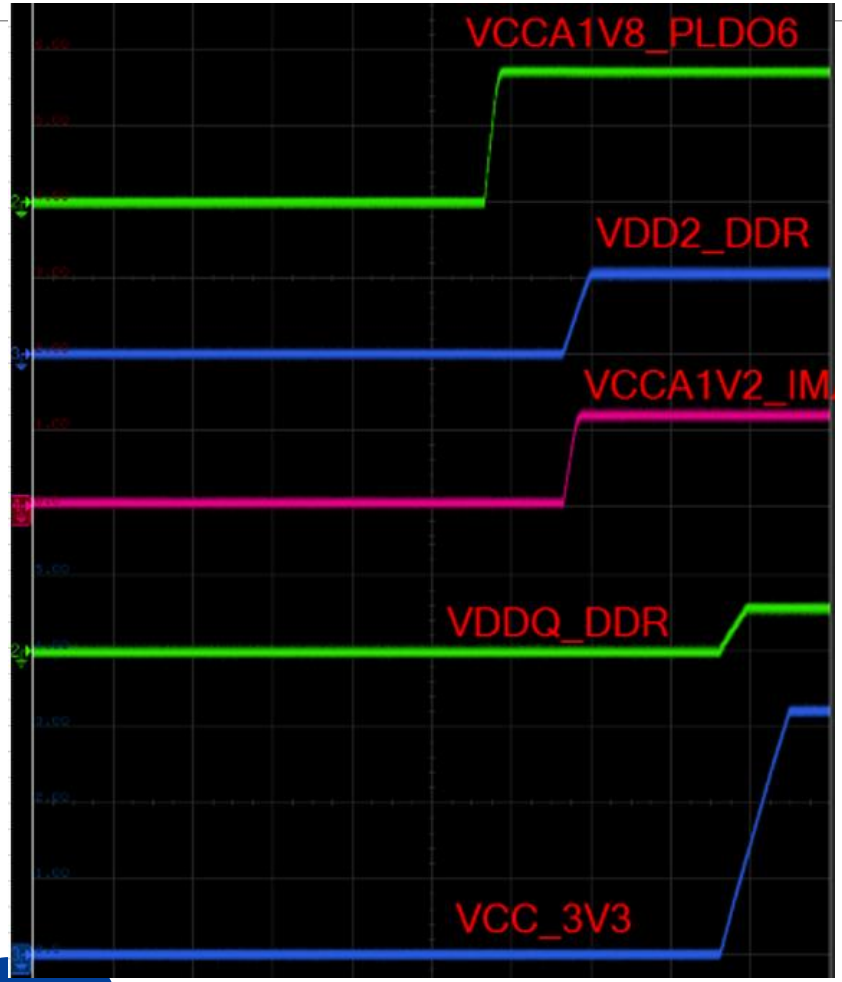
02.上电时序测试


KEYSIGHT TECHNOLOGIES
DSO-X 6004A, MY54390069, 07.31.2020012834: Mon Nov 15 17:40:28 2021
VCC_1V1_NLDO_S3
VCC_2V0_PLDO_S3
VDD_LOG
VDD_DDR

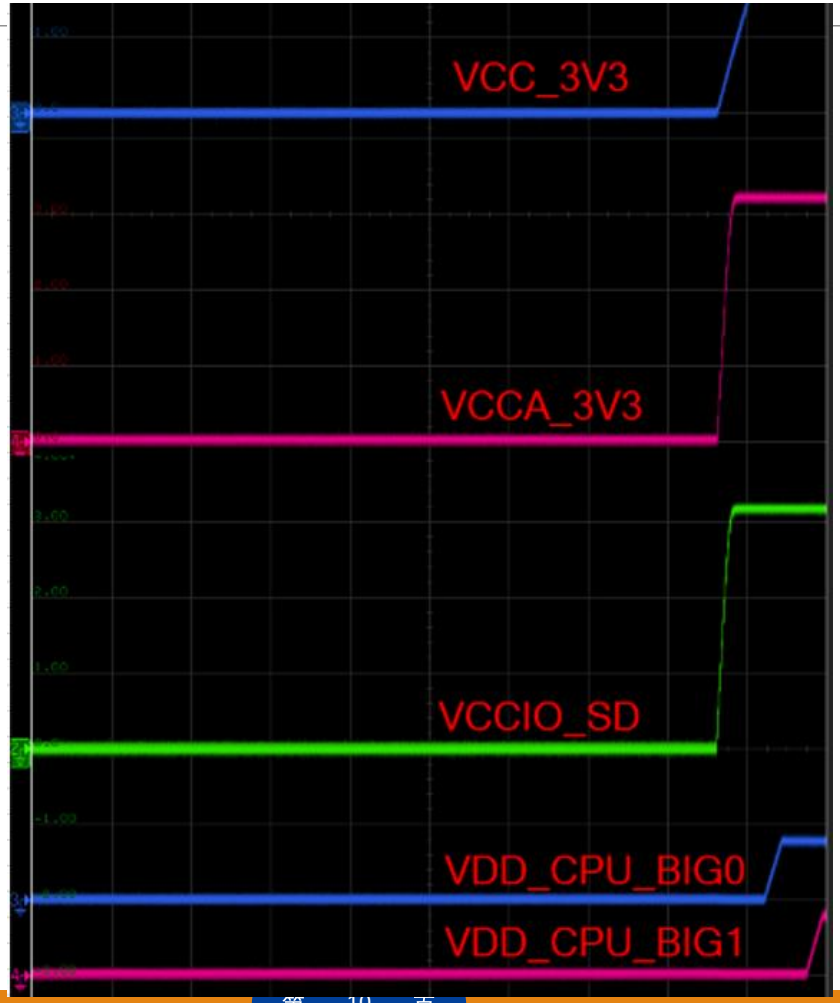

VDD_DDR
VDDA_0V75_PMU
VDDA_DDR_PLL
VDDA0V75_IMAGE
VDDA_0V75
VDDA_0V85
VDD_CPU_LIT

02.上电时序测试

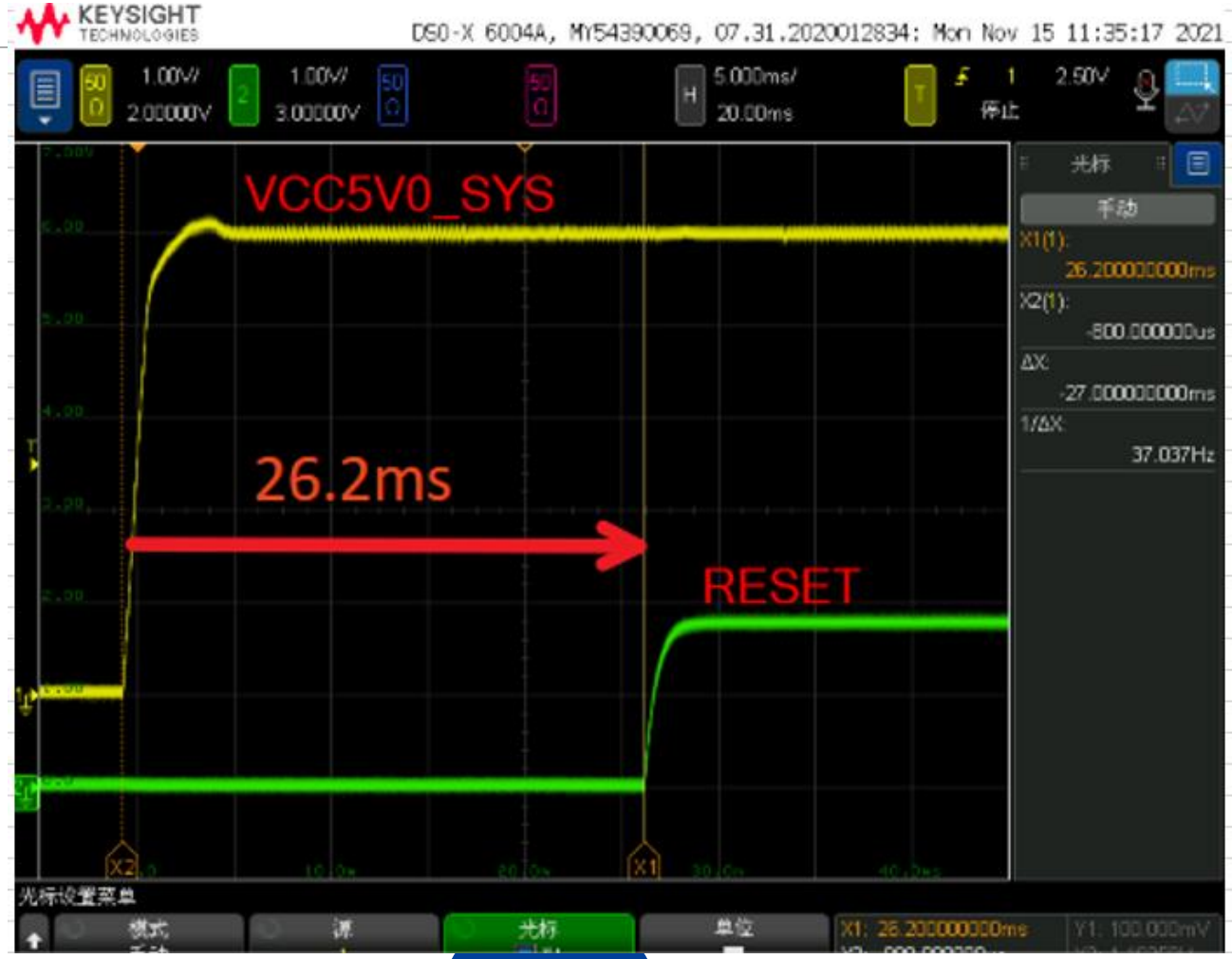

VDD_CPU_LIT
VCC_1V8
VCCA_1V8
VCCA1V8_IMAGE
VCCA1V8_PLDO6


VCCA1V8_PLDO6
VDD2_DDR
VCCA1V2_IM
VDDQ_DDR
VCC_3V3

02.上电时序测试



02.上电时序测试


KEYSIGHT TECHNOLOGIES
DSO-X 6004A, MY54390069, 07.31.2020012834: Mon Nov 15 11:35:17 2021
1.00V/
2.00000V
1.00V/
3.00000V
5.000ms/
20.00ms
停止
2.50V
光标
手动
X1(1):
26.200000000ms
X2(1):
-800.000000us
ΔX:
-27.000000000ms
1/ΔX:
37.037Hz
VCC5V0_SYS
26.2ms
RESET
光标设置菜单
模式
源
光标
单位
X1: 26.200000000ms
Y1: 100.000mV

03.功耗测试

RK3588各个核心模块的极限电流如下：

RK3588核心模块极限电流（高温）参考

测试条件：芯片结温100℃；
散热情况：裸板，无散热片；
测试方法：开发板工作稳定后，运行15分钟记录；
运行场景：不同模块在运行各自极限场景环境下测试所得；
注意：以下数据为内部研发板上的测试数据，仅供设计参考，不代表芯片的最终能力。功耗与产品实际应用场景强相关，如需深度优化，可与技术支持人员进一步探讨；

	电源网络	电压（V）	峰值电流（A）	峰值功率（W）	备注
核心模块极限电流	VDD_CPU_BIG0_S0	0.980	4.00	3.92	频率2400MHz
	VDD_CPU_BIG1_S0	0.980	4.00	3.92	频率2400MHz
	VDD_CPU_LIT_S0	0.950	3.00	2.85	频率1800MHz
	VDD_LOG_S0	0.750	2.50	1.88	
	VDD_GPU_S0	0.850	6.50	5.53	频率1000MHz
	VDD_NPU_S0	0.850	4.00	3.40	频率1000MHz
	VDD_VDENC_S0	0.775	2.50	1.94	频率750MHz
	VDD_DDR_S0	0.870	2.50	2.18	频率2112MHz

更详细的电流参数请参考发布的“RK3588 Power Consumption Test Report V1.1_20220829_CN ”

04.LPDDR4

LPDDR4 Test Report

Hardware Ver:	RK_NVR_DEMO_RK3588_LP4XD200P232SD8_V10_20210929new_final_lint.brd	Software Ver:	rk3588_spl_loader_v1.01.102_lcs.bin	TESTER:	谢晓圣	TEST DATA:	2021.11.26-12.6

Measurement Point

Power	Clock	Address Signal	Write DQS	Write DQ	Read DQS	Read DQ
	DDR_CH0_CLK_B ±	DDR_CH0_A3_B	DDR_CH0_DQS1_B ±	DDR_CH0_DQ9_B	DDR_CH0_DQS1_B ±	DDR_CH0_DQ8_B

Type	Frequency (MHz)	Supply(V)	Vref	Test Tool	Probe
LPDDR4-4266	2112	1.1		KEYSIGHT DSA91304A	KEYSIGHT 1169A(12Ghz)

Test name	Signal Name	Description	Test item	Unit	Spec limited			Measure		Test Result	Waveform	Remark
					Min	Tpical	Max	Min	Max			
CLK/CLK# Test (SDRAM die near-end)	CLK/CLK#	CK differential input voltage	Vindiff_CK	mV	360		--	1005		Pass	Vindiff CLK	
		Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	VIX(CK)	mv	-120		120	-50	43	Pass	VIX CLK	
		Single-ended Maximum amplitude for CK_t - CK_c	Vmax	V	--		1.4	0.452	0.511	Pass	Vmax CLK	
		Single-ended Minimum amplitude for CK_t - CK_c	Vmin	V	-0.3		--	-0.041	0.013	Pass	Vmin CLK	
		Average Clock Period	tCK(avg)	ns	0.469		100	0.473278	0.473715	Pass	tCK(avg)	
		Absolute Clock Period	tCK(abs)	ns	0.439			0.464		Pass	tCK(abs)	
		Absolute High Pulse Width	tCH(abs)	ns	0.20167		0.26733	0.228	0.245	Pass	tCH(abs)	
		Absolute Low Pulse Width	tCL(abs)	ns	0.20167		0.26733	0.23	0.24	Pass	tCL(abs)	
		Clock Period Jitter	tJIT(per)	ps	-30		30	-11	7	Pass	tJIT(per)	
		Cycle-to-Cycle Period Jitter	tJIT(cc)	ps	--		60	15	16	Pass	tJIT(cc)	
Address, CommandTest (SDRAM die near-end)	ADDRESSn	Maximum amplitude for Address, Command	Vmax	V	'--		1.4	0.573	0.615	Pass	Vmax CA	
		Minimum amplitude for Address, Command	Vmin	V	-0.3		--	-0.132		Pass	Vmin CA	
		Rx timing window total	TCIVW_total	ps			142.0454545		410	Pass	TCIVW total	测量示意图一
		Rx Mask voltage - p-p total	VCIVW_total	mV			145			Pass	VCIVW total	测量示意图一
		CA input pulse width	TCIPW	ps	284.0909091		--	435		Pass	TCIPW	测量示意图二
		CA AC input swing pk-pk	VIHL_AC	mV	180		--	742		Pass	VIHL AC	测量示意图三

04.LPDDR4

Write Test (SDRAM die near-end)	DQSn/DQSn#	DQS differential in-put voltage	Vindiff_DQS	mV	340		--	554	600	Pass	Vindiff_DQS_W	
		Max amplitude for DQS_t, DQS_c , TDQS_t, TDQS_c	Vmax	V	--		1.4	0.315	0.349	Pass	Vmax_DQS_W	
		Minimum amplitude for DQS_t, DQS_c , TDQS_t, TDQS_c	Vmin	V	-0.3		--	-0.024	0.012	Pass	Vmin_DQS_W	
		DQS latching transition to associated clock edge	tDQSS	ps	355.1136364		591.8560606	430	466	Pass	tDQSS	
		DQS input high pulse width	tDQSH	ps	189.3939394					Null	tDQSH	
		DQS input low pulse width	tDQSL	ps	189.3939394					Null	tDQSL	
		DQS falling edge to CK setup time	tDSS	ps	94.6969697		--	251		Pass	tDSS	
		DQS falling edge hold time from CK	tDSH	ps	94.6969697		--	200		Pass	tDSH	
	DQn /DMn/DBI	Maximum amplitude	Vmax	V	--		1.4	0.339	-0.004	Pass	Vmax_DQ_W	
		Minimum amplitude	Vmin	V	-0.3		--	-0.073	0.006	Pass	Vmin_DQ_W	
		Rx timing window total	TdIVW_total	ps			59.18560606			pass	TdIVW_total_W	测量示意图四
		Rx Mask voltage - p-p total	VdIVW_total	mV			120			pass	VdIVW_total_W	测量示意图四
		DQ input pulse width	TdIPW	ps	106.5340909		--	195		Pass	TdIPW_W	测量示意图五
		DQ AC input swing pk-pk	VIHL_AC	mV	170		--	473		Pass	VIHL_AC_W	测量示意图六
Read Test (CPU die near-end)	DQSn/DQSn#	DQS differential in-put voltage	Vindiff_DQS	mV	340		--	680	779	Pass	Vindiff_DQS_R	
		Maximum amplitude for DQS_t, DQS_c , TDQS_t, TDQS_c	Vmax	V	--		1.4		0.393	Pass	Vmax_DQS_R	
		Minimum amplitude for DQS_t, DQS_c , TDQS_t, TDQS_c	Vmin	V	-0.3		--	-0.052		Pass	Vmin_DQS_R	
	DQn /DMn	DQS Rise to DQ read High level time	tDQSQ-R-H	ps	--		42.61363636		35	Pass	tDQSQ-R-H	
		DQS Rise to DQ read Low level time	tDQSQ-R-L	ps	--		42.61363636		27	Pass	tDQSQ-R-L	
		DQS Fall to DQ read High level time	tDQSQ-F-H	ps	--		42.61363636		25	Pass	tDQSQ-F-H	
		DQS Fall to DQ read Low level time	tDQSQ-F-L	ps	--		42.61363636		28	Pass	tDQSQ-F-L	
		Rx Mask voltage - p-p total	VdIVW_total	mV	--		120			Pass	VdIVW_total_R	测量示意图四
		DQ input pulse width	TdIPW	ps	106.5340909		--	167		Pass	TdIPW_R	测量示意图五
		DQ AC input swing pk-pk	VIHL_AC	mV	170		--	521		Pass	VIHL_AC_R	测量示意图六

VDDQ (CPU die near-end) (SDRAM die near-end)	VDDQ	I/O buffer power	VDDQ	V	1.06	1.1	1.17			**Null**	VDDQ	
VDD2	VDD2	Core 2 power	VDD2	V	1.06	1.1	1.17			**Null**	VDD2	
VDD1 (CPU die near-end) (SDRAM die near-end)	VDD1	Core 1 power	VDD1	V	1.7	1.8	1.95			**Null**	VDD1	

05.LPDDR5

LPDDR5 Test Report(除了眼图，其他测试项见自动化测试报告)

Measurement Point								
Power	Clock	Address Signal	Control Signal	Write DQS	Write DQ	Read DQS	Read DQ	
	CLK_A	A2_A	CS0_A	DQS1_A	DQ11_A	DQS1_A	DQ10_A	
Type	Frequency (MHz)	Supply(V)	CA Vref	CS Vref	DQ Write Vref	DQ Read Vref	Test Tool	Probe
LPDDR5-5500	687.5	0.5	182.5mv	304mv	127mv	130mv	KEYSIGHT DSA91304A	KEYSIGHT 1169A(12Ghz)

Test name	Signal Name	Description	Test item	Unit	Spec limited			Measure		Test Result	Waveform	Remark
					Min	Tpical	Max	Min	Max			
CS Test (SDRAM die near-end)	CSn（SDR模式）	CS Rx mask width at VrefCS	tCSIVW1	ps	436.363636		'--			PASS	tCSIVW1	测量示意图一
		CS Rx mask width at vCSIVW	tCSIVW2	ps	320		'--			PASS	tCSIVW2	测量示意图一
		CS Rx mask height	vCSIVW	mV	180		'--			PASS	vCSIVW	测量示意图一
		CS Rx pulse width	tCSIPW	ps	872.727273		--	1388.9		Pass	tCSIPW	测量示意图一
		CS Rx pulse amplitude	vCSIHL_AC	mV	240		--	360.23		Pass	vCSIHL_AC	测量示意图一
Address, CommandTest (SDRAM die near-end)	ADDRESSn（DDR模式）	CA Rx mask width at Vref	tCIVW1	ps	218.181818		'--			PASS	tCIVW1	测量示意图二、三
		CA Rx mask width at vCIVW	tCIVW2	ps	130.909091		'--			PASS	tCIVW2	测量示意图二、三
		CA Rx mask height	vCIVW	mV	155		'--			PASS	vCIVW	测量示意图二、三
		CA Rx pulse width	tCIPW	ps	436.363636		--	675.8		Pass	tCIPW	测量示意图二、三
		CA Rx pulse amplitude	vCIHL_AC	mV	190		--	289.66		Pass	vCIHL_AC	测量示意图二、三
DQ Write Test (DRAM die near-end)	DQn /DMn	DQ Rx mask width at TBD	tDIVW1	ps	63.6363636		'--			PASS	tDIVW1	测量示意图四、五
		DQ Rx mask width at vDIVW	tDIVW2	ps	32.7272727		'--			PASS	tDIVW2	测量示意图四、五
		DQ Rx mask height	vDIVW	mV	100		'--			PASS	vDIVW	测量示意图四、五
		DQ Rx pulse width	tDIPW	ps	81.8181818		'--	144.47		Pass	tDIPW	测量示意图四、五
		DQ Rx pulse width above / below vDIVW	tDIHL	ps	45.4545455		--			PASS	tDIHL	测量示意图四、五
		DQ Rx pulse amplitude	vDIHL_AC	mV	140		--	198.33		Pass	vDIHL_AC	测量示意图四、五
DQ Read Test (CPU die near-end)	DQn /DMn	DQ Rx mask width at TBD	tDIVW1_R	ps	63.6363636		'--			PASS	tDIVW1_R	测量示意图四、五
		DQ Rx mask width at vDIVW	tDIVW2_R	ps	32.7272727		'--			PASS	tDIVW2_R	测量示意图四、五
		DQ Rx mask height	vDIVW_R	mV	100		'--			PASS	vDIVW_R	测量示意图四、五
		DQ Rx pulse width	tDIPW_R	ps	81.8181818		'--	139.97		Pass	tDIPW_R	测量示意图四、五
		DQ Rx pulse width above / below vDIVW	tDIHL_R	ps	45.4545455		--			PASS	tDIHL_R	测量示意图四、五
		DQ Rx pulse amplitude	vDIHL_AC_R	mV	140		--	179.59		Pass	vDIHL_AC_R	测量示意图四、五

eMMC SI Test Report

CLK Frequency (MHz)	IO Power Supply(V)	NOTE:
HS400	1.7-1.95	1.All timing values are measured relative to 50% of voltage level。 2.Rise and fall times are mearsured of voltage level(Please see below VOHmin、VOLmax、VIHmin、VILmax of the test table.) 建议先测试填写电源部分,为后面信号测试提供高低电平的参考。 3.测试结果根据指标要求，如果指标是大于等于Min值，则测试结果记录最小值。如果指标是小于等于Max值，则测试结果记录最大值。如果指标是大于等于Min值，同时小于等于Max值，则测试结果记录最小值和最大值。

Signal Name	Parameter	Test Item	Descriprion	Spec limited			Unit	Measure		Test Result	Test Waveform	Remark
				Min	Tpical	Max		Min	Max			
High-speed dual rate interface timing (referenced to CLK-DDR mode)	Clock	tPERIOD	CLK period	5			ns	5.05		Pass	tPERIOD	
		-	-				-			Null	-	
		CKSR	Slew rate	1.125			V/ns	1.629		Pass	CKSR	
		-	-				-			Null	-	
		tCKDCD	Duty cycle distortion	0		0.3	ns	0.09	0.11	Pass	tCKDCD	
		tCKMPW	Minimum pulse width	2.2				2.35		Pass	tCKMPW	
	Data Input	tISUddr	Data Input setup time	0.4			ns	0.904		Pass	tISUddr	
		tIHddr	Data Input hold time	0.4				0.854		Pass	tIHddr	
		DSR_IN	Data Input Slew Rate	1.125			V/ns	1.773		Pass	DSR_IN	
	Data Output	tRQ-DAT	Output skew			0.4	ns		0.285	Pass	tRQ-DAT	
		tRQH-DAT	Data Output hold skew			0.4	ns		0.358	Pass	tRQH-DAT	
		DSR-OUT	Data Output Slew Rate	1.125			V/ns	2.08		Pass	DSR-OUT	
		-	-				-			Null	-	
High-speed dual rate interface timing (referenced to CLK-SDR mode)	CMD Input	tISU-CMD	Input setup time	1.4			ns	2.5		Pass	tISU-CMD	
		tIH-CMD	Input Hold time	0.8				2.23		Pass	tIH-CMD	
	CMD Output	tRQ-CMD	Output skew			0.4	ns		0.236	Pass	tRQ-CMD	
		tRQH-CMD	Output hold skew			0.4			0.236	Pass	tRQH-CMD	
		CMDSR-OUT	CMD Output Slew rate	1.125			V/ns	2.419		Pass	CMDSR-OUT	
		-	-				-			Null	-	
High-speed dual rate interface timing (referenced to CLK-DDR mode)	DS	tPERIOD_DS	Data Strobe Cycle time	5			ns	5.05		Pass	tPERIOD_DS	
		DSSR	Data Strobe Slew Rate	1.125			V/ns	1.525		Pass	DSSR	
		tDSDCD	Data Strobe Duty Cycle Distortion Time	0		0.2	ns	0.115	0.14	Pass	tDSDCD	
		tDSMPW	Data Strobe Minimum Pulse Width Time	2				2.17		Pass	tDSMPW	
voltage	DC/AC	Vcc	Supply voltage (eMMC)	1.7		1.95	V	1.8	1.8	Pass	Vcc	
		tPRUL	Supply power-up Time for 1.8V			25	ms		0.493	Pass	tPRUL	
		VIHCLK	Input HIGH voltage			2.1	V		2.322	Fail	VIHCLK	
		VILCLK	Input LOW voltage	-0.3				-0.406		Fail	VILCLK	
		V_{IHData}	Input HIGH voltage	1.17		2.1		1.768	2.24	Fail	VIHData	
		V_{ILData}	Input LOW voltage	-0.3		0.63		0.031	0.107	Pass	VILData	

注意：信号有轻微上下冲，不影响EMMC的实际运行稳定性，风险可控。

eMMC SI Test Report

CLK Frequency (MHz)	IO Power Supply(V)	NOTE:
HS200	1.7-1.95	1.All timing values are measured relative to 50% of voltage level。 2.Rise and fall times are mearsured of voltage level(Please see below VOHmin、VOLmax、VIHmin、VILmax of the test table.) 建议先测试填写电源部分,为后面信号测试提供高低电平的参考。 3.测试结果根据指标要求，如果指标是大于等于Min值，则测试结果记录最小值。如果指标是小于等于Max值，则测试结果记录最大值。如果指标是大于等于Min值，同时小于等于Max值，则测试结果记录最小值和最大值。

Signal Name	Parameter	Test Item	Descriprion	Spec limited			Unit	Measure		Test Result	Test Waveform	Remark
				Min	Tpical	Max		Min	Max			
HS200 Clock signal timing	Clock	tPERIOD	CLK period	5			ns	5.05		Pass	tPERIOD	
		Duty Cycle	Clock duty cycle(includes jitter,phase noise)	30		70	%	48.3	50.9	Pass	Duty Cycle	
		-	-				-			Null	-	
		-	-				-			Null	-	
		tTLH	Clock rise time			1.01	ns		0.41	Pass	tTLH	
		tTHL	Clock fall time			1.01			0.419	Pass	tTHL	
	Data Input	tISU	Data Input setup time	1.4			ns	2.35		Pass	tISU	
		tIH	Data Input hold time	0.8				2.21		Pass	tIH	
		-	-				-			Null	-	
	Data Output	tPH	Device output momentary phasw from CLK input to CMD or DATA lines output			10.1	ns		1.54	Pass	tPH	
		tVW	tWH=2.88ns at 200MHz	2.90375			ns	3.63		Pass	tVW	
		-	-				-			Null	-	
		-	-				-			Null	-	
-	CMD Input	tISU-CMD	Input setup time	1.4			ns	2.46		Pass	tISU-CMD	
		tIH-CMD	Input Hold time	0.8				2.29		Pass	tIH-CMD	
	CMD Output	tPH	Device output momentary phasw from CLK input to CMD or DATA lines output			10.1	ns		1.3	Pass	tPH	
		tVW	tWH=2.88ns at 200MHz	2.90375				3.85		Pass	tVW	
		-	-				-			Null	-	
		-	-				-			Null	-	
-	-	-	-				-			Null	-	
		-	-				-			Null	-	
		-	-				-			Null	-	
		-	-							Null	-	
voltage	DC/AC	Vcc	Supply voltage (eMMC)	1.7		1.95	V	1.8	1.8	Pass	Vcc	
		tPRUL	Supply power-up Time for 1.8V			25	ms		0.493	Pass	tPRUL	
		V_{IHCLK}	Input HIGH voltage			2.1	V		1.926	Pass	VIHCLK	
		V_{ILCLK}	Input LOW voltage	-0.3				-0.111		Pass	VILCLK	
		V_{IHData}	Input HIGH voltage	1.17		2.1		1.769	1.952	Pass	VIHData	
		V_{ILData}	Input LOW voltage	-0.3		0.63		0.05	0.117	Pass	VILData	

PCIE30x4 GEN1测试综述

KEYSIGHT TECHNOLOGIES

Test Report

Overall Result PASS

Test Configuration Details	
Application	
Name	D9040PCIC PCI Express
Version	4.70.10.0
Test Session Details	
Infiniium SW Version	06.70.00001
Infiniium Model Number	DSOV254A
Infiniium Serial Number	MY61380102
Debug Mode Used	No
Last Test Date	2021-11-16 11:04:25 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	6
Total	6

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	RootComplex Tests, Unit Interval (2.5 GT/s)	400.00300 ps	48.8 %	399.88000 ps <= VALUE <= 400.12000 ps
✓	0	1	RootComplex Tests, Template Tests (2.5 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex Tests, Median to Max Jitter (2.5 GT/s)	19.43 ps	74.8 %	VALUE <= 77.00 ps
✓	0	1	RootComplex Tests, Eye-Width (2.5 GT/s)	373.03 ps	51.6 %	VALUE >= 246.00 ps
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s)	887.7 mV	35.9 %	274.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(2.5 GT/s)	812.4 mV	40.9 %	253.0 mV <= VALUE <= 1.2000 V

PCIE30x4 GEN2测试综述

KEYSIGHT TECHNOLOGIES

Test Report

Overall Result PASS

Test Configuration Details	
Application	
Name	D9040PCIC PCI Express
Version	4.70.10.0
Test Session Details	
Infiniium SW Version	06.70.00001
Infiniium Model Number	DSOV254A
Infiniium Serial Number	MY61380102
Debug Mode Used	No
Last Test Date	2021-11-16 11:13:09 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	12
Total	12

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	RootComplex Tests, Unit Interval (5.0 GT/s)	200.00200 ps	48.3 %	199.94000 ps <= VALUE <= 200.06000 ps
✓	0	1	RootComplex Tests, Template Tests (5.0 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Transition)(5.0 GT/s)	663.4 mV	45.0 %	225.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)	577.1 mV	36.1 %	225.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Eye-Width with crosstalk (5.0 GT/s)	163.23 ps	71.8 %	VALUE >= 95.00 ps
✓	0	1	RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)	2.136 ps	37.4 %	VALUE <= 3.410 ps
✓	0	1	RootComplex Tests, Maximum Deterministic Jitter with crosstalk (5.0 GT/s)	6.740 ps	88.2 %	VALUE <= 57.000 ps
✓	0	1	RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s)	36.768 ps	65.0 %	VALUE <= 105.000 ps
✓	0	1	RootComplex Tests, Eye-Width without crosstalk (5.0 GT/s)	162.99 ps	50.9 %	VALUE >= 108.00 ps
✓	0	1	RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)	2.113 ps	38.0 %	VALUE <= 3.410 ps
✓	0	1	RootComplex Tests, Maximum Deterministic Jitter without crosstalk (5.0 GT/s)	7.307 ps	83.4 %	VALUE <= 44.000 ps
✓	0	1	RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s)	37.012 ps	59.8 %	VALUE <= 92.000 ps

PCIE30x4 GEN3测试综述

KEYSIGHT TECHNOLOGIES

Test Report

Overall Result: PASS

Test Configuration Details	
Application	
Name	D9040PCIC PCI Express
Version	4.70.10.0
Test Session Details	
Infiniium SW Version	06.70.00001
Infiniium Model Number	DSOV254A
Infiniium Serial Number	MY61380102
Debug Mode Used	No
Last Test Date	2021-11-16 11:31:58 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	5
Total	5

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	RootComplex Tests, Unit Interval (8.0 GT/s)	125.00400 ps	45.0 %	124.98000 ps <= VALUE <= 125.04000 ps
✓	0	1	RootComplex Tests, Template Tests (8.0 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Transition)(8.0 GT/s)	324.5 mV	24.9 %	34.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(8.0 GT/s)	329.8 mV	25.4 %	34.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Eye-Width (8.0 GT/s)	96.17 ps	133.1 %	VALUE >= 41.25 ps

08.PCIE2.0

RK3588_PCIE2.0_DATA_5G

KEYSIGHT TECHNOLOGIES

Test Report

Overall Result: PASS

Test Configuration Details	
Application	
Name	D9040PCIC PCI Express
Version	4.70.10.0
Test Session Details	
Infiniium SW Version	06.60.00601
Infiniium Model Number	DSO91304A
Infiniium Serial Number	MY52260147
Debug Mode Used	No
Last Test Date	2022-03-05 11:33:23 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	12
Total	12

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	RootComplex Tests, Unit Interval (5.0 GT/s)	200.00500 ps	45.8 %	199.94000 ps <= VALUE <= 200.06000 ps
✓	0	1	RootComplex Tests, Template Tests (5.0 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Transition)(5.0 GT/s)	638.0 mV	37.6 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)	596.1 mV	32.9 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Eye-Width with crosstalk (5.0 GT/s)	150.45 ps	58.4 %	VALUE >= 95.00 ps
ⓘ		1	RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)	2.175 ps		Information Only
✓	0	1	RootComplex Tests, Maximum Deterministic Jitter with crosstalk (5.0 GT/s)	18.963 ps	66.7 %	VALUE <= 57.000 ps
✓	0	1	RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s)	49.545 ps	52.8 %	VALUE <= 105.000 ps
✓	0	1	RootComplex Tests, Eye-Width without crosstalk (5.0 GT/s)	150.60 ps	39.4 %	VALUE >= 108.00 ps
ⓘ		1	RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)	2.161 ps		Information Only
✓	0	1	RootComplex Tests, Maximum Deterministic Jitter without crosstalk (5.0 GT/s)	19.014 ps	56.8 %	VALUE <= 44.000 ps
✓	0	1	RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s)	49.398 ps	46.3 %	VALUE <= 92.000 ps

08.PCIE2.0

RK3588_PCIE2.0_CLK_5G

KEYSIGHT TECHNOLOGIES

Test Report

Overall Result: PASS

Test Configuration Details	
Application	
Name	D9040PCIC PCI Express
Version	4.70.10.0
Test Session Details	
Infiniium SW Version	06.60.00601
Infiniium Model Number	DSO91304A
Infiniium Serial Number	MY52260147
Debug Mode Used	No
Last Test Date	2022-03-05 11:24:00 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	4
Total	4

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)	2.76 ps	11.0 %	VALUE <= 3.10 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)	910 fs	69.7 %	VALUE <= 3.00 ps
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)	3.44 ps	14.0 %	VALUE <= 4.00 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)	1.15 ps	84.7 %	VALUE <= 7.50 ps

09.SATA3.0

RK3588_SATA_6G

Summary of Results

Test Statistics	
Failed	0
Passed	25
Total	25

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	PHY-01 : Channel Speed, FBaud & Unit Interval (Gen3)	166.9697 ps	38.0 %	166.6083 ps <= VALUE <= 167.5583 ps
✓	0	1	PHY-03 : Spread-Spectrum Modulation Frequency	31.105 kHz	36.8 %	30.000 kHz <= VALUE <= 33.000 kHz
✓	0	1	PHY-04[a] : Spread-Spectrum Modulation Deviation (Min)	-4.149 kppm of Fbaud	21.1 %	-5.350 kppm of Fbaud <= VALUE <= 350 ppm of Fbaud
✓	0	1	PHY-04[b] : Spread-Spectrum Modulation Deviation (Max)	94 ppm of Fbaud	4.5 %	-5.350 kppm of Fbaud <= VALUE <= 350 ppm of Fbaud
✓	0	1	PHY-04[c] : Spread-Spectrum Modulation DFDT (Min) (Informative)	-880 ppm/us	14.8 %	-1.250 kppm/us <= VALUE <= 1.250 kppm/us
✓	0	1	PHY-04[d] : Spread-Spectrum Modulation DFDT (Max) (Informative)	922 ppm/us	13.1 %	-1.250 kppm/us <= VALUE <= 1.250 kppm/us
✓	0	1	TSG-02[a] : Rise Time (Gen3) (Informative)	68.67 ps	24.1 %	33.00 ps <= VALUE <= 80.00 ps
✓	0	1	TSG-02[b] : Fall Time (Gen3) (Informative)	68.73 ps	24.0 %	33.00 ps <= VALUE <= 80.00 ps
✓	0	1	TSG-03[a] : Differential Skew, HFTP (Gen1, Gen2, Gen3) (Informative)	2.90 ps	85.5 %	VALUE <= 20.00 ps
✓	0	1	TSG-03[b] : Differential Skew, MFTP (Gen1, Gen2, Gen3) (Informative)	2.06 ps	89.7 %	VALUE <= 20.00 ps
✓	0	1	TSG-04[a] : AC Common Mode Voltage, MFTP (Gen3)	8.83 mV	92.6 %	VALUE <= 120.00 mV
✓	0	1	TSG-04[b] : AC Common Mode Voltage, HFTP (Gen3)	12.71 mV	89.4 %	VALUE <= 120.00 mV
✓	0	1	TSG-13[d] : TJ after CIC, LBP, Clock To Data, JTF Defined (BER=1E-12) (Gen3)	335.90 mUI	35.4 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, LBP, Clock To Data, JTF Defined (BER=1E-6) (Gen3)	260.80 mUI	43.3 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, HFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	217.60 mUI	58.2 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, HFTP, Clock To Data, JTF Defined (BER=1E-6) (Gen3) (Informative)	160.20 mUI	65.2 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, MFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	213.30 mUI	59.0 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, MFTP, Clock To Data, JTF Defined (BER=1E-6) (Gen3) (Informative)	152.20 mUI	66.9 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, LFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	221.30 mUI	57.4 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, LFTP, Clock To Data, JTF Defined (BER=1E-6) (Gen3) (Informative)	162.40 mUI	64.7 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, SSOP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	333.20 mUI	35.9 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, SSOP, Clock To Data, JTF Defined (BER=1E-6) (Gen3) (Informative)	259.80 mUI	43.5 %	VALUE <= 460.00 mUI
✓	0	1	TSG-14 : TX Maximum Differential Voltage Amplitude (Gen3)	684.00 mV	24.0 %	VALUE <= 900.00 mV
✓	0	1	TSG-15 : TX Minimum Differential Voltage Amplitude (UI=5E6) (Gen3)	302.70 mV	51.4 %	VALUE >= Vdiff_Min_Gen3i_Limit V
✓	0	1	TSG-17[b] : Tx Emphasis, MFTP (Host) (Gen3)	-1.667 dB	9.5 %	-2.000 dB <= VALUE <= 1.500 dB

09.SATA3.0

RK3588_SATA_6G

Summary of Results

Test Statistics	
Failed	0
Passed	21
Total	21

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	PHY-01 : Channel Speed, FBaud & Unit Interval (Gen3)	166.6712 ps	6.6 %	166.6083 ps <= VALUE <= 167.5583 ps
✓	0	1	PHY-02 : Frequency Long-Term Stability / Accuracy (Gen3)	-27 ppm	46.1 %	-350 ppm <= VALUE <= 350 ppm
✓	0	1	TSG-02[a] : Rise Time (Gen3) (Informative)	65.39 ps	31.1 %	33.00 ps <= VALUE <= 80.00 ps
✓	0	1	TSG-02[b] : Fall Time (Gen3) (Informative)	65.73 ps	30.4 %	33.00 ps <= VALUE <= 80.00 ps
✓	0	1	TSG-03[a] : Differential Skew, HFTP (Gen1, Gen2, Gen3) (Informative)	5.85 ps	70.8 %	VALUE <= 20.00 ps
✓	0	1	TSG-03[b] : Differential Skew, MFTP (Gen1, Gen2, Gen3) (Informative)	6.05 ps	69.8 %	VALUE <= 20.00 ps
✓	0	1	TSG-04[a] : AC Common Mode Voltage, MFTP (Gen3)	17.54 mV	85.4 %	VALUE <= 120.00 mV
✓	0	1	TSG-04[b] : AC Common Mode Voltage, HFTP (Gen3)	24.49 mV	79.6 %	VALUE <= 120.00 mV
✓	0	1	TSG-13[d] : TJ after CIC, LBP, Clock To Data, JTF Defined (BER=1E-12) (Gen3)	327.80 mUI	37.0 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, LBP, Clock To Data, JTF Defined (BER=1E-6) (Gen3)	272.40 mUI	40.8 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, HFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	198.70 mUI	61.8 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, HFTP, Clock To Data, JTF Defined (BER=1E-6) (Gen3) (Informative)	129.00 mUI	72.0 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, MFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	204.60 mUI	60.7 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, MFTP, Clock To Data, JTF Defined (BER=1E-6) (Gen3) (Informative)	141.20 mUI	69.3 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, LFTP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	207.00 mUI	60.2 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, LFTP, Clock To Data, JTF Defined (BER=1E-6) (Gen3) (Informative)	142.90 mUI	68.9 %	VALUE <= 460.00 mUI
✓	0	1	TSG-13[d] : TJ after CIC, SSOP, Clock To Data, JTF Defined (BER=1E-12) (Gen3) (Informative)	317.10 mUI	39.0 %	VALUE <= 520.00 mUI
✓	0	1	TSG-13[e] : TJ after CIC, SSOP, Clock To Data, JTF Defined (BER=1E-6) (Gen3) (Informative)	270.00 mUI	41.3 %	VALUE <= 460.00 mUI
✓	0	1	TSG-14 : TX Maximum Differential Voltage Amplitude (Gen3)	753.70 mV	16.3 %	VALUE <= 900.00 mV
✓	0	1	TSG-15 : TX Minimum Differential Voltage Amplitude (UI=5E6) (Gen3)	312.10 mV	56.1 %	VALUE >= Vdiff_Min_Gen3i_Limit V
✓	0	1	TSG-17[b] : Tx Emphasis, MFTP (Host) (Gen3)	-1.497 dB	14.4 %	-2.000 dB <= VALUE <= 1.500 dB

10.HDMI TX

hdmi1.4_1920x1080x60Hz

Summary of Results

Test Statistics	
Failed	0
Passed	32
Total	32

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	7-9: Clock Jitter	36 mTbit	85.6 %	VALUE <= 250 mTbit
✓	0	1	7-4: Clock Rise Time	110.881 ps	47.8 %	VALUE >= 75.000 ps
✓	0	1	7-4: Clock Fall Time	109.416 ps	45.9 %	VALUE >= 75.000 ps
✓	0	1	7-8: Clock Duty Cycle(Minimum)	49.954	24.9 %	>=40%
✓	0	1	7-8: Clock Duty Cycle(Maximum)	50.082	16.5 %	<=60%
✓	0	1	7-2: VL Clock +	2.813 V	29.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL Clock -	2.801 V	33.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Clock	2 mTbit	49.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-10: D0 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	1	7-10: D0 Data Jitter	38 m	87.3 %	<=0.3Tbit
✓	0	1	7-4: D0 Rise Time	100.649 ps	34.2 %	VALUE >= 75.000 ps
✓	0	1	7-4: D0 Fall Time	101.496 ps	35.3 %	VALUE >= 75.000 ps
✓	0	1	7-2: VL D0+	2.810 V	30.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D0-	2.811 V	29.7 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 0	-4 mTbit	48.7 %	-150 mTbit <= VALUE <= 150 mTbit

10.HDMI TX

✓	0	1	7-10: D1 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	1	7-10: D1 Data Jitter	37 m	87.7 %	<=0.3Tbit
✓	0	1	7-4: D1 Rise Time	92.904 ps	23.9 %	VALUE >= 75.000 ps
✓	0	1	7-4: D1 Fall Time	91.817 ps	22.4 %	VALUE >= 75.000 ps
✓	0	1	7-2: VL D1+	2.804 V	32.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D1-	2.805 V	31.7 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 1	-10 mTbit	46.7 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-10: D2 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	1	7-10: D2 Data Jitter	36 m	88.0 %	<=0.3Tbit
✓	0	1	7-4: D2 Rise Time	100.412 ps	33.9 %	VALUE >= 75.000 ps
✓	0	1	7-4: D2 Fall Time	97.366 ps	29.8 %	VALUE >= 75.000 ps
✓	0	1	7-2: VL D2+	2.810 V	30.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D2-	2.805 V	31.7 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 2	-12 mTbit	46.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-6: Inter-Pair Skew - D0/D2	-800 碌Tpixel	49.8 %	-200 mTpixel <= VALUE <= 200 mTpixel
✓	0	1	7-6: Inter-Pair Skew - D1/D2	-700 碌Tpixel	49.8 %	-200 mTpixel <= VALUE <= 200 mTpixel
✓	0	1	7-6: Inter-Pair Skew - D0/D1	-2 mTpixel	49.5 %	-200 mTpixel <= VALUE <= 200 mTpixel

10.HDMI TX

hdmi2.0_4k_60Hz

Summary of Results

Test Statistics	
Failed	0
Passed	32
Total	32

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	5	7-9: Clock Jitter	81 mTbit	67.6 %	VALUE <= 250 mTbit
✓	0	5	7-4: Clock Rise Time	95.362 ps	27.1 %	VALUE >= 75.000 ps
✓	0	5	7-4: Clock Fall Time	98.641 ps	31.5 %	VALUE >= 75.000 ps
✓	0	5	7-8: Clock Duty Cycle(Minimum)	49.922	24.8 %	>=40%
✓	0	5	7-8: Clock Duty Cycle(Maximum)	50.209	16.3 %	<=60%
✓	0	5	7-2: VL Clock +	2.824 V	25.3 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	7-2: VL Clock -	2.819 V	27.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	7-7: Intra-Pair Skew - Clock	-28 mTbit	40.7 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	5	7-10: D2 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	5	7-10: D2 Data Jitter	81 m	73.0 %	<=0.3Tbit
✓	0	5	7-4: D2 Rise Time	84.832 ps	13.1 %	VALUE >= 75.000 ps
✓	0	5	7-4: D2 Fall Time	81.923 ps	9.2 %	VALUE >= 75.000 ps

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✓	0	5	7-2: VL D2+	2.815 V	28.3 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	7-2: VL D2-	2.818 V	27.3 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	7-7: Intra-Pair Skew - Data Lane 2	-21 mTbit	43.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	5	7-10: D0 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	5	7-10: D0 Data Jitter	83 m	72.3 %	<=0.3Tbit
✓	0	5	7-4: D0 Rise Time	90.687 ps	20.9 %	VALUE >= 75.000 ps
✓	0	5	7-4: D0 Fall Time	89.428 ps	19.2 %	VALUE >= 75.000 ps
✓	0	5	7-2: VL D0+	2.816 V	28.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	7-2: VL D0-	2.828 V	24.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	7-7: Intra-Pair Skew - Data Lane 0	-12 mTbit	46.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	5	7-10: D1 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	5	7-10: D1 Data Jitter	113 m	62.3 %	<=0.3Tbit
✓	0	5	7-4: D1 Rise Time	87.437 ps	16.6 %	VALUE >= 75.000 ps
✓	0	5	7-4: D1 Fall Time	88.462 ps	17.9 %	VALUE >= 75.000 ps
✓	0	5	7-2: VL D1-	2.819 V	27.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	5	7-7: Intra-Pair Skew - Data Lane 1	-17 mTbit	44.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	5	7-2: VL D1+	2.816 V	28.0 %	Low erLimit V <= VALUE <= 2.900 V
✓	0	4	7-6: Inter-Pair Skew - D0/D1	-3 mTpixel	49.3 %	-200 mTpixel <= VALUE <= 200 mTpixel
✓	0	4	7-6: Inter-Pair Skew - D1/D2	-5 mTpixel	48.8 %	-200 mTpixel <= VALUE <= 200 mTpixel
✓	0	4	7-6: Inter-Pair Skew - D0/D2	-4 mTpixel	49.0 %	-200 mTpixel <= VALUE <= 200 mTpixel

10.HDMI TX

FRL_12G

Summary of Results

Test Statistics	
Failed	0
Passed	81
Total	81

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
ⓘ		1	Save Lane D3 Waveform (TP1) (LTP8) (All lanes transmit)	0.000		Information Only
ⓘ		1	Save Lane D3 Waveform (TP1) (LTP8)	0.000		Information Only
ⓘ		1	Save Lane D3 Waveform (TP1) (LTP3)	0.000		Information Only
ⓘ		1	Save Lane D3 Waveform (TP1) (LTP4)	0.000		Information Only
ⓘ		1	Save Lane D0 Waveform (TP1) (LTP5) (All lanes transmit)	0.000		Information Only
ⓘ		1	Save Lane D0 Waveform (TP1) (LTP5)	0.000		Information Only

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ⓘ		1	Save Lane D0 Waveform (TP1) (LTP3)	0.000		Information Only
ⓘ		1	Save Lane D0 Waveform (TP1) (LTP4)	0.000		Information Only
ⓘ		1	Save Lane D3 and D0 Waveform	0.000		Information Only
ⓘ		1	Save Lane D1 Waveform (TP1) (LTP6) (All lanes transmit)	0.000		Information Only
ⓘ		1	Save Lane D1 Waveform (TP1) (LTP6)	0.000		Information Only
ⓘ		1	Save Lane D1 Waveform (TP1) (LTP3)	0.000		Information Only
ⓘ		1	Save Lane D1 Waveform (TP1) (LTP4)	0.000		Information Only
ⓘ		1	Save Lane D2 Waveform (TP1) (LTP7)	0.000		Information Only
ⓘ		1	Save Lane D2 Waveform (TP1) (LTP3)	0.000		Information Only
ⓘ		1	Save Lane D2 Waveform (TP1) (LTP4)	0.000		Information Only
ⓘ		1	Save Lane D1 and D2 Waveform	0.000		Information Only
ⓘ		1	Save Lane D2 Waveform (TP1) (LTP7) (All lanes transmit)	0.000		Information Only
ⓘ		1	Save Lane D0 and D1 Waveform	0.000		Information Only
✓	0	1	HFR1-3: D3+ Rise Slew Rate	3.771 mV/ps	76.4 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D3- Rise Slew Rate	4.087 mV/ps	74.6 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D3+ Fall Slew Rate	4.129 mV/ps	74.2 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D3- Fall Slew Rate	4.207 mV/ps	73.7 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-1: D3 DC Common Mode	3.301 V	3.5 %	2.500 V <= VALUE <= 3.330 V
✓	0	1	HFR1-2: Vse Min D3+	3.085 V	5.5 %	VALUE >= FRLVseMinLimit V
✓	0	1	HFR1-2: Vse Max D3+	3.516 V	4.3 %	VALUE <= FRLVseMaxLimit V
✓	0	1	HFR1-2: Vse Min D3-	3.088 V	5.6 %	VALUE >= FRLVseMinLimit V
✓	0	1	HFR1-2: Vse Max D3-	3.518 V	4.3 %	VALUE <= FRLVseMaxLimit V

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✓	0	1	HFR1-5: D3 Data Rate	-23.740 ppm	46.0 %	-300.000 ppm <= VALUE <= 300.000 ppm
✓	0	1	HFR1-8: D3 AC Common Mode Noise	42 mV	72.0 %	VALUE <= 150 mV
✓	0	1	HFR1-6: D3 RJ Measurement Test	78 mTbit	38.7 %	1 mTbit <= VALUE <= 200 mTbit
✓	0	1	HFR1-7: D3 Eye Mask Test - Category 3 Worst Cable Model (WCM3)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-7: D3 Eye Mask Test - Category 3 Short Cable Model (SCM3)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-3: D0+ Rise Slew Rate	4.017 mV/ps	74.9 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D0- Rise Slew Rate	4.118 mV/ps	74.3 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D0+ Fall Slew Rate	4.158 mV/ps	74.0 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D0- Fall Slew Rate	4.321 mV/ps	73.0 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-1: D0 DC Common Mode	3.300 V	3.6 %	2.500 V <= VALUE <= 3.330 V
✓	0	1	HFR1-2: Vse Min D0+	3.085 V	5.5 %	VALUE >= FRLVseMinLimit V
✓	0	1	HFR1-2: Vse Max D0+	3.518 V	4.3 %	VALUE <= FRLVseMaxLimit V
✓	0	1	HFR1-2: Vse Min D0-	3.082 V	5.4 %	VALUE >= FRLVseMinLimit V
✓	0	1	HFR1-2: Vse Max D0-	3.517 V	4.3 %	VALUE <= FRLVseMaxLimit V
✓	0	1	HFR1-5: D0 Data Rate	-23.968 ppm	46.0 %	-300.000 ppm <= VALUE <= 300.000 ppm
✓	0	1	HFR1-8: D0 AC Common Mode Noise	52 mV	65.3 %	VALUE <= 150 mV
✓	0	1	HFR1-6: D0 RJ Measurement Test	77 mTbit	38.2 %	1 mTbit <= VALUE <= 200 mTbit
✓	0	1	HFR1-7: D0 Eye Mask Test - Category 3 Worst Cable Model (WCM3)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-7: D0 Eye Mask Test - Category 3 Short Cable Model (SCM3)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-3: D1+ Rise Slew Rate	3.923 mV/ps	75.5 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D1- Rise Slew Rate	4.060 mV/ps	74.6 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D1+ Fall Slew Rate	4.169 mV/ps	73.9 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D1- Fall Slew Rate	4.260 mV/ps	73.4 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-1: D1 DC Common Mode	3.300 V	3.6 %	2.500 V <= VALUE <= 3.330 V
✓	0	1	HFR1-2: Vse Min D1+	3.091 V	5.7 %	VALUE >= FRLVseMinLimit V
✓	0	1	HFR1-2: Vse Max D1+	3.516 V	4.3 %	VALUE <= FRLVseMaxLimit V
✓	0	1	HFR1-2: Vse Min D1-	3.080 V	5.3 %	VALUE >= FRLVseMinLimit V
✓	0	1	HFR1-2: Vse Max D1-	3.524 V	4.1 %	VALUE <= FRLVseMaxLimit V

10.HDMI TX

✓	0	1	HFR1-5: D1 Data Rate	-24.403 ppm	45.9 %	-300.000 ppm <= VALUE <= 300.000 ppm
✓	0	1	HFR1-8: D1 AC Common Mode Noise	35 mV	76.7 %	VALUE <= 150 mV
✓	0	1	HFR1-6: D1 RJ Measurement Test	78 mTbit	38.7 %	1 mTbit <= VALUE <= 200 mTbit
✓	0	1	HFR1-7: D1 Eye Mask Test - Category 3 Worst Cable Model (WCM3)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-7: D1 Eye Mask Test - Category 3 Short Cable Model (SCM3)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-3: D2+ Rise Slew Rate	4.221 mV/ps	73.6 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D2- Rise Slew Rate	4.127 mV/ps	74.2 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D2+ Fall Slew Rate	4.408 mV/ps	72.5 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-3: D2- Fall Slew Rate	4.406 mV/ps	72.5 %	VALUE <= 16.000 mV/ps
✓	0	1	HFR1-1: D2 DC Common Mode	3.300 V	3.6 %	2.500 V <= VALUE <= 3.330 V
✓	0	1	HFR1-2: Vse Min D2+	3.083 V	5.4 %	VALUE >= FRLVseMinLimit V
✓	0	1	HFR1-2: Vse Max D2+	3.515 V	4.4 %	VALUE <= FRLVseMaxLimit V
✓	0	1	HFR1-2: Vse Min D2-	3.082 V	5.4 %	VALUE >= FRLVseMinLimit V
✓	0	1	HFR1-2: Vse Max D2-	3.519 V	4.2 %	VALUE <= FRLVseMaxLimit V
✓	0	1	HFR1-5: D2 Data Rate	-24.018 ppm	46.0 %	-300.000 ppm <= VALUE <= 300.000 ppm
✓	0	1	HFR1-8: D2 AC Common Mode Noise	50 mV	66.7 %	VALUE <= 150 mV
✓	0	1	HFR1-6: D2 RJ Measurement Test	78 mTbit	38.7 %	1 mTbit <= VALUE <= 200 mTbit
✓	0	1	HFR1-7: D2 Eye Mask Test - Category 3 Worst Cable Model (WCM3)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-7: D2 Eye Mask Test - Category 3 Short Cable Model (SCM3)	0.000	50.0 %	No Mask Failures
✓	0	1	HFR1-4: Inter-Pair Skew - D3/D0	39 mTBit	49.5 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit
✓	0	1	HFR1-4: Inter-Pair Skew - D1/D2	5 mTBit	49.9 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit
✓	0	1	HFR1-4: Inter-Pair Skew - D0/D1	-101 mTBit	48.7 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit
✓	0	1	HFR1-4: Inter-Pair Skew - D3/D1	-62 mTBit	49.2 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit
✓	0	1	HFR1-4: Inter-Pair Skew - D3/D2	-57 mTBit	49.3 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit
✓	0	1	HFR1-4: Inter-Pair Skew - D0/D2	-96 mTBit	48.8 %	InterpairSkew ThresholdNeg TBit <= VALUE <= InterpairSkew ThresholdPos TBit

DisplayPort

Summary of Results

Test Statistics	
Failed	0
Passed	16
Total	16

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	10	3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7	864 mV	37.4 %	VALUE <= 1.380 V
✓	0	10	3.3 Lane 1 - Peak to Peak Voltage Test - PRBS 7	886 mV	35.8 %	VALUE <= 1.380 V
✓	0	10	3.3 Lane 2 - Peak to Peak Voltage Test - PRBS 7	824 mV	40.3 %	VALUE <= 1.380 V
✓	0	10	3.3 Lane 3 - Peak to Peak Voltage Test - PRBS 7	872 mV	36.8 %	VALUE <= 1.380 V
✓	0	1	3.1 Lane 0 - Eye Diagram Test - PRBS 7	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 1 - Eye Diagram Test - PRBS 7	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 2 - Eye Diagram Test - PRBS 7	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 3 - Eye Diagram Test - PRBS 7	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	4	3.12 Lane 0 - Total Jitter Test (HBR) - PRBS 7	216.100 mUI	48.5 %	VALUE <= 420.000 mUI
✓	0	4	3.12 Lane 1 - Total Jitter Test (HBR) - PRBS 7	150.800 mUI	64.1 %	VALUE <= 420.000 mUI
✓	0	4	3.12 Lane 2 - Total Jitter Test (HBR) - PRBS 7	242.700 mUI	42.2 %	VALUE <= 420.000 mUI
✓	0	4	3.12 Lane 3 - Total Jitter Test (HBR) - PRBS 7	220.000 mUI	47.6 %	VALUE <= 420.000 mUI
✓	0	4	3.11 Lane 0 - Non ISI Jitter Test (HBR) - PRBS 7	136.800 mUI	50.4 %	VALUE <= 276.000 mUI
✓	0	4	3.11 Lane 1 - Non ISI Jitter Test (HBR) - PRBS 7	111.800 mUI	59.5 %	VALUE <= 276.000 mUI
✓	0	4	3.11 Lane 2 - Non ISI Jitter Test (HBR) - PRBS 7	154.900 mUI	43.9 %	VALUE <= 276.000 mUI
✓	0	4	3.11 Lane 3 - Non ISI Jitter Test (HBR) - PRBS 7	146.500 mUI	46.9 %	VALUE <= 276.000 mUI

11.TYPEC—DP

DisplayPort

Summary of Results

Test Statistics	
Failed	0
Passed	24
Total	24

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	3.1 Lane 0 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 1 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 2 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 3 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.12 Lane 0 - Total Jitter Test (TP3_EQ) (HBR2) - HBR2CPAT	171.300 mUI	70.5 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 1 - Total Jitter Test (TP3_EQ) (HBR2) - HBR2CPAT	179.300 mUI	69.1 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 2 - Total Jitter Test (TP3_EQ) (HBR2) - HBR2CPAT	179.500 mUI	69.1 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 3 - Total Jitter Test (TP3_EQ) (HBR2) - HBR2CPAT	189.300 mUI	67.4 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 0 - Total Jitter Test with No Cable Model (TP3_EQ) (HBR2) - HBR2CPAT	200.000 mUI	65.5 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 1 - Total Jitter Test with No Cable Model (TP3_EQ) (HBR2) - HBR2CPAT	198.000 mUI	65.9 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 2 - Total Jitter Test with No Cable Model (TP3_EQ) (HBR2) - HBR2CPAT	210.600 mUI	63.7 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 3 - Total Jitter Test with No Cable Model (TP3_EQ) (HBR2) - HBR2CPAT	205.800 mUI	64.5 %	VALUE <= 580.000 mUI
✓	0	1	3.12 Lane 0 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	79.000 mUI	83.9 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 1 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	86.800 mUI	82.3 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 2 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	89.200 mUI	81.8 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 3 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	98.500 mUI	79.9 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 0 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	104.400 mUI	78.7 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 1 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	104.100 mUI	78.8 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 2 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	113.700 mUI	76.8 %	VALUE <= 490.000 mUI
✓	0	1	3.12 Lane 3 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	114.300 mUI	76.7 %	VALUE <= 490.000 mUI

11.TYPEC—DP

DisplayPort

Summary of Results

Test Statistics	
Failed	0
Passed	12
Total	12

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	3.1 Lane 0 - Eye Diagram Test (TP3_CTLE) - TPS4	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 1 - Eye Diagram Test (TP3_CTLE) - TPS4	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 2 - Eye Diagram Test (TP3_CTLE) - TPS4	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 3 - Eye Diagram Test (TP3_CTLE) - TPS4	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.11 Lane 0 - Total Jitter Test (TP3_CTLE) - TPS4	281.200 mUI	44.4 %	VALUE <= 470.000 mUI
✓	0	1	3.11 Lane 1 - Total Jitter Test (TP3_CTLE) - TPS4	259.800 mUI	44.7 %	VALUE <= 470.000 mUI
✓	0	1	3.11 Lane 2 - Total Jitter Test (TP3_CTLE) - TPS4	275.100 mUI	41.5 %	VALUE <= 470.000 mUI
✓	0	1	3.11 Lane 3 - Total Jitter Test (TP3_CTLE) - TPS4	245.400 mUI	47.8 %	VALUE <= 470.000 mUI
✓	0	1	3.11 Lane 0 - Non ISI Jitter Test (TP3_CTLE) - TPS4	98.800 mUI	57.0 %	VALUE <= 230.000 mUI
✓	0	1	3.11 Lane 1 - Non ISI Jitter Test (TP3_CTLE) - TPS4	99.200 mUI	56.9 %	VALUE <= 230.000 mUI
✓	0	1	3.11 Lane 2 - Non ISI Jitter Test (TP3_CTLE) - TPS4	108.300 mUI	52.9 %	VALUE <= 230.000 mUI
✓	0	1	3.11 Lane 3 - Non ISI Jitter Test (TP3_CTLE) - TPS4	95.200 mUI	58.6 %	VALUE <= 230.000 mUI

12.eDP

RK3588 eDP 1.62G RBR

Summary of Results

Test Statistics	
Failed	0
Passed	3
Total	3

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	10	Lane 0 - Peak to Peak Differential Voltage Test (PRBS 7)	1.156 V	16.2 %	VALUE <= 1.380 V
✓	0	10	Lane 0 - Differential Voltage Level Test (PRBS 7)	377.518 mV	31.3 %	DiffVoltageLevelAbsoluteMinLimit V <= VALUE <= DiffVoltageLevelAbsoluteMaxLimit V
✓	0	10	Lane 0 - Pre-Emphasis Level Test (PRBS 7)	3.663 dB	38.4 %	PreEmphasisLevelAbsoluteMinLimit dB <= VALUE <= PreEmphasisLevelAbsoluteMaxLimit dB

RK3588 eDP 2.7G HBR

Summary of Results

Test Statistics	
Failed	0
Passed	3
Total	3

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	10	Lane 0 - Peak to Peak Differential Voltage Test (PRBS 7)	1.061 V	23.1 %	VALUE <= 1.380 V
✓	0	10	Lane 0 - Differential Voltage Level Test (PRBS 7)	703.833 mV	6.0 %	DiffVoltageLevelAbsoluteMinLimit V <= VALUE <= DiffVoltageLevelAbsoluteMaxLimit V
✓	0	10	Lane 0 - Pre-Emphasis Level Test (PRBS 7)	5.203 dB	16.8 %	PreEmphasisLevelAbsoluteMinLimit dB <= VALUE <= PreEmphasisLevelAbsoluteMaxLimit dB

12.eDP

RK3588 eDP 5.4G HBR2

Summary of Results

Test Statistics	
Failed	0
Passed	3
Total	3

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	10	Lane 0 - Peak to Peak Differential Voltage Test (PLTPAT)	1.117 V	19.1 %	VALUE <= 1.380 V
✓	0	10	Lane 0 - Differential Voltage Level Test (PLTPAT)	697.914 mV	3.4 %	DiffVoltageLevelAbsoluteMinLimit V <= VALUE <= DiffVoltageLevelAbsoluteMaxLimit V
✓	0	10	Lane 0 - Pre-Emphasis Level Test (PLTPAT)	5.170 dB	15.4 %	PreEmphasisLevelAbsoluteMinLimit dB <= VALUE <= PreEmphasisLevelAbsoluteMaxLimit dB

13.MIPI D/C PHY

MIPI D-PHY TX

Summary of Results

Test Statistics	
Failed	0
Passed	12
Total	12

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)	195.84 mV	45.8 %	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.3.8 HS Data TX Vcmtx Mismatch	710 ?V	85.8 %	VALUE < 5.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)	-225.50 mV	34.2 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD1 Pulse)	215.04 mV	42.3 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.3.5 HS Data TX Differential Voltage Mismatch (Pulse)	10.45 mV	25.4 %	VALUE < 14.00 mV
✓	0	1	1.3.6 HS Data TX Single Ended Output High Voltage(VOHHS Pulse)	309.07 mV	14.1 %	VALUE <= 360.00 mV
✓	0	1	1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx)	200.68 mV	49.3 %	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.4.8 HS Clock TX Vcmtx Mismatch	620 ?V	87.6 %	VALUE < 5.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse)	-224.39 mV	35.1 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)	218.33 mV	39.7 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)	6.06 mV	56.7 %	VALUE < 14.00 mV
✓	0	1	1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)	319.96 mV	11.1 %	VALUE <= 360.00 mV

13.MIPI D/C PHY

MIPI D-PHY RX

Summary of Results

Test Statistics	
Failed	0
Passed	27
Total	27

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)	221.94 mV	28.1 %	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.3.8 HS Data TX Vcmtx Mismatch	910 µV	81.8 %	VALUE < 5.00 mV
✓	0	1	1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))	5.31 mV	64.6 %	VALUE < 15.00 mV
✓	0	1	1.3.9 HS Data TX Common-Level Variations Between 50-450MHz (VCMTX(LF))	7.63 mV	69.5 %	VALUE < 25.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)	-211.99 mV	44.6 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD1 Pulse)	201.83 mV	47.6 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.3.5 HS Data TX Differential Voltage Mismatch (Pulse)	10.16 mV	27.4 %	VALUE < 14.00 mV
✓	0	1	1.3.6 HS Data TX Single Ended Output High Voltage(VOHHS Pulse)	327.51 mV	9.0 %	VALUE <= 360.00 mV
✓	0	1	1.4.9 HS Clock TX Common-Level Variations Between 50-450MHz (VCMTX(LF))	6.43 mV	74.3 %	VALUE < 25.00 mV
✓	0	1	1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx)	228.20 mV	21.8 %	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF))	6.65 mV	55.7 %	VALUE < 15.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse)	-222.25 mV	36.7 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)	222.92 mV	36.2 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)	670 µV	95.2 %	VALUE < 14.00 mV
✓	0	1	1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)	338.61 mV	5.9 %	VALUE <= 360.00 mV
✓	0	1	1.4.17 HS Clock Instantaneous (Ulinst)(Min)	371 ps	371.0 %	VALUE >= Ulinst_Min_Limit s
✓	0	1	1.3.1 HS Entry: DATA TLPX	57.59 ns	15.2 %	VALUE >= 50.00 ns
✓	0	1	1.3.2 HS Entry: DATA TX THS-PREPARE	52.43 ns	23.6 %	THSPrepare_LimitMin s <= VALUE <= THSPrepare_LimitMax s
✓	0	1	1.3.3 HS Entry: DATA TX THS-PREPARE+THS-ZERO	176.07 ns	18.2 %	VALUE >= TXTHSPrepareTHSZero_LimitMin s
✓	0	1	1.3.13 HS Exit: DATA TX THS-TRAIL	71.94 ns	16.8 %	VALUE >= TXTHSTrail_LimitMin s
✓	0	1	1.3.14 HS Exit: DATA TX TREOT	9.74 ns	72.2 %	VALUE <= 35.00 ns
✓	0	1	1.3.15 HS Exit: DATA TX TEOT	81.68 ns	25.6 %	VALUE <= TXTEOT_LimitMax s
✓	0	1	1.3.16 HS Exit: DATA TX THS-EXIT	4.99679 µs	490E+01 %	VALUE >= 100.00 ns
✓	0	1	1.5.3 HS Clock Rising Edge Alignment to First Payload Bit	Pass	100.0 %	VALUE <= 500.000000000 m
✓	0	1	1.4.17 HS Clock Instantaneous (Ulinst)(Max)	431 ps	96.6 %	VALUE < 12.500 ns
✓	0	1	1.5.4 Data-to-Clock Skew (TSKEW(TX))(Max,Min)	-102 mUlinst	24.5 %	MinMaxTSkewTest_LimitMin Ulinst <= VALUE <= MinMaxTSkewTest_LimitMax Ulinst
✓	0	1	1.5.4 Data-to-Clock Skew (TSKEW(TX))(Mean)	-4 mUlinst	49.0 %	MeanTSkewTest_LimitMin Ulinst <= VALUE <= MeanTSkewTest_LimitMax Ulinst

14.MIPI DPHY

MIPI D-PHY RX

Summary of Results

Test Statistics	
Failed	1
Passed	51
Total	52

Pass	# Failed	# Trials	Test Name	Actual Value	Pass Limits
✓	0	1	1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)	223.56 mV	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.3.8 HS Data TX Vcmtx Mismatch	300 mV	VALUE < 5.00 mV
✓	0	1	1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))	6.65 mV	VALUE < 15.00 mV
✓	0	1	1.3.9 HS Data TX Common-Level Variations Between 50-450MHz (VCMTX(LF))	6.90 mV	VALUE < 25.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)	-221.37 mV	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD1 Pulse)	193.08 mV	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.3.6 HS Data TX Single Ended Output High Voltage(VOHHS Pulse)	331.17 mV	VALUE <= 360.00 mV
✓	0	1	1.4.17 HS Clock Instantaneous (Ulinst)(Max)	438 ps	VALUE < 12.500 ns
✓	0	1	1.3.3 HS Entry: DATA TX THS-PREPARE+THS-ZERO	175.60 ns	VALUE >= TXTHSPrepareTHSZero_LimitMin s
✗	1	1	1.3.11 HS Data TX 20%-80% Rise Time (tR)(Burst Data)	188 ps	VALUE < DataRiseTime_LimitMax s
✓	0	1	1.3.11 HS Data TX 20%-80% Rise Time (tR)(Burst Data)(Min Conformance Limit)(Informative)	188 ps	VALUE > DataRiseTime_LimitMin s
✓	0	1	1.3.12 HS Data TX 80%-20% Fall Time (tF)(Burst Data)	118 ps	VALUE < DataFallTime_LimitMax s
✓	0	1	1.3.12 HS Data TX 80%-20% Fall Time (tF)(Burst Data)(Min Conformance Limit)(Informative)	118 ps	VALUE > DataFallTime_LimitMin s
✓	0	1	1.4.9 HS Clock TX Common-Level Variations Between 50-450MHz (VCMTX(LF))	6.21 mV	VALUE < 25.00 mV
✓	0	1	1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx)	224.59 mV	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.4.8 HS Clock TX Vcmtx Mismatch	1.55 mV	VALUE < 5.00 mV
✓	0	1	1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF))	7.14 mV	VALUE < 15.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse)	-192.02 mV	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)	186.99 mV	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)	5.03 mV	VALUE < 14.00 mV
✓	0	1	1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)	323.96 mV	VALUE <= 360.00 mV
✓	0	1	1.4.3 HS Entry: CLK TX TCLK-PREPARE+TCLK-ZERO	377.39 ns	VALUE >= 300.00 ns
✓	0	1	1.4.11 HS Clock TX 20%-80% Rise Time (tR)(Burst Clock)	155 ps	VALUE < CLKRiseTime_LimitMax s
✓	0	1	1.4.11 HS Clock TX 20%-80% Rise Time (tR)(Burst Clock)(Min Conformance Limit)(Informative)	155 ps	VALUE > CLKRiseTime_LimitMin s
✓	0	1	1.4.12 HS Clock TX 80%-20% Fall Time (tF)(Burst Clock)	153 ps	VALUE < CLKFallTime_LimitMax s
✓	0	1	1.4.12 HS Clock TX 80%-20% Fall Time (tF)(Burst Clock)(Min Conformance Limit)(Informative)	153 ps	VALUE > CLKFallTime_LimitMin s
✓	0	1	1.4.17 HS Clock Instantaneous (Ulinst)(Min)	361 ps	VALUE >= Ulinst_Min_Limit s
✓	0	1	1.3.1 HS Entry: DATA TLPX	57.46 ns	VALUE >= 50.00 ns
✓	0	1	1.3.2 HS Entry: DATA TX THS-PREPARE	51.59 ns	THSPrepare_LimitMin s <= VALUE <= THSPrepare_LimitMax s
✓	0	1	1.3.13 HS Exit: DATA TX THS-TRAIL	74.99 ns	VALUE >= TXTHSTrail_LimitMin s
✓	0	1	1.3.14 HS Exit: DATA TX TREOT	7.33 ns	VALUE <= 35.00 ns
✓	0	1	1.3.15 HS Exit: DATA TX TEOT	82.32 ns	VALUE <= TXTEOT_LimitMax s

15.USB3.0

USB3.0 HOST

Summary of Results

Test Statistics	
Failed	0
Passed	23
Total	23

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	LFPS Peak-Peak Differential Output Voltage	1.0821 V	29.5 %	800.0 mV <= VALUE <= 1.2000 V
✓	0	1	LFPS Period (tPeriod)	41.6479 ns	27.1 %	20.0000 ns <= VALUE <= 100.0000 ns
✓	0	1	LFPS Burst Width (tBurst)	1.0500 µs	43.8 %	600.0 ns <= VALUE <= 1.4000 µs
✓	0	1	LFPS Repeat Time Interval (tRepeat)	10.0418 µs	49.5 %	6.0000 µs <= VALUE <= 14.0000 µs
✓	0	1	LFPS Rise Time	256.1 ps	93.6 %	VALUE <= 4.0000 ns
✓	0	1	LFPS Fall Time	259.2 ps	93.5 %	VALUE <= 4.0000 ns
✓	0	1	LFPS Duty cycle	51.0477 %	44.8 %	40.0000 % <= VALUE <= 60.0000 %
✓	0	1	LFPS AC Common Mode Voltage	33.0 mV	67.0 %	VALUE <= 100.0 mV
✓	0	1	5G TSSC-Freq-Dev-Min	-4.828473 kppm	29.5 %	-5.300000 kppm <= VALUE <= -3.700000 kppm
✓	0	1	5G TSSC-Freq-Dev-Max	225.193 ppm	12.5 %	TSSCMin ppm <= VALUE <= TSSCMax ppm
✓	0	1	5G SSC Modulation Rate	31.113316 kHz	37.1 %	30.000000 kHz <= VALUE <= 33.000000 kHz
✓	0	1	5G SSC Slew Rate	4.838 ms	51.6 %	VALUE <= 10.000 ms
✓	0	1	5G SSC df/dt	346.0 ppm/us	72.3 %	VALUE <= 1.2500 kppm/us
ⓘ	0	1	5G Short Channel Random Jitter	709 fs	100.0 %	Information Only
✓	0	1	5G Short Channel Maximum Deterministic Jitter	27.461 ps	68.1 %	VALUE <= 86.000 ps
✓	0	1	5G Short Channel Total Jitter at BER-12	37.432 ps	71.6 %	VALUE <= 132.000 ps
✓	0	1	5G Short Channel Template Test	0.000	100.0 %	VALUE = 0.000
✓	0	1	5G Short Channel Differential Output Voltage	445.9 mV	31.4 %	100.0 mV <= VALUE <= 1.2000 V
ⓘ	0	1	5G Random Jitter (CTLE ON)	654 fs	100.0 %	Information Only
✓	0	1	5G Far End Maximum Deterministic Jitter (CTLE ON)	46.918 ps	45.4 %	VALUE <= 86.000 ps
✓	0	1	5G Far End Total Jitter at BER-12 (CTLE ON)	56.118 ps	57.5 %	VALUE <= 132.000 ps
✓	0	1	5G Far End Template Test (CTLE ON)	0.000	100.0 %	VALUE = 0.000
✓	0	1	5G Far End Differential Output Voltage (CTLE ON)	230.6 mV	11.9 %	100.0 mV <= VALUE <= 1.2000 V

16.USB2.0

USB2.0 DEVICE

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	EL_38 EL_39 Device Suspend Timing Response	3.064 ms	48.8 %	3.000 ms <= VALUE <= 3.125 ms
✓	0	1	EL_40 Device Resume Timing Response	Pass	100.0 %	Pass/Fail
✓	0	1	EL_27 Device CHIRP Response to Reset from Hi-Speed Operation	3.563 ms	16.0 %	3.100 ms <= VALUE <= 6.000 ms
✓	0	1	EL_28 Device CHIRP Response to Reset from Suspend	20.322 µs	0.3 %	2.500 µs <= VALUE <= 6.000000 ms

USB2.0 HOST

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	EL_33 CHIRP Timing Response	5.307 µs	5.3 %	1 ns <= VALUE <= 100.000 µs
✓	0	1	EL_34 CHIRP K Width	50.064 µs	49.7 %	40.000 µs <= VALUE <= 60.000 µs
✓	0	1	EL_34 CHIRP J Width	50.070 µs	49.7 %	40.000 µs <= VALUE <= 60.000 µs
✓	0	1	EL_35 SOF Timing Response	304.230 µs	48.9 %	100.000 µs <= VALUE <= 500.000 µs

17.RGMII

Signal Name	Description	Test item	Unit	Spec limited			Measure			Test Result	Waveform	Remark
				Min	Tpical	Max	Min	Mean	Max	Null		
RGMII_MDC	MDC Cycle Time	tMCC	ns	80.00			495.8			Pass	tMCC	参考图一中t3，在PHY端测试
	MDC High Time	tMCH		32.00			247.9			Pass	tMCH	参考图一中t2，在PHY端测试
	MDC Low Time	tMCL		32.00			247.9			Pass	tMCL	参考图一中t1，在PHY端测试
	MDC Input High Voltage	Vih_MDC	V	1.20			1.8		1.85	Pass	Vih_MDC	
	MDC Input Low Voltage	Vil_MDC				0.50	-0.023		-0.004	Pass	Vil_MDC	
RGMII_MDIO	MDIO Setup Time	tMSU	ns	10.00			254.4			Pass	tMSU	参考图一中t4，高低电平参考图二，在PHY端测试
	MDIO Hold Time	tMHT		10.00			246.3			Pass	tMHT	参考图一中t5，高低电平参考图二，在PHY端测试
	MDIO Clock Rise to MDIO Valid	tMRV				300.00			43	Pass	tMRV	参考图一中t6，高低电平参考图二，在PHY端测试
	MDIO Input High Voltage	Vih_MDIO	V	1.20			1.77		1.88	Pass	Vih_MDIO	
	MDIO Input Low Voltage	Vil_MDIO				0.50	0.024		0.042	Pass	Vil_MDIO	
MDIO_CPU	CPU MDIO Input Setup Time	CPU_tMSU	ns	-		-	208.4			Null	CPU_tMSU	
	CPU MDIO Input Hold time	CPU_tMHT					278.1			Null	CPU_tMHT	
	CPU MDIO Input High Voltage	CPU_Vih_MDIO	V				1.78		1.82	Null	CPU_Vih_MDIO	
	CPU MDIO Input Low Voltage	CPU_Vil_MDIO					0.063		0.081	Null	CPU_Vil_MDIO	
RGMII_CLK	CLK period	tGCC_CLK	ns	7.20		8.80				Null	tGCC_CLK	此模式没有RGMII_CLK
	CLK frequency deviation	FD_CLK	ppm	-		-				Pass	FD_CLK	
	CLK Duty Cycle	tDuty_CLK	%	-		-				Pass	tDuty_CLK	
	CLK Rise Time	tR_CLK	ns			-				Pass	tR_CLK	20%~80%
	CLK Fall Time	tF_CLK				-				Pass	tF_CLK	20%~80%
RGMII_TXC	TXC clock period	tGCC_TXC	ns	7.2	8.0	8.8	7.94	8	8.07	Pass	tGCC_TXC	
	TXC Duty Cycle	tDuty_TXC	%	45	50	55	49.5	49.9	50.5	Pass	tDuty_TXC	
	TXC Rise Time	tR_TXC	ns			0.75			0.65	Pass	tR_TXC	20%~80%
	TXC Fall Time	tF_TXC				0.75			0.485	Pass	tF_TXC	20%~80%
RGMII_RXC	RXC clock period	tGCC_RXC	ns	7.2	8.0	8.8	7.7	8	8.2	Pass	tGCC_RXC	
	RXC Duty Cycle	tDuty_RXC	%	45	50	55	47.2	49.3	50.9	Pass	tDuty_RXC	
	RXC Rise Time	tR_RXC	ns			0.75			1.26	Fail	tR_RXC	20%~80%
	RXC Fall Time	tF_RXC				0.75			1.41	Fail	tF_RXC	20%~80%
RGMII_TXD&TXC	TXD Input High Voltage	Vih_TXD	V	1.20			1.7		1.88	Pass	Vih_TXD	
	TXD Input Low Voltage	Vil_TXD					-0.039		0.043	Pass	Vil_TXD	
	TXD to Clock Input Setup	tSETUP	ns	1.2	2.0		1.65	-	-	Pass	tSETUP	高低电平参考图二
	TXD to Clock Input Hold	tHOLD		1.2	2.0		1.7	-	-	Pass	tHOLD	高低电平参考图二
RGMII_RXD&RXC	RXD CPU Iput High Voltage	CPU Vih_RXD	V				1.75	-	1.85	Null	CPU_Vih_RXD	
	RXD CPU Iput Low Voltage	CPU Vil_RXD					-0.092	-	0.082	Null	CPU_Vil_RXD	
	RXD to Clock Input Setup	CPU tSETUP	ns				1.4	-	-	Null	CPU_tSETUP	PHY端延迟开启
	RXD to Clock Input Hold	CPU tHOLD					1.62	-	-	Null	CPU_tHOLD	

NOTE: tR_RXC/tF_RXC为RGMII PHY（RTL8211）过来的信号，与RK3588无关，可不关注。

SD Spec SI Test Reports

SD Signal Integrity and Timing Analysis													
4 Data Lane Speed Mode	Drive strength (mA)	Power supply (V)	NOTE: The test points need to be at the far end of the signal output.										
SDR104		1.7-1.95											
Signal Name	Trace length mils	Description	Test item	Unit	Spec limited			Measure			Test Result	Waveform	Remark
					Min	Tpical	Max	MIN	Mean	MAX	Pass		
SD_CLK		Frequence	fPP	MHz	0		208	-	148.5	-	Do not care	SD-fPP	
		Clock Cycle	tCLK	ns	4.8		-	6.64	6.83	-	Pass	SD-tCLK	
		Clock Duty	tDUTY	%	30		70	47.8	-	50.5	Pass	SD-tDUTY	
		Time of Low Level to High Level	tCR	ns	-		1.366	-	-	0.553	Pass	SD-tCR	
		Time of High Level to Low Level	tCF		-		1.366	-	-	0.538	Pass	SD-tCF	
SD_CMD		Setup Time of Input	tISU	ns	1.4		-	2.93	-	-	Pass	SD-CMD-tISU	
		Hold Time of Input	tIH		0.8		-	3.05	-	-	Pass	SD-CMD-tIH	
		Card Output Phase	tOP		0		13.66	-	-	4.05	Pass	SD-CMD-tOP	
		Output valid data window	tODW		4.098		-	6.08	-	-	Pass	SD-CMD-tODW	
SD_Data		Setup Time of Input	tISU	ns	1.4		-	2.65	-	-	Pass	SD-Data-tISU	
		Hold Time of Input	tIH		0.8		-	3.08	-	-	Pass	SD-Data-tIH	
		Card Output Phase	tOP		0		13.66	-	-	4.16	Pass	SD-Data-tOP	
		Output valid data window	tODW		4.098		-	5.97	-	-	Pass	SD-Data-tODW	

Push-pull mode bus signal level For 1.7V-1.95V VDDIO range										
1.7-1.95						Measure		Test Result	Waveform	Remark
Parameter	Symbol	Min	Max	Unit	Conditions	MIN	MAX	Null		
IO Power Supply Voltage	VDD	1.7	1.95	V				Null	-	
CPU Input High Voltage of CMD	CPU-VIH-CMD	指标根据	CPU规格书填写	V		1.856	1.993	Null	CPU-VIH-CMD	
CPU lutput Low Voltage of CMD	CPU-VIL-CMD	指标根据	CPU规格书填写	V		-0.047	0.05	Null	CPU-VIL-CMD	
CPU lutput High Voltage of Data	CPU-VIH-Data	指标根据	CPU规格书填写	V		1.89	1.95	Null	CPU-VIH-Data	
CPU lutput Low Voltage of Data	CPU-VIL-Data	指标根据	CPU规格书填写	V		-0.277	0.03	Null	CPU-VIL-Data	
Device InputHigh Voltage of CLK	VIH-CLK	1.27	2	V		1.75	1.79	Pass	SD_VIH_CLK	
Device InputLow Voltage of CLK	VIL-CLK	-0.3	0.58	V		-0.077	-0.019	Pass	SD_VIL_CLK	
Device InputHigh Voltage of CMD	VIH-CMD	1.27	2	V		1.7	1.8	Pass	SD_VIH_CMD	
Device InputLow Voltage of CMD	VIL-CMD	-0.3	0.58	V		-0.057	0.023	Pass	SD_VIL_CMD	
Device InputHigh Voltage of Data	VIH-Data	1.27	2	V		1.77	1.82	Pass	SD_VIH_DATA	
Device InputLow Voltage of Data	VIL-Data	-0.3	0.58	V		-0.012	0.043	Pass	SD_VIL_DATA	
		-	-	V				Do not care	-	

19.SPDIF

SPDIF Test Report

SPDIF Signal Integrity and Timing Analysis

Drive strength (ohm)	Power supply (V)	NOTE： The test points need to be at the far end of the signal output.
40	1.8	

Signal Name	Description	Test item	Unit	25M Spec limited			Measure		Test Result	Waveform	Remark
				Min	Typical	Max	Min	Max	Pass		
SPDIF_TX	Frequence	Freq	MHz				3.058	3.072	Pass	SPDIF-Freq	
	Rise Time	tRISE	ns	0.1		25	1.550	2.200	Pass	SPDIF-tRISE	
	Fall Time	tFALL	ns	0.1		25	0.900	2.260	Pass	SPDIF-tFALL	
	Jitter	Tjitter	ns	-		15	-	0.510	Pass	SPDIF-Jitter	
	Signal Voltage	VIH	V				1.810	1.880	Pass	SPDIF-VIH	

Uart2 M0 3.3V SI Test Report

Baud rate	Power supply (V)	NOTE： The test points need to be at the far end of the signal output.
3000000	3.3	

Normal model

Signal Name	Description	Test item	Unit	Spec limited			Measure		Test Result	Waveform	Remark
				Min	Tpical	Max	Min	Max			
TX	Baud rate	TX-BR	Mb/s	2.82		3.18	2.998	3.001	Pass	TX-BR	
	Pulse duration	TX-Tw	ns	331.3333		335.33333	333.15	333.60	Pass	TX-Tw	
	Input HIGH voltage	VIH	V	2		3.6	3.21	3.22	Pass	TX-VIH	
	Input LOW voltage	VIL	V	-0.3		0.8	0.040	0.060	Pass	TX-VIL	
RX	Baud rate	RX-BR	Mb/s	2.82		3.18	2.992	3.01	Pass	RX-BR	板载FT232R测试
	Pulse duration	RX-Tw	ns	320		350	326.45	328.60	Pass	RX-Tw	
	Input HIGH voltage	VIH	V	2		3.6	3.22	3.24	Pass	RX-VIH	
	Input LOW voltage	VIL	V	-0.3		0.8	0.040	0.060	Pass	RX-VIL	

21.I2S

I²S0 SI Test Report

Channels (Ch)	Sampling Digit (bits)	Sample Rate (kHz)	Power supply (V)	NOTE: 1.The test points need to be at the far end of the signal output.
8	16	48	1.8	

Signal Name	Test item	Description	Unit	Spec limited			Measure			Test Result	Waveform	Remark
				Min	Typical	Max	Min	Mean	Max	Pass		
MCLK	fMCLK	Frequency	MHz	6.144	12.288	24.576	12.28	12.29	12.3	Pass	fMCLK	
	dMCLK	MCLK Duty Cycle	%	45.00		55.00	49.91	49.976	50.03	Pass	dMCLK	
	VIH-MCLK	High-level Input Voltage	V	1.26		2.10	1.732	1.738	1.75	Pass	VIH-MCLK	
	VIL-MCLK	Low-level Input Voltage		-0.30		0.54	0.051	0.059	0.06	Pass	VIL-MCLK	
LRCLK	fLRCLK	Frequency	kHz	46.56	48	49.44	47.998	47.999	48.001	Pass	fLRCLK	
	tLRCLKH	High Time(us)	us	9.79		11.04	10.416	10.417	10.417	Pass	tLRCLKH	
	tLRCLKL	Low Time(us)		9.79		11.04	10.417	10.417	10.418	Pass	tLRCLKL	
	VIH-LRCLK	High-level Input Voltage	V	1.26		2.10	1.783	1.793	1.793	Pass	VIH-LRCLK	
	VIL-LRCLK	Low-level Input Voltage		-0.30		0.54	0.012	0.012	0.012	Pass	VIL-LRCLK	
SCLK	fBCLK	Frequency	MHz	2.92	3.072	3.23	3.0698	3.072	3.0736	Pass	fBCLK	
	dBCLK	BCLK Duty Cycle	%	45.00		55.00	49.98	49.994	50.02	Pass	dBCLK	
	t_{hsclk}	sclk pulse width high	ns	113.93		211.59	162.65	162.75	162.85	Pass	thsclk	
	t_{lsclk}	sclk pulse width low		113.93		211.59	162.70	162.78	162.90	Pass	tlsclk	
	VIH-BCLK	High-level Input Voltage	V	1.26		2.10	1.741	1.7528	1.759	Pass	VIH-BCLK	
	VIL-BCLK	Low-level Input Voltage		-0.30		0.54	0.033	0.042	0.042	Pass	VIL-BCLK	
SDO	VIH-SDO	High-level Input Voltage	V	1.26		2.10	1.809	1.818	1.818	Pass	VIH-SDO	
	VIL-SDO	Low-level Input Voltage		-0.30		0.54	-0.009	0.000	0.000	Pass	VIL-SDO	
SDI	VOH-SDI	CPU High-level Input Voltage	V	1.26		2.10	1.760	1.769	1.769	Pass	VOH-SDI	
	VOL-SDI	CPU Low-level Input Voltage		-0.30		0.54	-0.002	0.002	0.007	Pass	VOL-SDI	
Timing	$t_{od\_sclk2lrck}$	$i2s_x$_lrck_rx/$i2s_x$_lrck_tx delay time from i2sx_sclk falling edge	ns	-162.76		97.66	1.5		1.92	Pass	tod_sclk2lrck	指标根据CPU规格书填写
	t_{susdi}	$i2s_x$_sdi setup time to $i2s_x$_sclk rising edge	ns	65.10		-	94			Pass	tsusdi	
	t_{hsdi}	$i2s_x$_sdi hold time from $i2s_x$_sclk rising edge	ns	81.38		-	187.5			Pass	thsdi	
	$t_{od\_sclk2sdo}$	$i2s_x$_sdo propagation delay from $i2s_x$_sclk falling edge	ns	-81.38		97.66	1.93		3.95	Pass	tod_sclk2sdo	

21.I2S

Jitter	Tj-MCLK	MCLK Total Jitter	ns	-		3.00			0.17	Pass	Tj-MCLK	
	Tj-BCLK	MCLK Total Jitter	ns	-		3.00			0.41	Pass	Tj-BCLK	

22.PDM

PDM 1.8V

PDM_1.8V SI Test Report

PDM Signal Integrity and Timing Analysis

Power supply（V）
1.7-1.95

NOTE：The test points need to be at the far end of the signal output.

Signal Name	Description	Test item	Unit	Limited		Measure			Test Result	Waveform
				Min	Max	Min	Mean	Max	Pass	
CLK	Frequency of PDM_CLK	fCLK	MHz	1.024	6.144	3.0703	3.072	3.0731	Pass	fCLK
	Duty cycle of PDM_CLK	Tduty	%	45	55	49.95	49.978	50.00	Pass	Tduty
	CLK Rise Time	tR_CLK	ns		20	-	-	2.50	Pass	tR_CLK
	CLK Fall Time	tF_CLK			20	-	-	2.55	Pass	tF_CLK
SDI	Input SDI hold time to PDM_CLK rising edge	thdp	ns	0		39.6	-	-	Pass	thdp
	Input SDI setup time to PDM_CLK rising edge	tsup		16.1		96	-	-	Pass	tsup
	Input SDI hold time to PDM_CLK falling edge	thdn	ns	0		38.8	-	-	Pass	thdn
	Input SDI setup time to PDM_CLK falling edge	tsun		16.1		94.4	-	-	Pass	tsun
Voltage	CLK low level input voltage	VIL_CLK	V		0.54	0	-	0.01	Pass	VIL_CLK
	CLK high level input voltage	VIH_CLK		1.26		1.76	-	1.77	Pass	VIH_CLK
	SDI low level input voltage at rising edge	VIL_SDI			0.54	0.03	-	0.04	Pass	VIL_SDI
	SDI high level input voltage at rising edge	VIH_SDI		1.26		1.67	-	1.68	Pass	VIH_SDI

PDM 3.3V

PDM1_3.3V SI Test Report

PDM Signal Integrity and Timing Analysis

Power supply（V）
2.7-3.6

NOTE：The test points need to be at the far end of the signal output.

Signal Name	Description	Test item	Unit	Limited		Measure			Test Result	Waveform
				Min	Max	Min	Mean	Max	Pass	
CLK	Frequency of PDM_CLK	fCLK	MHz	1.024	6.144	3.0703	3.072	3.0736	Pass	fCLK
	Duty cycle of PDM_CLK	Tduty	%	45	55	49.95	49.982	50.02	Pass	Tduty
	CLK Rise Time	tR_CLK	ns		20	-	-	2.55	Pass	tR_CLK
	CLK Fall Time	tF_CLK			20	-	-	2.45	Pass	tF_CLK
SDI	Input SDI hold time to PDM_CLK rising edge	thdp	ns	0		18.66	-	-	Pass	thdp
	Input SDI setup time to PDM_CLK rising edge	tsup		16.1		131.6	-	-	Pass	tsup
	Input SDI hold time to PDM_CLK falling edge	thdn	ns	0		18.4	-	-	Pass	thdn
	Input SDI setup time to PDM_CLK falling edge	tsun		16.1		130.6	-	-	Pass	tsun
Voltage	CLK low level input voltage	VIL_CLK	V		0.8	0	-	0.02	Pass	VIL_CLK
	CLK high level input voltage	VIH_CLK		2		3.22	-	3.24	Pass	VIH_CLK
	SDI low level input voltage at rising edge	VIL_SDI			0.8	0.02	-	0.04	Pass	VIL_SDI
	SDI high level input voltage at rising edge	VIH_SDI		2		3.12	-	3.14	Pass	VIH_SDI

23.I2C

I2C Test Report

Operation Mode	Pullup (KΩ)	Power supply (V)	NOTE： Please fill out the power supply first. The test points need to be at the far end of the signal output. Each test item relatived to time must be measured at least three times.
Standard Mode	2.2	1.8	

Signal Name	Description	Test item	Unit	Spec limited			Measure			Test Result	Waveform	Remark
				Min	Tpical	Max	Min	Mean	Max	Pass		
I2C_SCL	Frequency	fCLK	KHz	0		100	98.8	98.8	98.8	Pass	fCLK	
	Rise Time of SCL	tR_SCL	ns			1000	-		97	Pass	tR_SCL	This is dictated by external components
	Fall Time of SCL	tF_SCL				300	-		4.75	Pass	tF_SCL	
	High Time	tHIGH	us	4		-	4.96		-	Pass	tHIGH	
	Low Time	tLOW		4.7		-	5.05		-	Pass	tLOW	
I2C_SDA	Rise Time of SDA	tR_SDA	ns			1000	-		107	Pass	tR_SDA	
	Fall Time of SDA	tF_SDA				300	-		4.95	Pass	tF_SDA	
I2C_SCL&I2C_SDA	data valid time	tVD_DAT	us	-		3.45	-		2.075	Pass	tVD_DAT	
	data valid acknowledge time	tVD_ACK		-		3.45	-		0.176	Pass	tVD_ACK	
	Bus Free Time between STOP and START	tBUF		4.7		-	36.3		-	Pass	tBUF	
	START Hold Time	tHD_STA		4		-	15		-	Pass	tHD_STA	
	START Setup Time	tSU_STA		4.7		-	9.88		-	Pass	tSU_STA	
	STOP Setup Time	tSU_STO		4		-	4.97		-	Pass	tSU_STO	
	SDA Hold Time	tHD_DAT		0		3.45	1.87		1.955	Pass	tHD_DAT	Slave and Master Default
	SDA Setup Time	tSU_DAT	ns	250		-	2970		-	Pass	tSU_DAT	
Signal level	LOW level input voltage of SCL	VIL_SCL	V	-0.5		0.54	0.04		0.049	Pass	VIL-SCL	
	HIGH level input voltage of SCL	VIH_SCL		1.26		2.3	1.76		1.774	Pass	VIH-SCL	
	LOW level input voltage of SDA	VIL_SDA		-0.5		0.54	0.05		0.058	Pass	VIL-SDA	
	HIGH level input voltageof SDA	VIH_SDA		1.26		2.3	1.77		1.783	Pass	VIH-SDA	