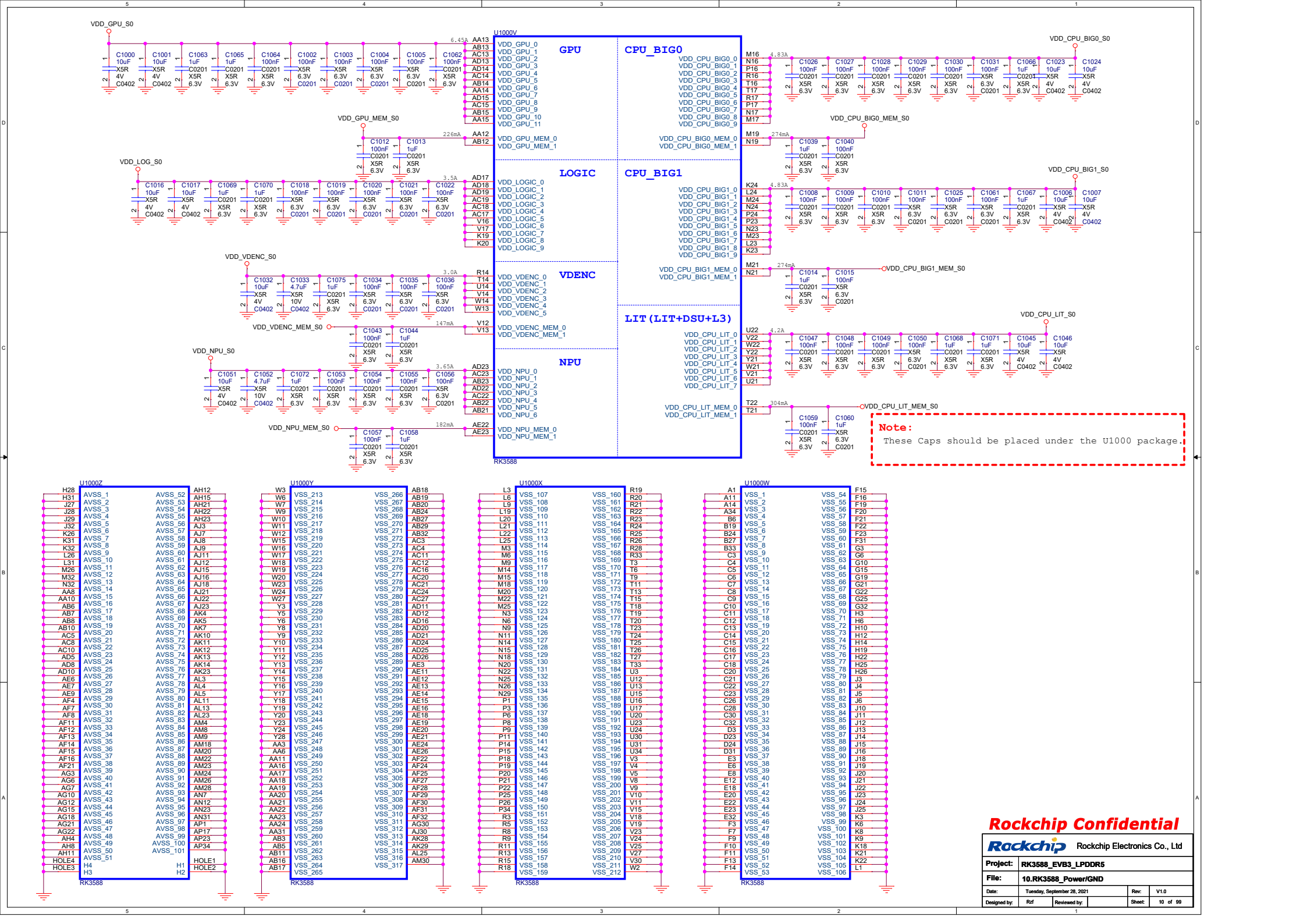
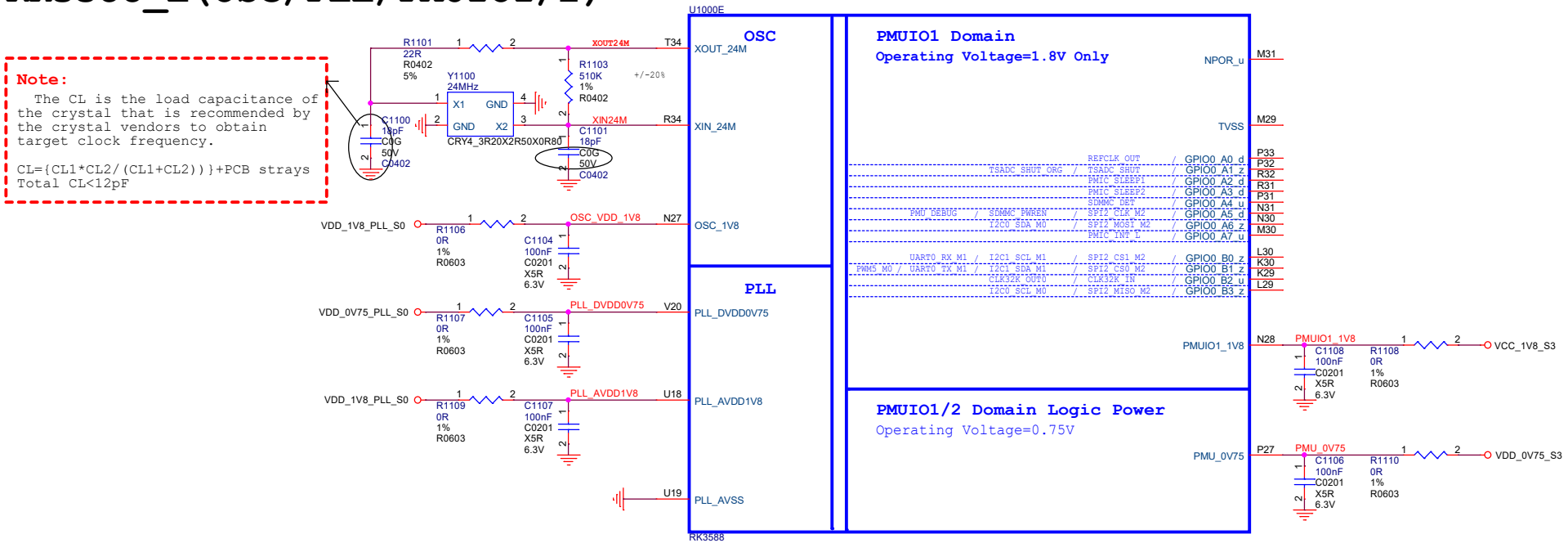


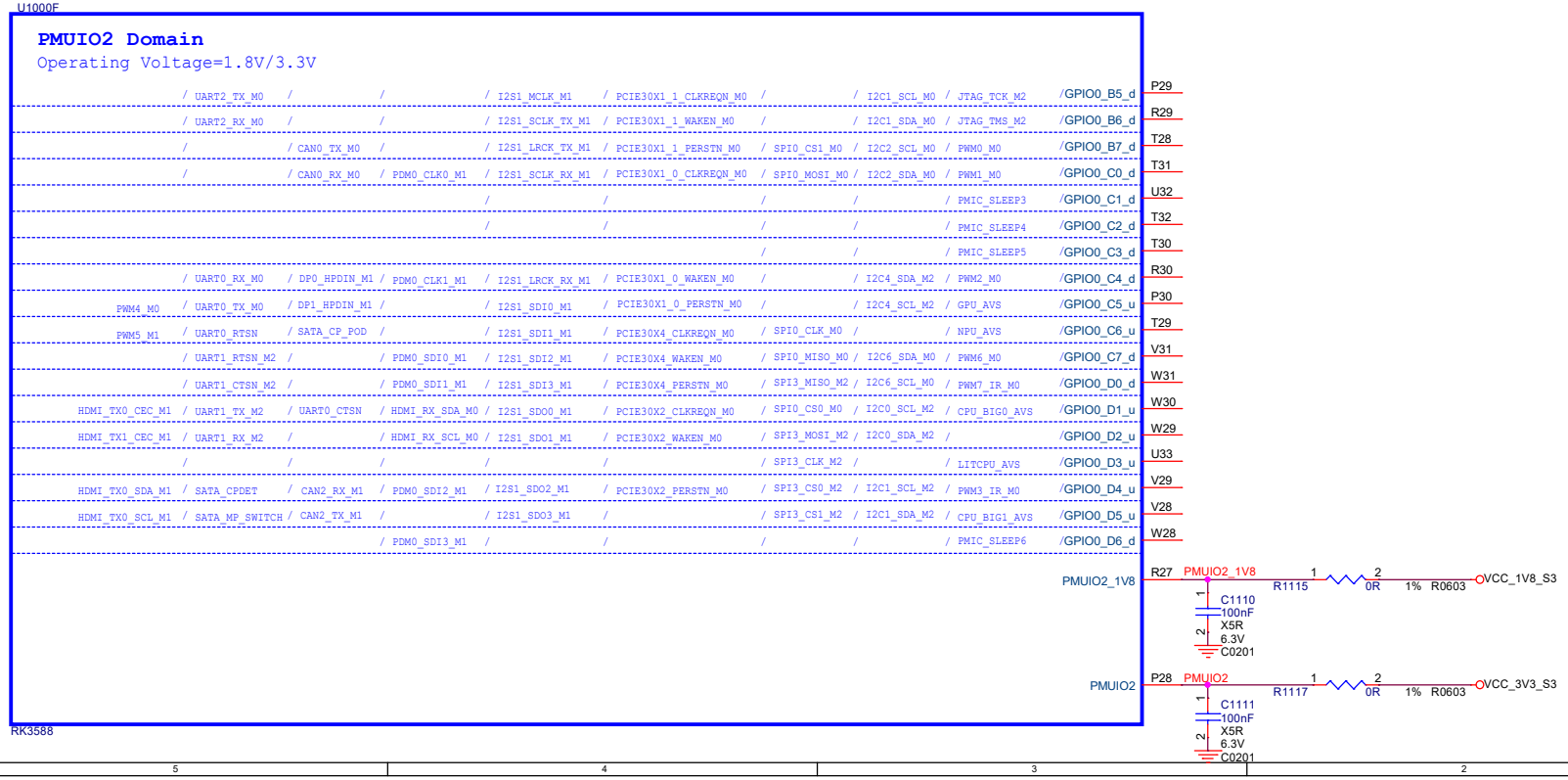
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_EVB3_LPDDR5		
File:	10.RK3588_Power/GND		
Date:	Tuesday, September 28, 2021	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Sheet: 10 of 99

RK3588_E(OSC/PLL/PMUIO1/2)



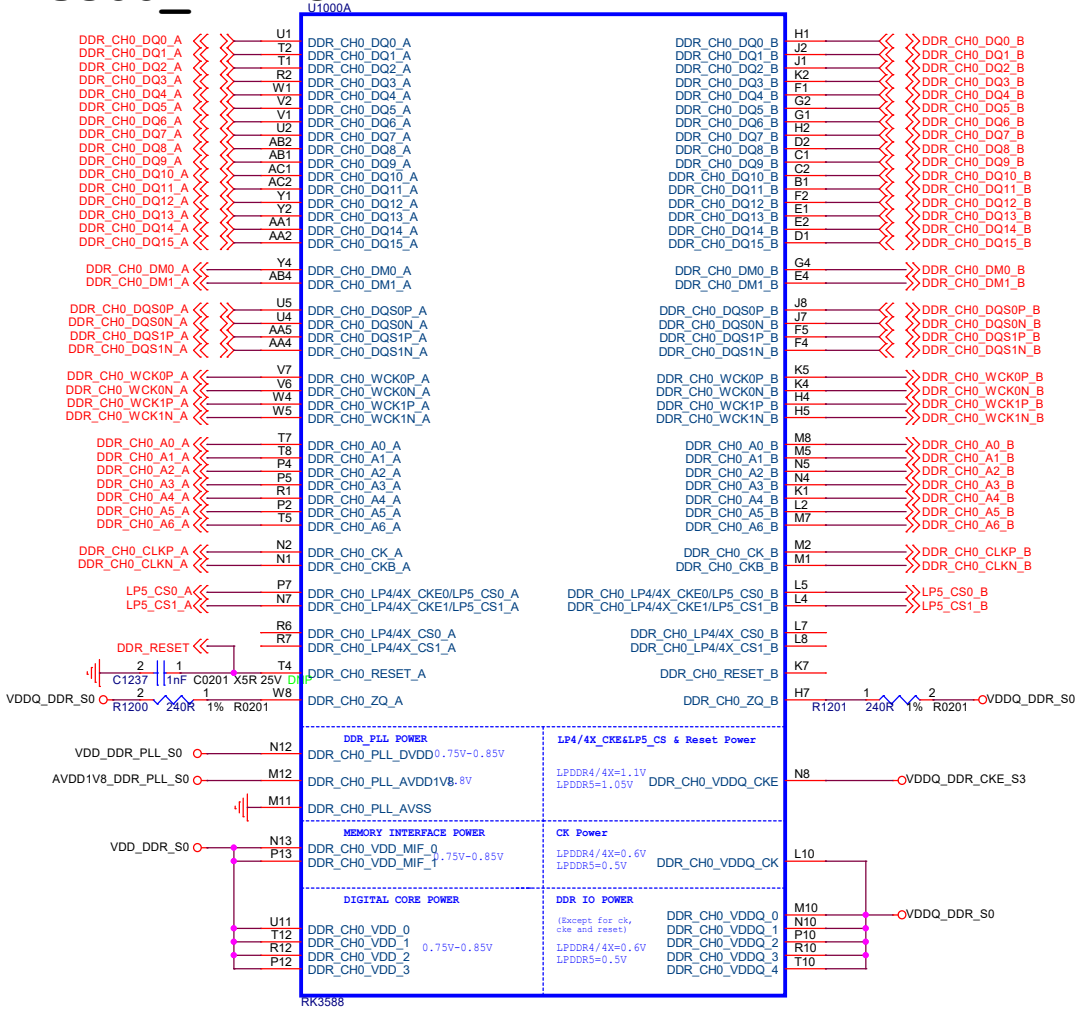
RK3588_F(PMUIO2)

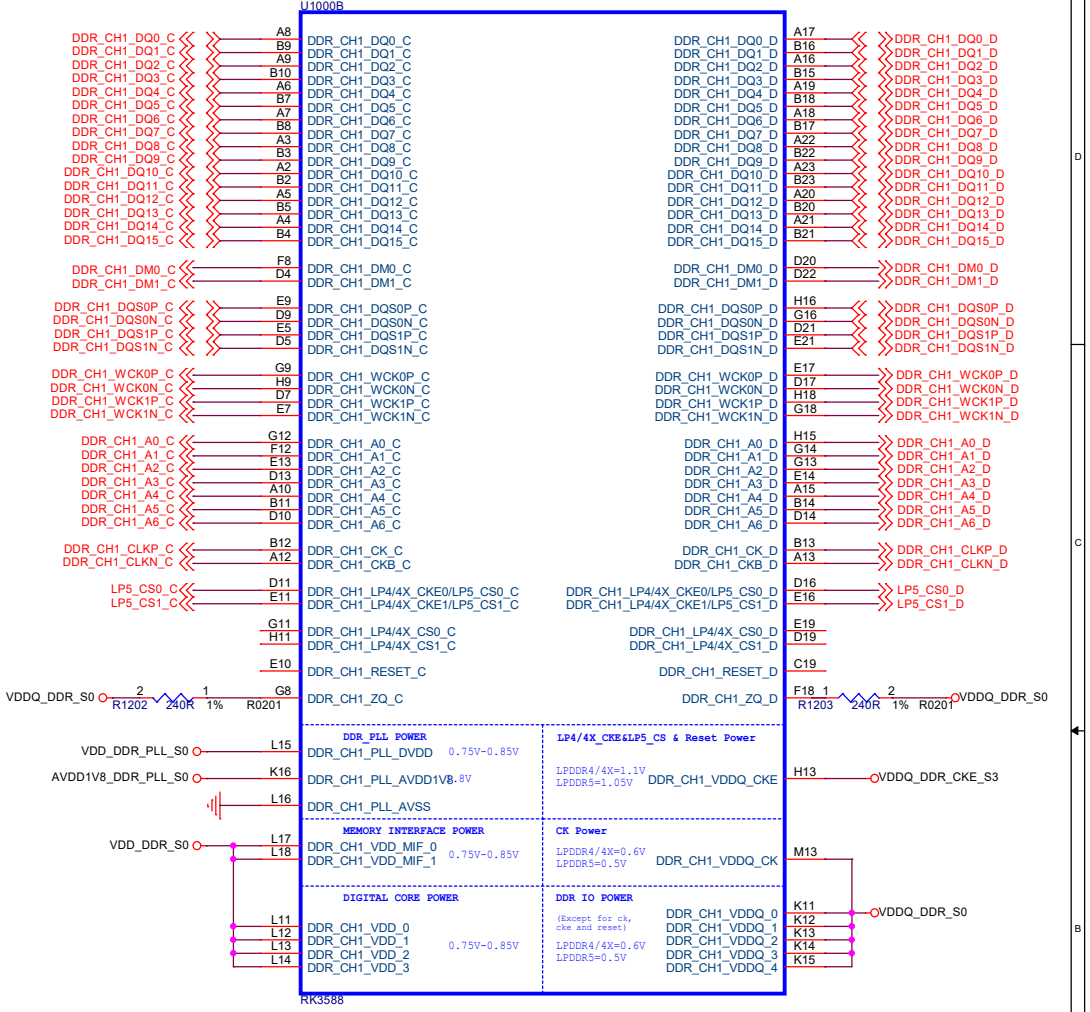


Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_EVB3_LPDDR5				
File:	11.RK3588_OSC/PLL/PMUIO				
Date:	Tuesday, March 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	11 of 99

RK3588_DDR CTRL





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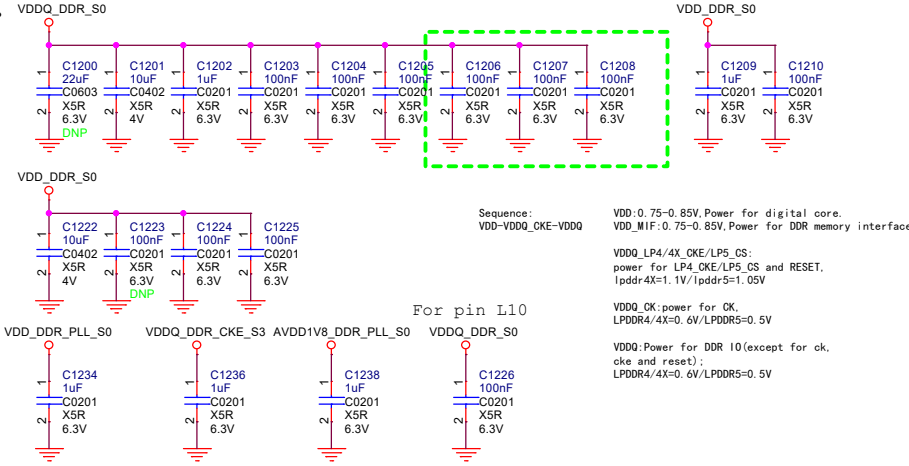
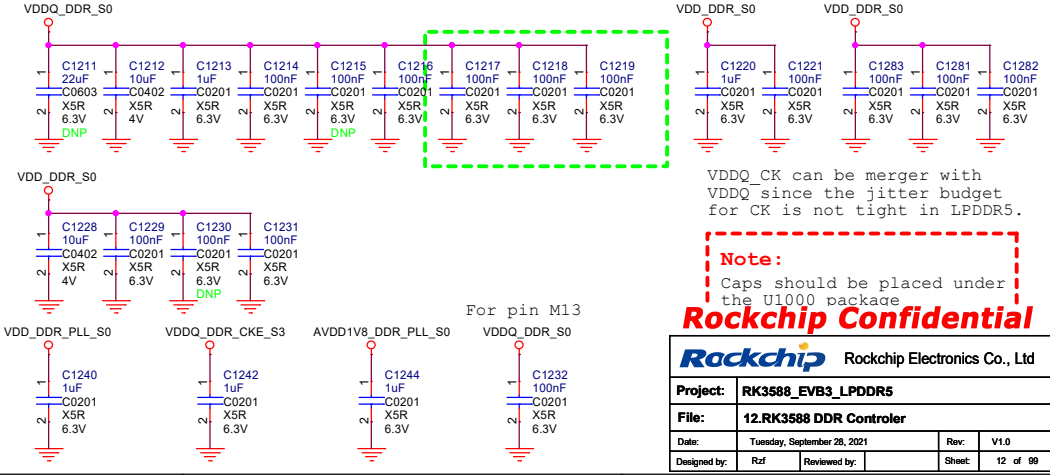


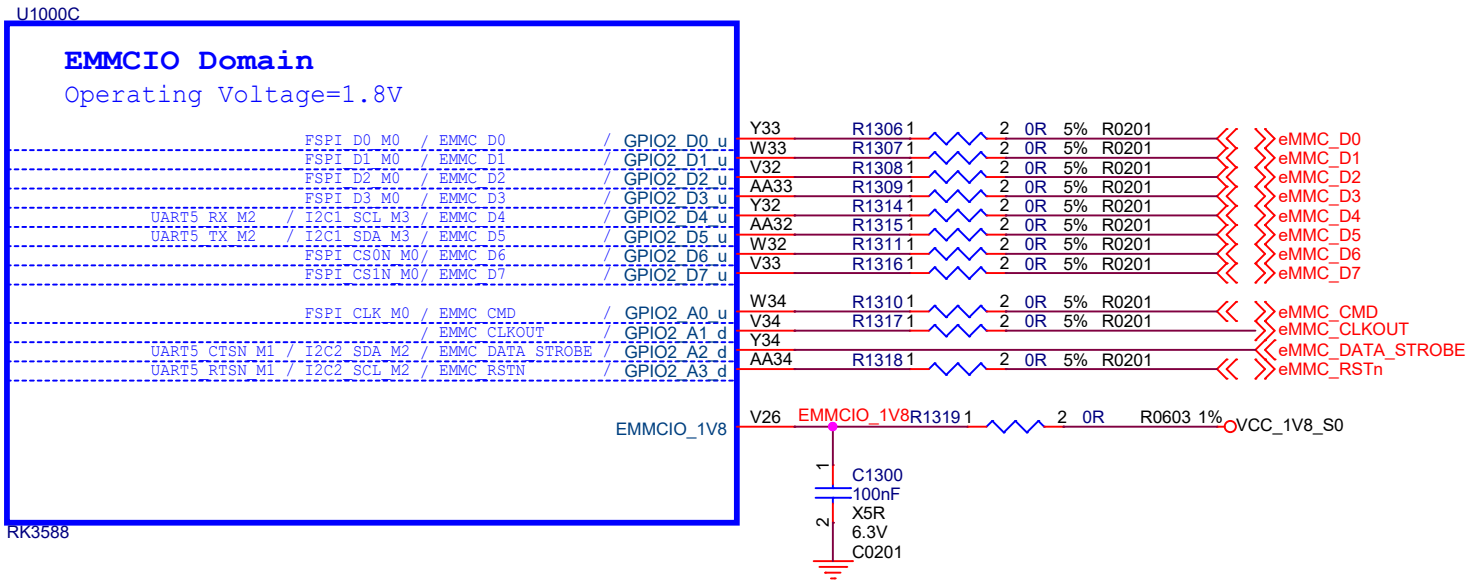


VDDQ_CK can be merger with VDDQ since the jitter budget for CK is not tight in LPDDR5.

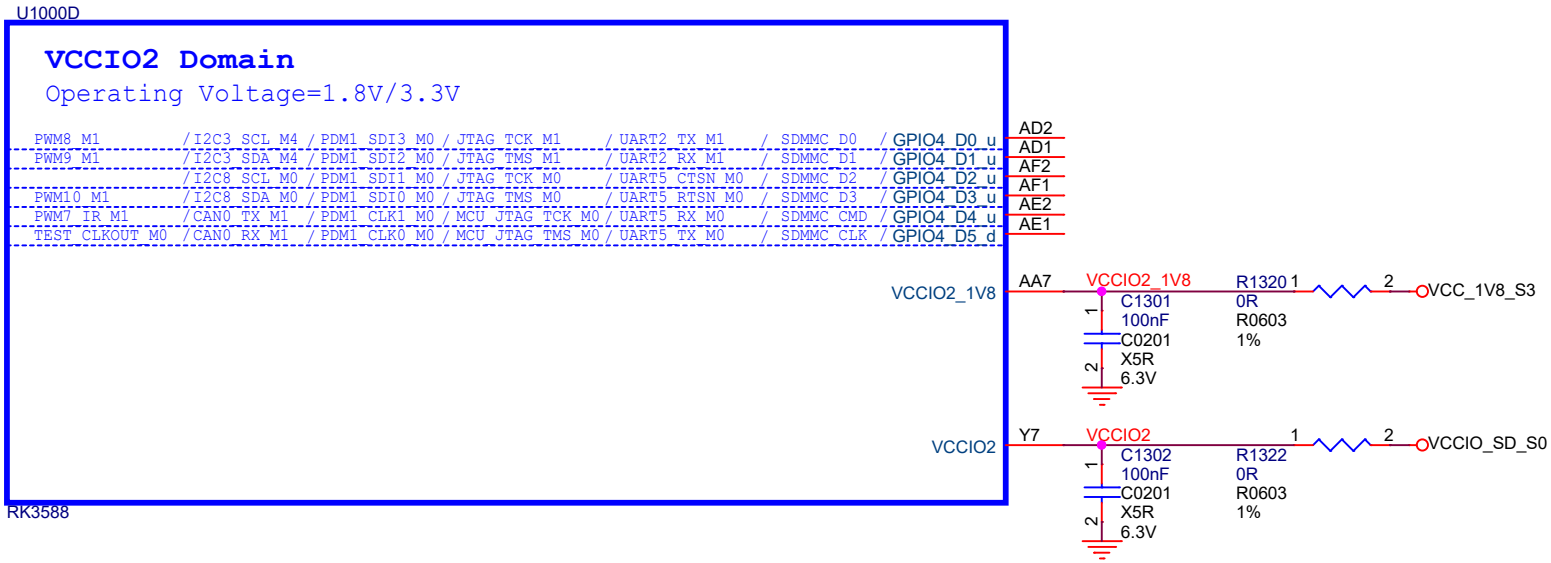
Note:
Caps should be placed under the U1000 package

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_EVB3_LPDDR5		
File:	12.RK3588 DDR Controler		
Date:	Tuesday, September 28, 2021	Rev:	V1.0
Designed by: Rzf	Reviewed by:	Sheet:	12 of 99

RK3588_C(EMMCIO Domain)



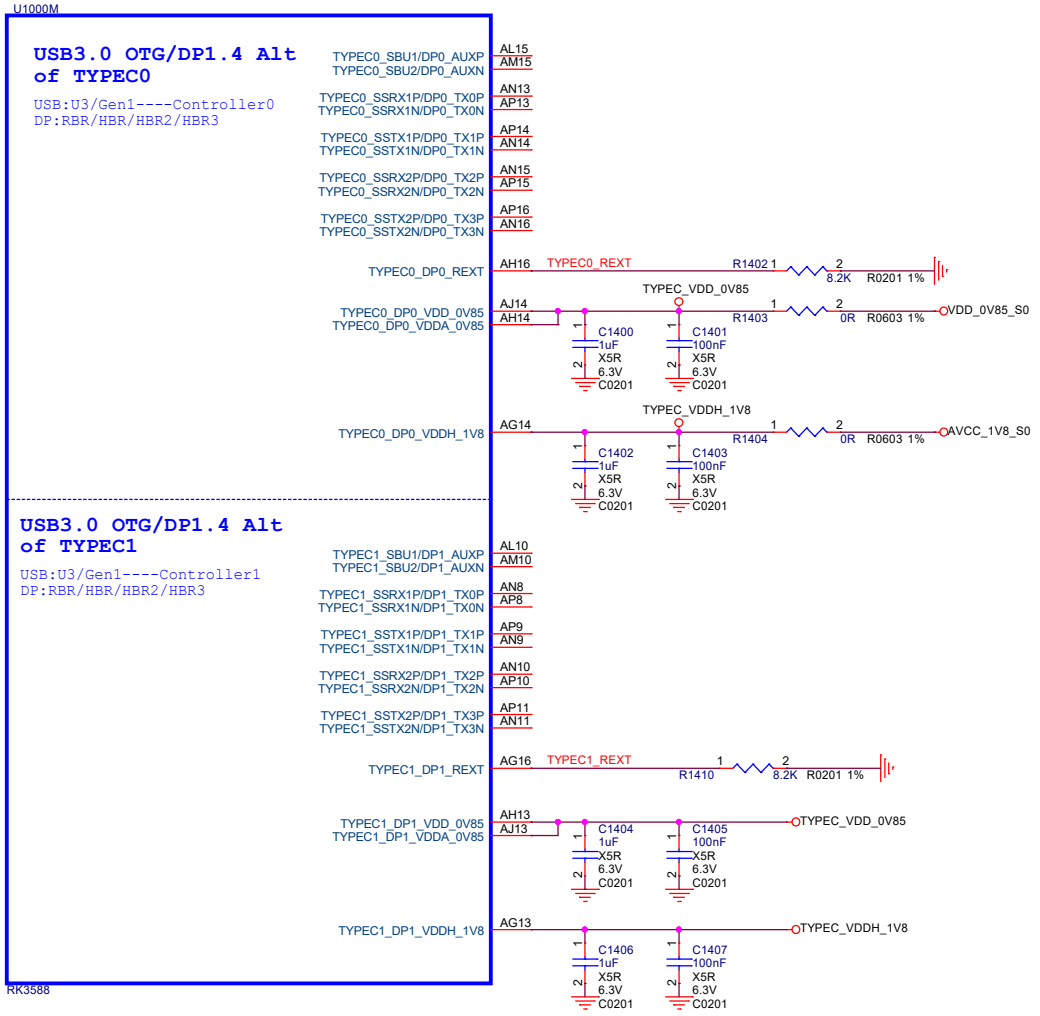
RK3588_D(VCCIO2 Domain)



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_EVB3_LPDDR5				
File:	13.RK3588_Flash/SD Controller				
Date:	Tuesday, March 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	13 of 99

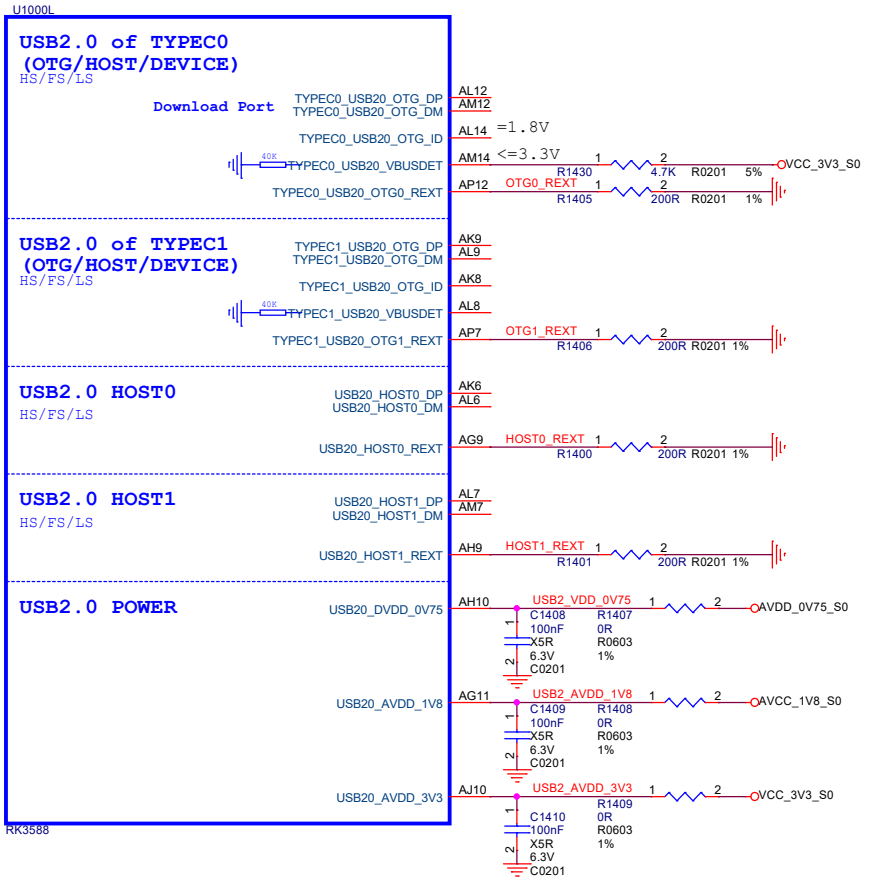
RK3588_M(TYPEC/DP)



USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*USB30_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)

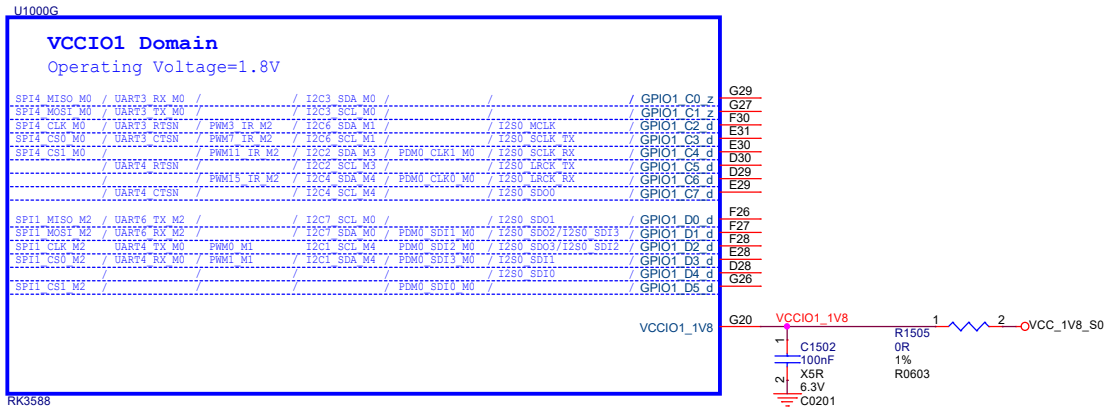


Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

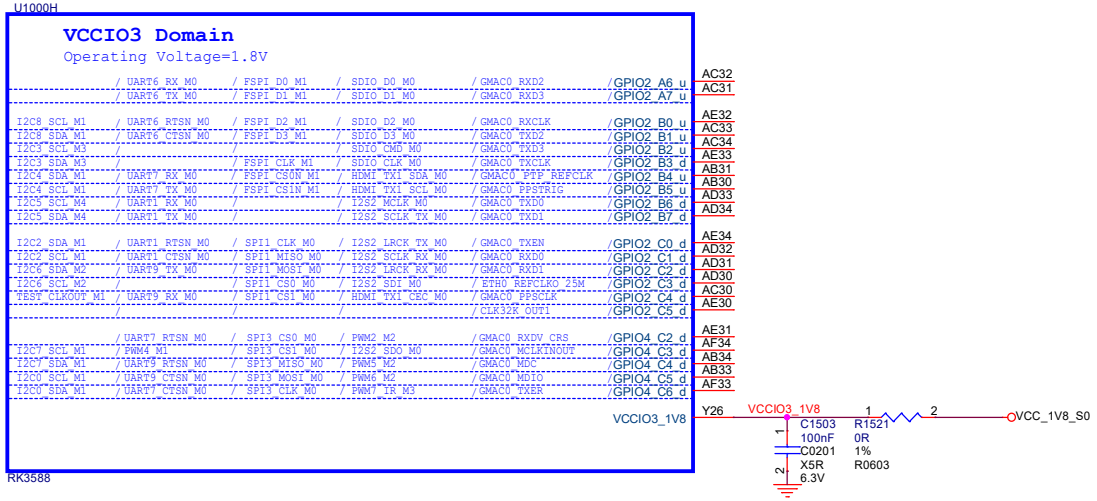
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_EVB3_LPDDR5				
File:	14.RK3588_USB30/USB20_Ctrl				
Date:	Tuesday, March 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	14 of 99

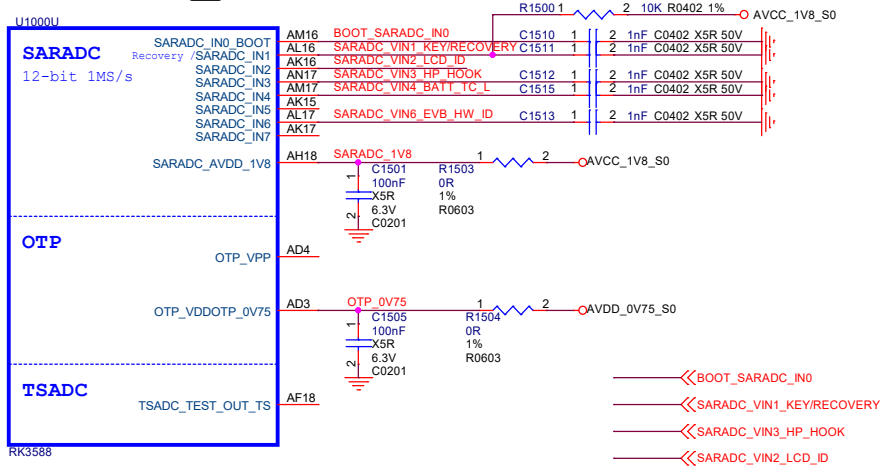
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

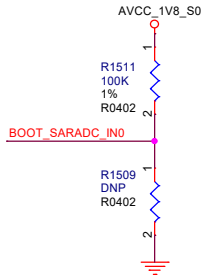


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	360K	180K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	180K	360K	2730	1.2V	FSPI M1-USB
LEVEL6	20K	100K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

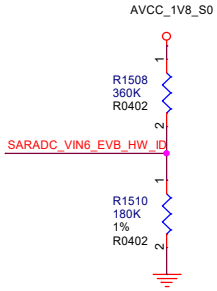
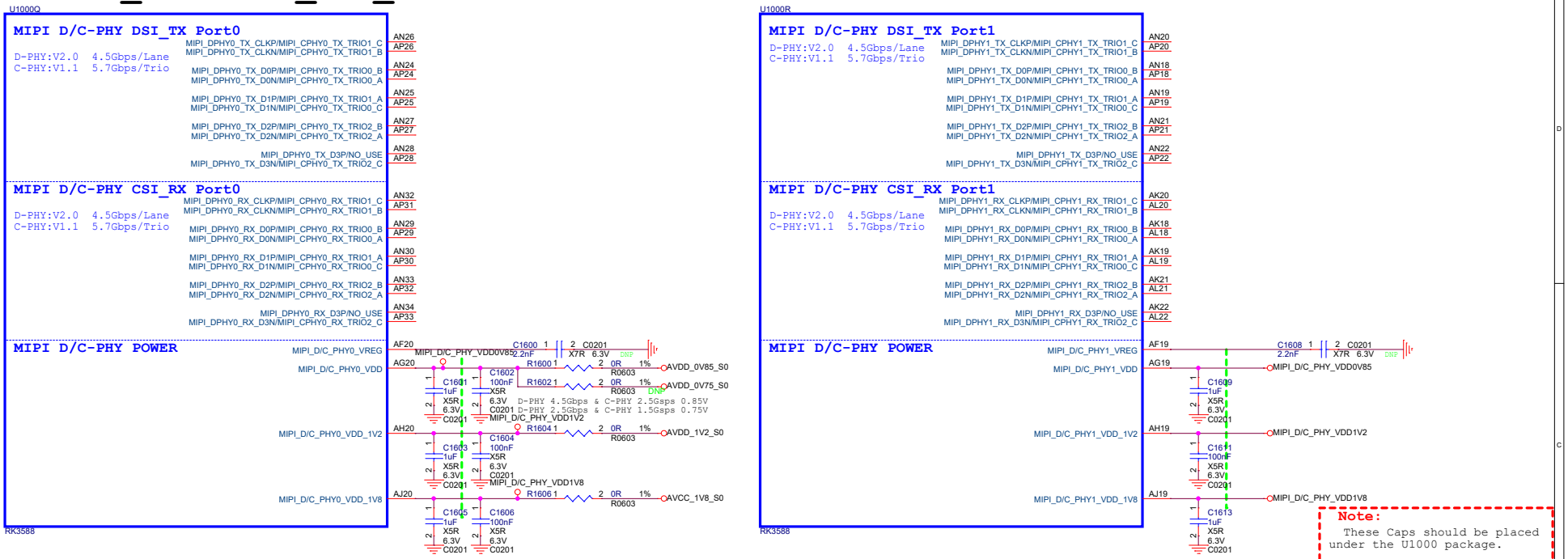


TABLE 2

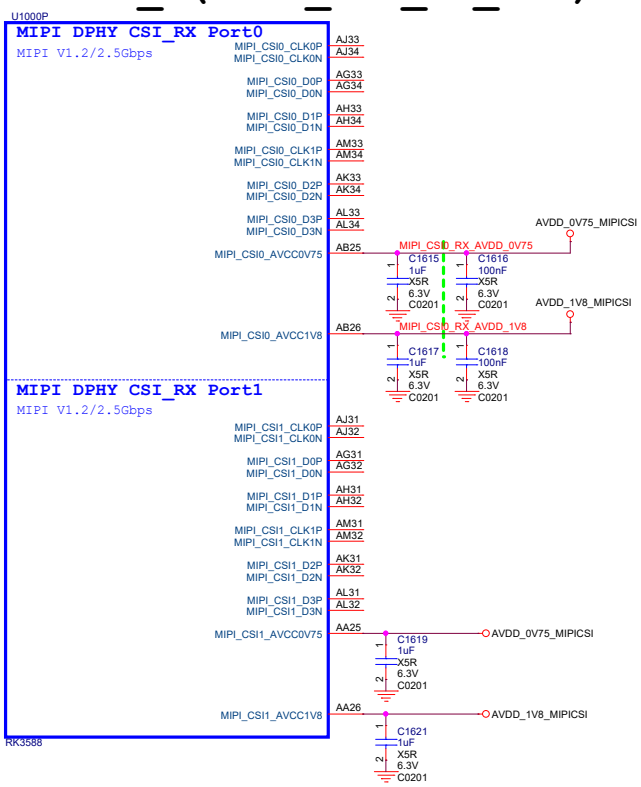
Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	360K	180K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	180K	360K	2730	1.2V	V5.0
LEVEL6	20K	100K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_EVB3_LPDDR5		
File:	15.RK3588_SARADC/1.8V Only GPIO		
Date:	Tuesday, March 15, 2022	Rev:	V1.0
Designed by: Rzf	Reviewed by:	Sheet:	15 of 99

RK3588_Q/R(MIPI_D/C_PHY0/1)



RK3588_P(MIPI_CSI_RX_PHY)



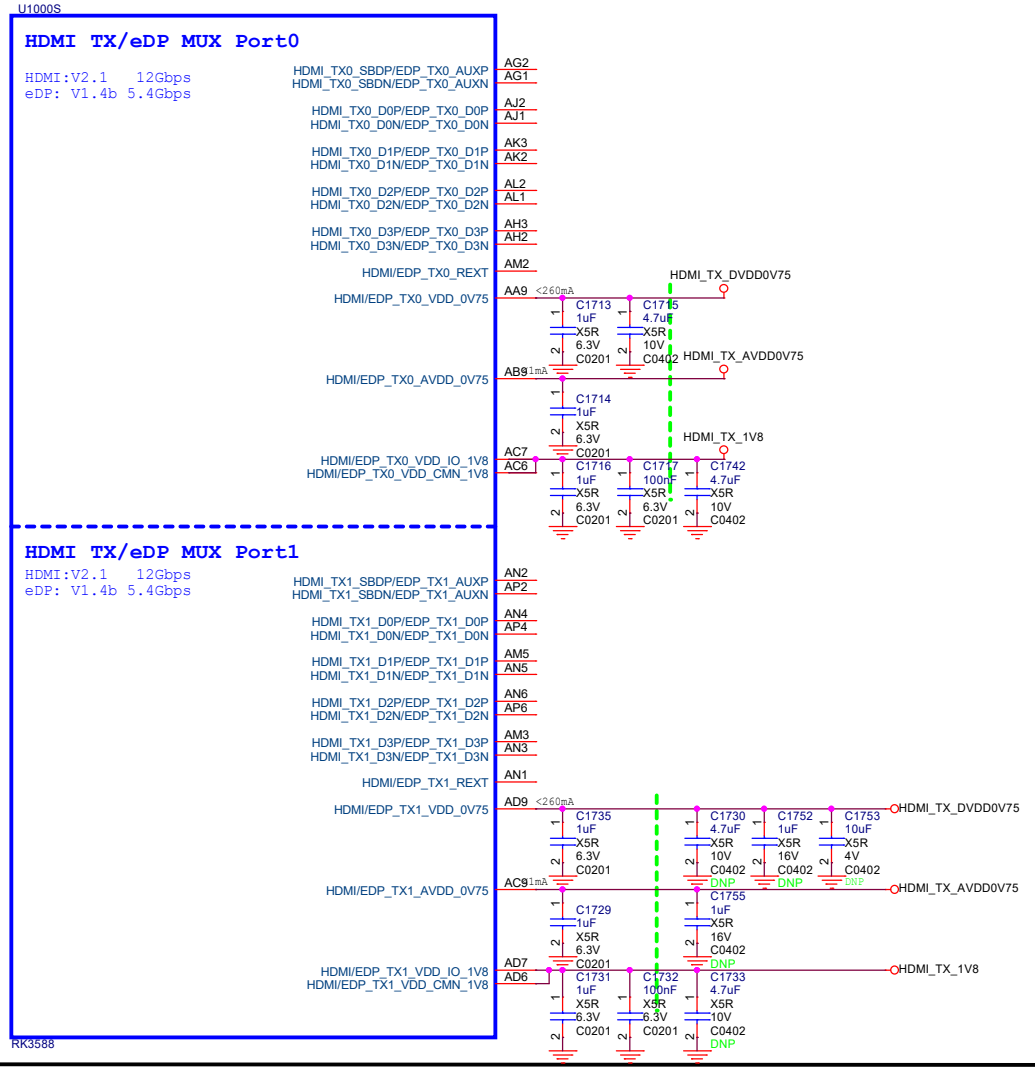
MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

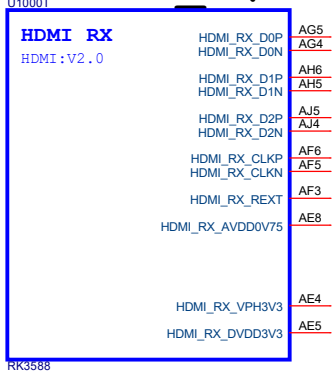
Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Rockchip Electronics Co., Ltd					
Project:	RK3588_EVB3_LPDDR5				
File:	16.RK3588_MIPI Interface				
Date:	Thursday, March 17, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	16 of 99



RK3588_T(HDMI20 RX)



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Rockchip Electronics Co., Ltd					
Project:	RK3588_EVB3_LPDDR5				
File:	17.RK3588_HDMI Interface				
Date:	Tuesday, March 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	17 of 99

RK3588_N(PCIE20)

CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

PCIE20_0_REFCLKP L32
PCIE20_0_REFCLKN L33
PCIE20_0_TXP/SATA30_0_TXP M34
PCIE20_0_TXN/SATA30_0_TXN M33
PCIE20_0_RXP/SATA30_0_RXP N33
PCIE20_0_RXN/SATA30_0_RXN N34
PCIE20_SATA30_0_AVDD_0V85 M28
C1810 100nF X5R 6.3V C0201
PCIE20_SATA30_0_AVDD_1V8 M27
C1808 100nF X5R 6.3V C0201

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

PCIE20_1_REFCLKP H32
PCIE20_1_REFCLKN H33
PCIE20_1_TXP/SATA30_1_TXP K33
PCIE20_1_TXN/SATA30_1_TXN K34
PCIE20_1_RXP/SATA30_1_RXP J33
PCIE20_1_RXN/SATA30_1_RXN J34
PCIE20_SATA30_1_AVDD_0V85 L28
C1818 100nF X5R 6.3V C0201
PCIE20_SATA30_1_AVDD_1V8 L27
C1816 100nF X5R 6.3V C0201

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 OTG Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 OTG
Controller2

MUX

PCIE20_2_REFCLKP G31
PCIE20_2_REFCLKN G30
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP H30
PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN H29
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP J31
PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN J30
PCIE20_SATA30_USB30_2_AVDD_0V85 K28
C1806 100nF X5R 6.3V C0201
C1807 4.7uF X5R 10V C0402
AVDD_0V85_PCIE20
PCIE20_SATA30_USB30_2_AVDD_1V8 K27
C1804 1uF X5R 6.3V C0201
C1805 4.7uF X5R 10V C0402
AVCC_1V8_PCIE20

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588

Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

RK3588_O(PCIE30)

U1000O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIE20/SATA30 MUX1

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE20/SATA30/USB30 MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0 DM(EP&RC)

PCIE30_PORT0_REF_CLKP E33
PCIE30_PORT0_REF_CLKN E34
Lane0
PCIE30_PORT0_TX0P D32
PCIE30_PORT0_TX0N D33
PCIE30_PORT0_RX0P G33
PCIE30_PORT0_RX0N G34
Lane1
PCIE30_PORT0_TX1P C33
PCIE30_PORT0_TX1N C34
PCIE30_PORT0_RX1P F32
PCIE30_PORT0_RX1N F33
PCIE30_PORT0_RESREF B34
PCIE30_PORT0_AVDD0V75 G24
PCIE30_PORT0_AVDD1V8 G23

PCIE30 PORT1 (RC)

PCIE30_PORT1_REF_CLKP A28
PCIE30_PORT1_REF_CLKN B28
Lane2
PCIE30_PORT1_TX0P B30
PCIE30_PORT1_TX0N A30
PCIE30_PORT1_RX0P B32
PCIE30_PORT1_RX0N A32
Lane3
PCIE30_PORT1_TX1P C29
PCIE30_PORT1_TX1N B29
PCIE30_PORT1_RX1P C31
PCIE30_PORT1_RX1N B31
PCIE30_PORT1_RESREF A33
PCIE30_PORT1_AVDD0V75 H24
C1814 1uF X5R 6.3V C0201
C1815 4.7uF X5R C0402 10V
PCIE30_PORT_AVDD0V75
PCIE30_PORT1_AVDD1V8 H23
C1812 100nF X5R 6.3V C0201
C1813 4.7uF X5R 10V C0402
PCIE30_PORT_AVDD1V8

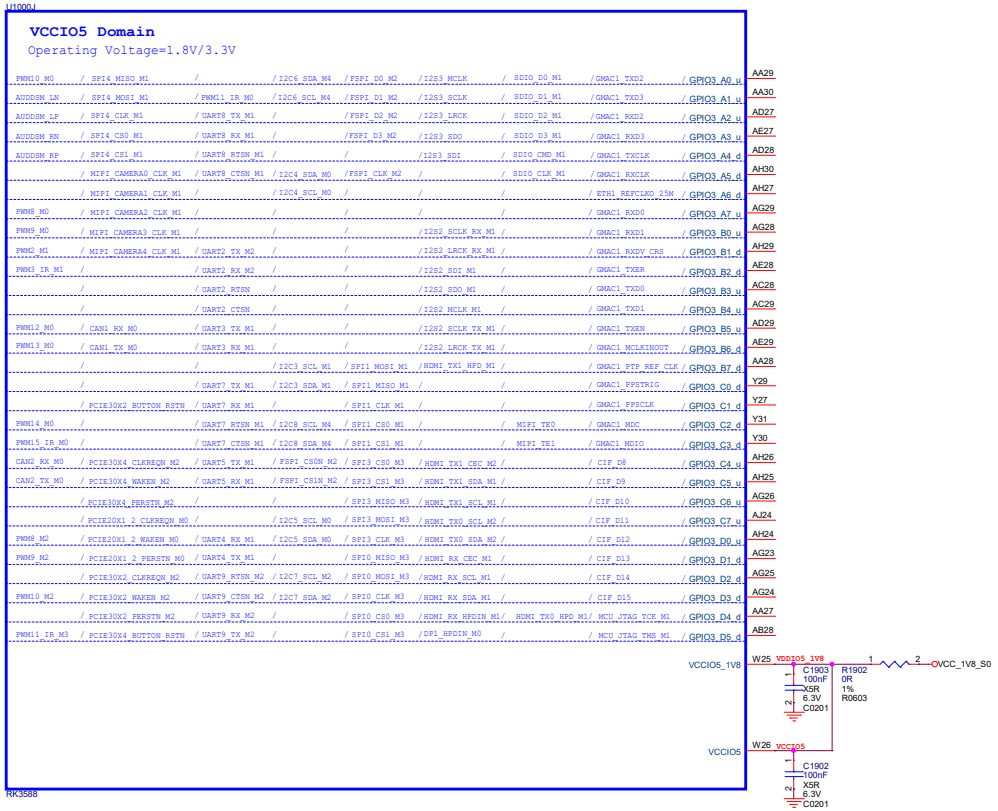
RK3588

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

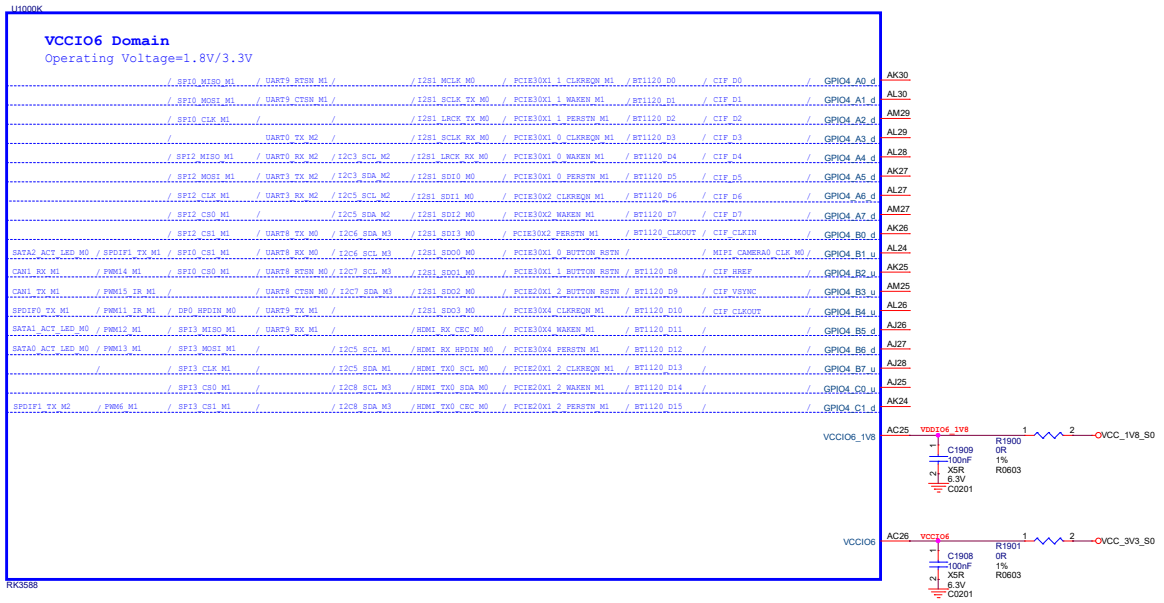
Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

Rockchip Electronics Co., Ltd					
Project:	RK3588_EVB3_LPDDR5				
File:	18.RK3588_PCIE30/PCIE20/SATA30				
Date:	Tuesday, March 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	18 of 99

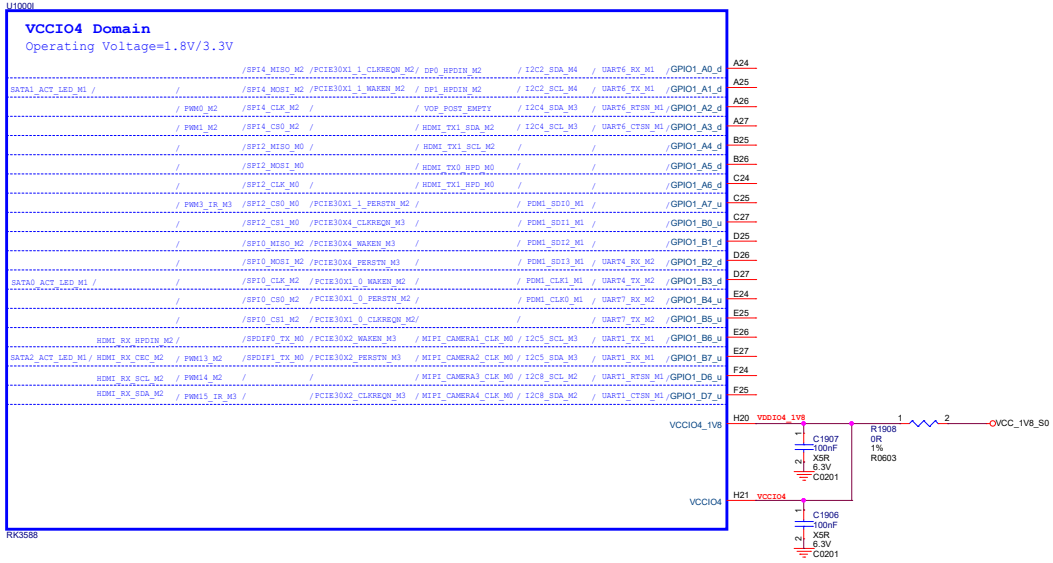
RK3588_J(VCCIO5 Domain)



RK3588_K(VCCIO6 Domain)



RK3588_I(VCCIO4 Domain)



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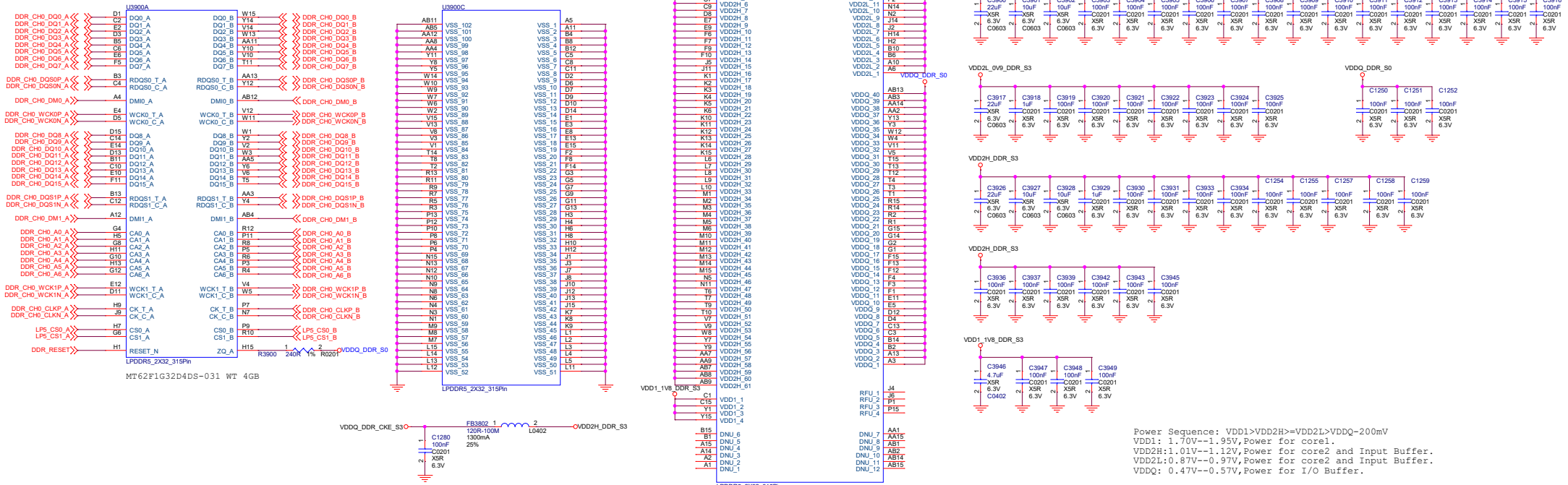
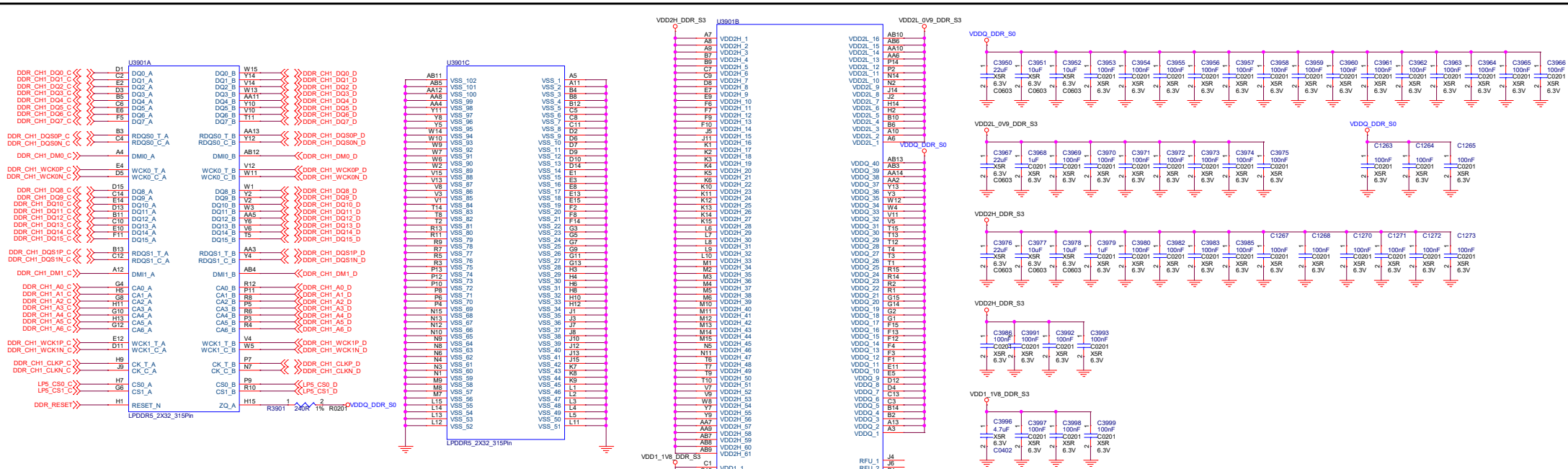
Rockchip Rockchip Electronics Co., Ltd			
Project:	RK3588_EVB3_LPDDR5		
File:	19.RK3588_1.8V/ 3.3V GPIO		
Date:	Tuesday, March 15, 2022	Rev:	V1.0
Designed by: Rzf	Reviewed by:	Sheet:	19 of 99

LPDDR5





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Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_EVB3_LPDDR5		
File:	39.DRAM-LPDDR5X_315P_2X32bit		
Date:	Thursday, March 17, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by: Default	Sheet: 39 of 99

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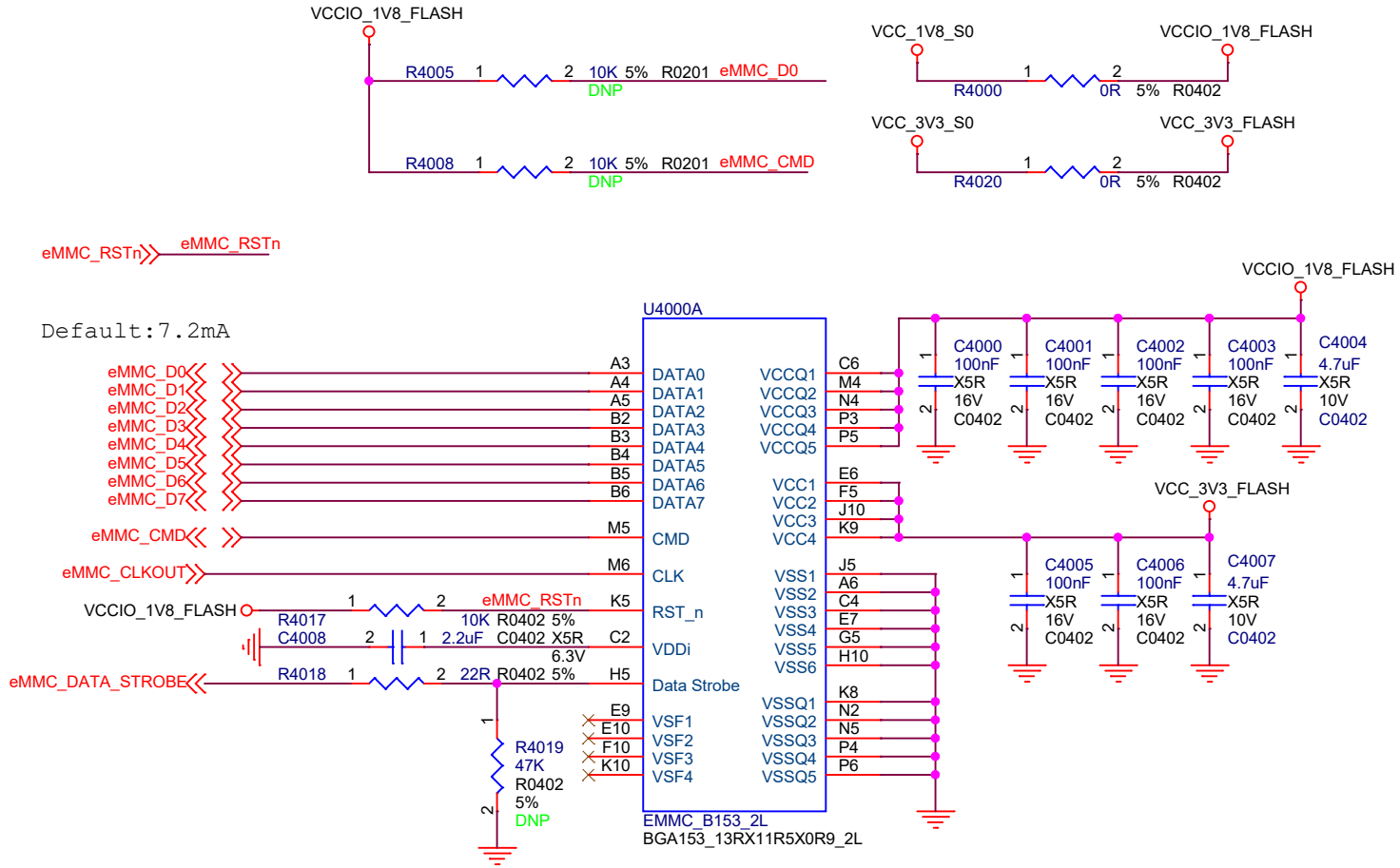
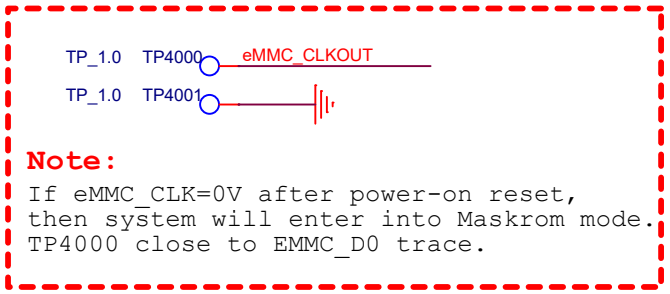
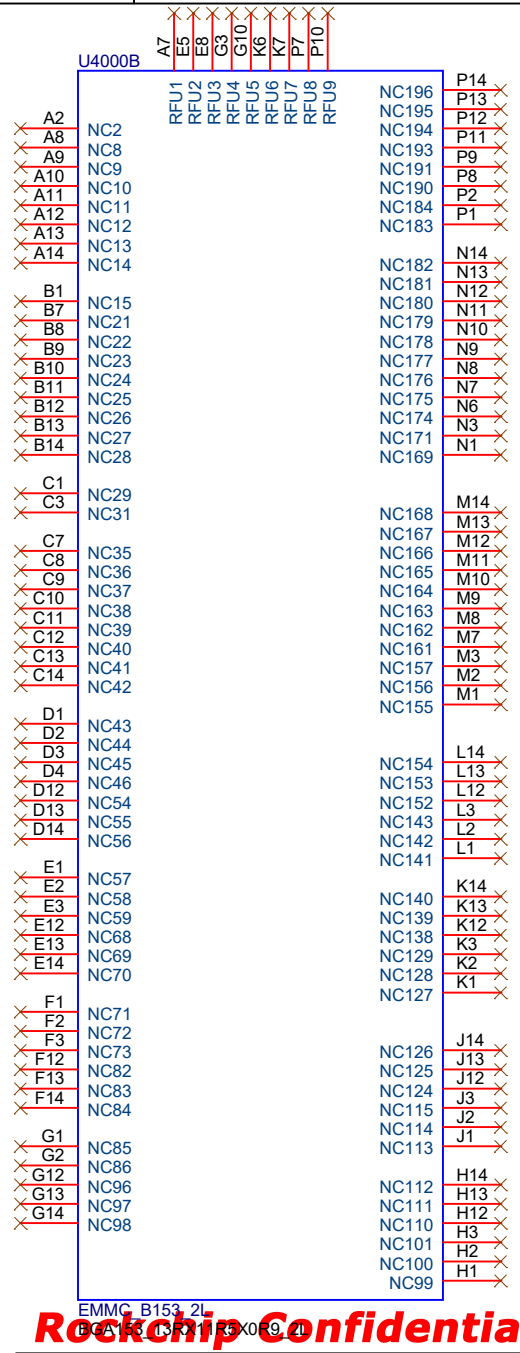
eMMC FLASH



KLMBG2JETD-B041
SDINBDA6-32G-XI1





Rockchip Electronics Co., Ltd			
Project:	RK3588_EVB3_LPDDR5		
File:	40.Flash-eMMC Flash		
Date:	Tuesday, September 28, 2021	Rev:	V1.0
Designed by: Rzf	Reviewed by:	Sheet:	40 of 99