Reference Schematics For RK3588S

RK3588S_Tablet_REF_SCH

Main Functions Introduction

1) Charger: 1Cell Battery_QC or 2Cell Battery_QC
2) PMIC: 1 x RK806-1+DiscretePower
3) RAM: 2 x 32bits LPDDR4/4x or 2 x 32bits LPDDR5
4) ROM: eMMC5.1(Default) or SPI Falsh
5) Support: 1 x Micro SD Card3.0
6) Support: 1 x Type-C 3.0(with DP function) +1 x USB2.0 HOST + 1 x USB3.0 HOST
7) Support: 2 x 4Lanes MIPI D/CPHY RX Camera
8) Support: 2 x 2Lanes MIPI DPHY RX Camera
9) Support: 1 x HDMI2.1 TX or 1 x eDP1.3 TX
10) Support: 2 x 4Lanes MIPI D/CPHY TX
11) Support: a/b/g/n/ac/ax 2T2R WIFI(PCIE) + BT5.0
Or: a/b/g/n/ac 2T2R WIFI(SDIO) + BT5.0
12) Support: 1 x Headphone + 2 x Speaker out + 1 x Analog MIC
13) Support: 2 x PDM MIC Array
14) Support: Gyroscope+G-sensor+Ambient Light+Proximity +Hall Sensor

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	00.Cover Page				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	1 of 54

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Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

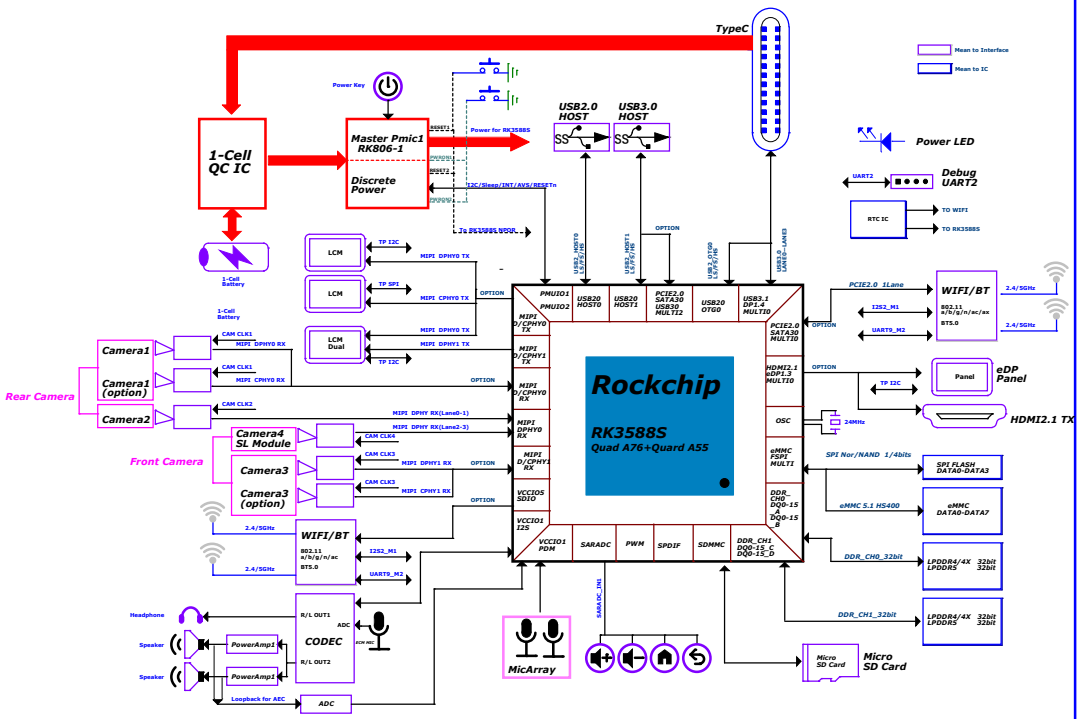
NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	01.Index and Notes				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	2 of 54

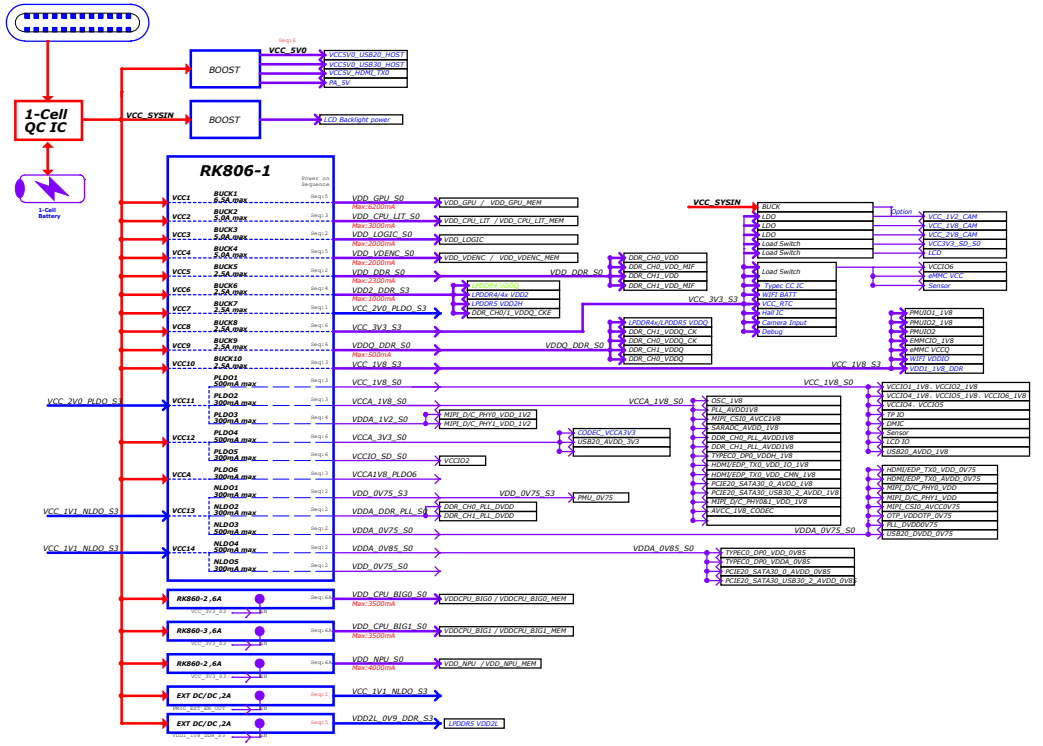
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2022-01-05	Joseph.Wei	1:Revision preliminary version	
V1.1	2022-02-18	Joseph.Wei	1. The capacitance of C1604 and C1612 is changed to 1uF/4V. 2. To reduce standby power consumption, change the PMUIO2 power field to 1.8V, and modify the IO field corresponding to the peripheral IO voltage accordingly 3. Set the inductance of L2203, L2205, L2207, L2300, L2301, L2302 from 0.22uH (TDK) Change to 0.24uH (Sunlord); The inductance of L2201 is changed from 0.22uH (TDK) to 0.22uH (Sunlord), and IND is packaged_ 404020。 4. HDMI eARC function is not supported, and related eARC network is changed to HDMI0_ TX_ SBDP/N	
V1.2	2022-11-10	Joseph.Wei	1. Change the measured current data on Page PAGE04 and Page PAGE10 2. Change the package of RK3588S and add the use description of MIPI D/C PHY (1lane or 2Lane is recommended) 3. SPK PA model TT8642 is changed to TCS7191A 4. Add SPK PA reference circuit of AW88394 5. Delete HDMI eARC function supports description 6. Add the manufacturer and model of 2A/3A BUCK in the drawing 7. The pull-down resistance of HDMI is changed from 499ohm to 590ohm. 8. RK3588S Delete the network "PMIC_PWR_CTRL3" (Pin AG36). 9. MP8759 add MODE SELECT control. 10.HDMI/EDP_ TX0_ VDD_ Change 0V75 voltage network to "HDMI_VDDA0V85_S0" (The output terminal is RK806-1 NLDO5) The actual software setting is 0.8375V. 11. Correct power network VDD2L_ 0V9_ DDR_ S3 suspension problem. 12. When using SDIO WiFi, the VCCIO5 power supply will remain powered by default in standby mode. 13. Update 1Cell_QC function 14.2Cell_QC's Gas Gauge changed to CW2017AAAAD 15. Fast charging function increase discharge circuit 16.Update power VCCIO_ FLASH power supply path 17.Power Supply VCCA_ 1V8_ S0 moves to RK806-1 PLDO1 Power Supply VCC_ 1V8_ S0 moves to RK806-1 PLDO2 18.USB_ AVDD_ 1V8 power supply fixed to VCCA_ 1V8_ S0 19.The sensor MPU6500 model is changed to ICM_20600	

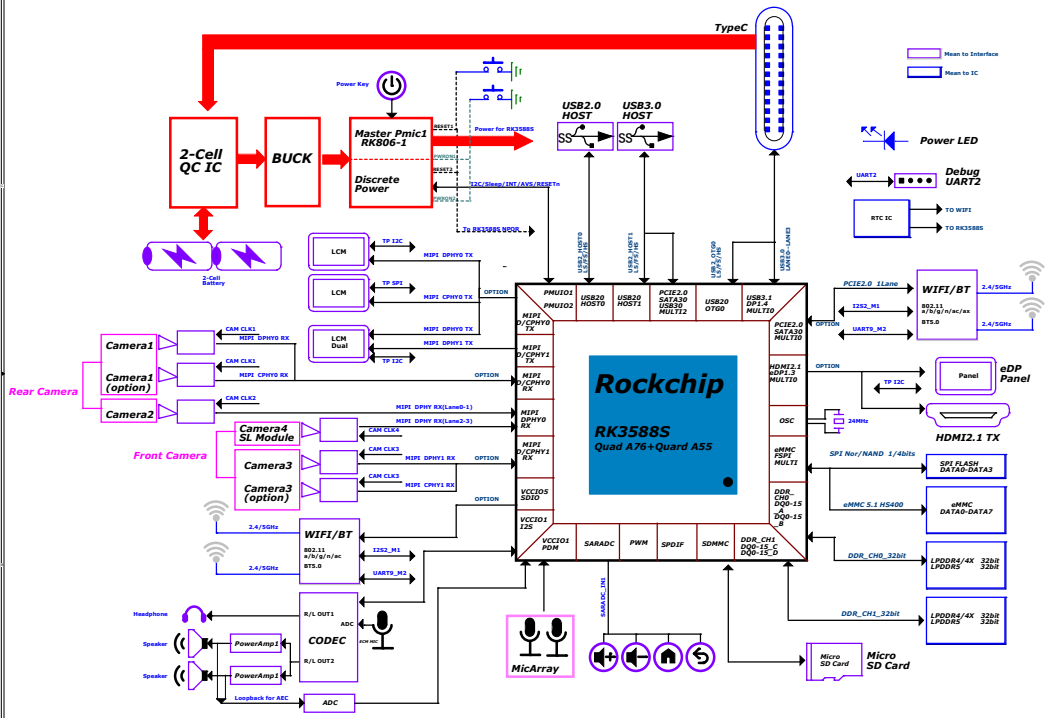
RK3588S Tablet Ref Block Diagram for 1-Cell Charger



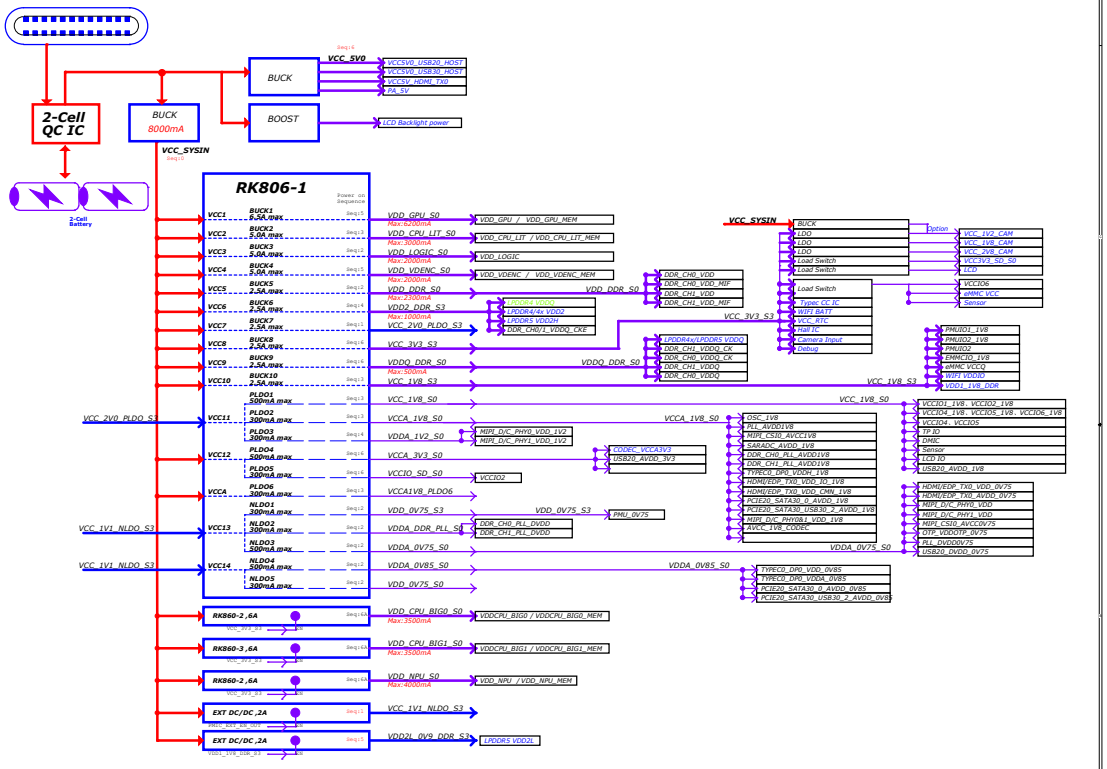
Power tree for 1-Cell Charger



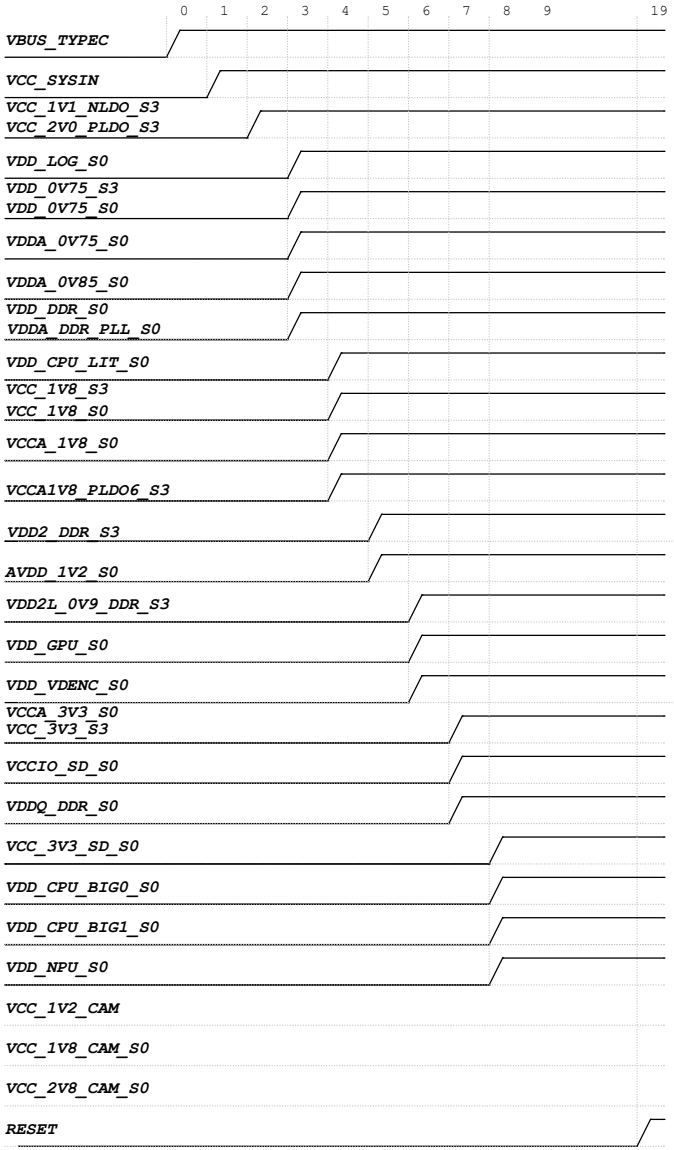
RK3588S Tablet Ref Block Diagram for 2-Cell Charger



Power tree for 2-Cell Charger



Power Sequence



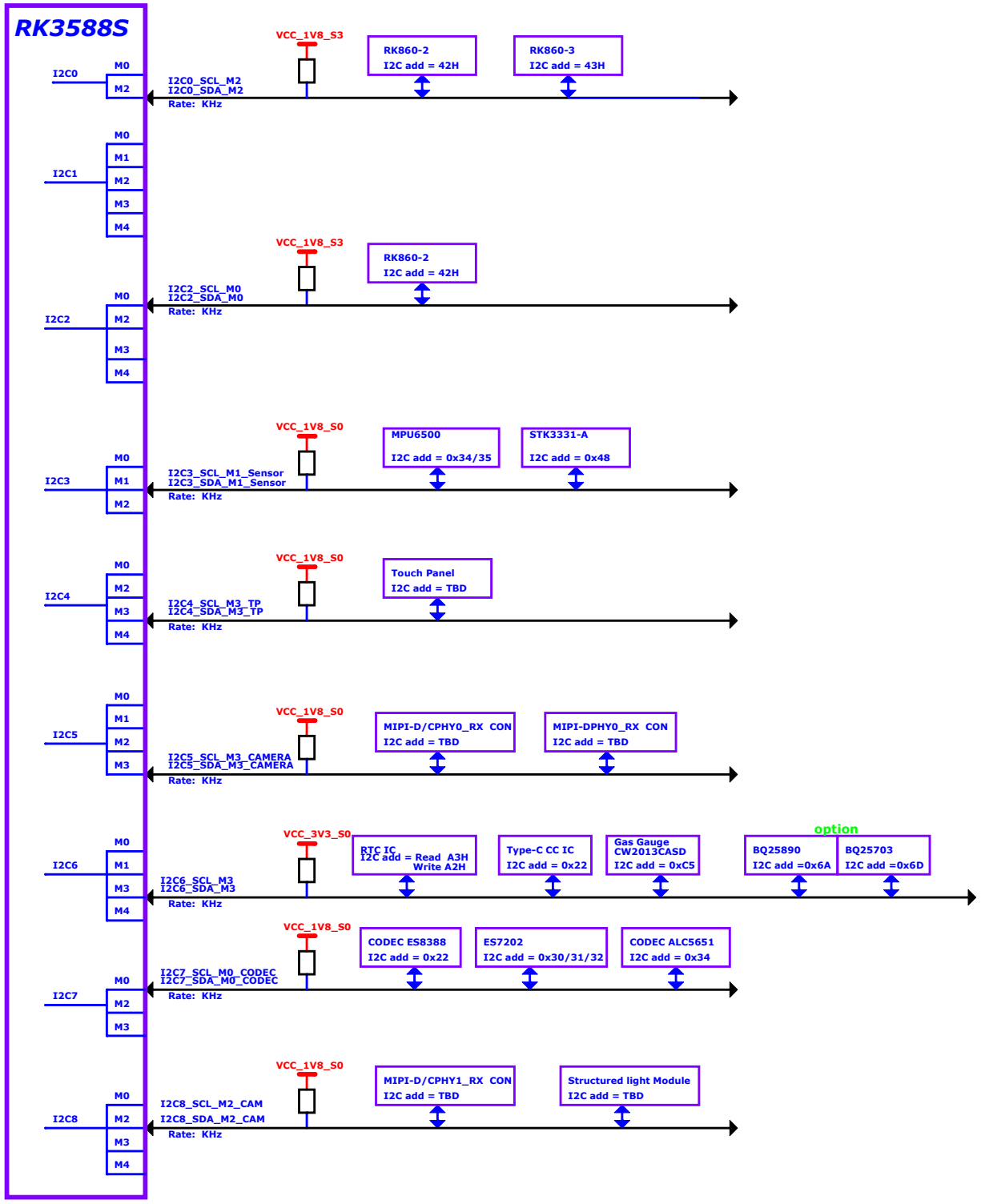
Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

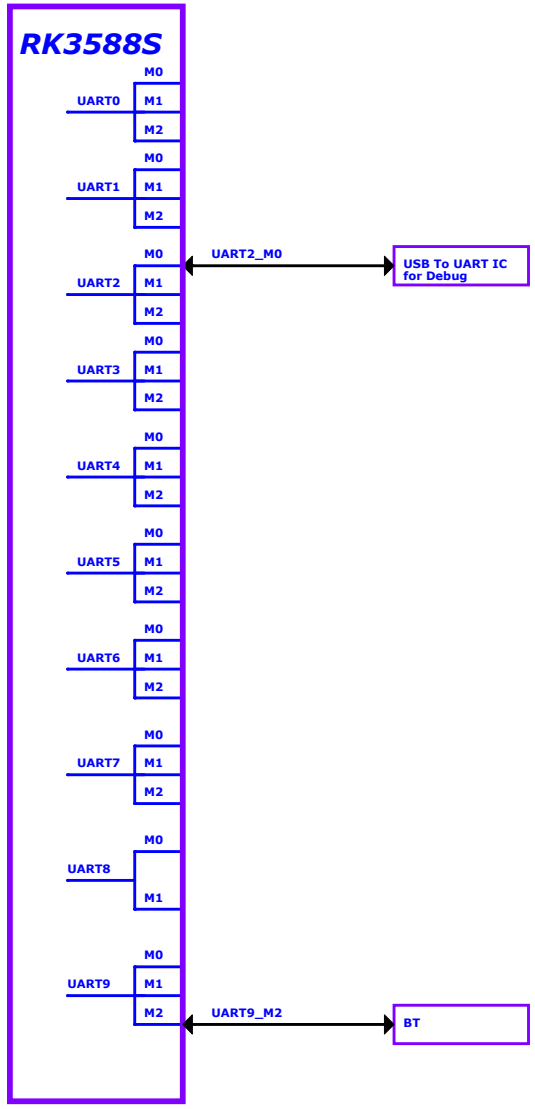
IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37 Pin V35 V36	1.8V or 3.3V	PMUIO2_1V8 PMUIO2_	VCC_1V8_S3 VCC_1V8_S3	1.8V 1.8V
EMMCIO	Pin AC35 Pin AC36	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11 Pin AK10	1.8V or 3.3V	VCCIO2_1V8 VCCIO2_	VCC_1V8_S0 VCC_IO_SD	1.8V 1.8V/3.3V
VCCIO4	Pin G27 G28 Pin G31	1.8V or 3.3V	VCCIO4_1V8 VCCIO4_	VCC_1V8_S0 VCC_3V3_S0	1.8V 1.8V
VCCIO5	Pin AF35 AF36 Pin AC33 AC34	1.8V or 3.3V	VCCIO5_1V8 VCCIO5_	VCC_1V8_S0 VCC_1V8_S0	1.8V 1.8V
VCCIO6	Pin AJ34 Pin AL33 AM33	1.8V or 3.3V	VCCIO6_1V8 VCCIO6_	VCC_1V8_S0 VCC_3V3_S0	1.8V 3.3V

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	05.System Power Sequence				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	6 of 54

I2C MAP



UART MAP



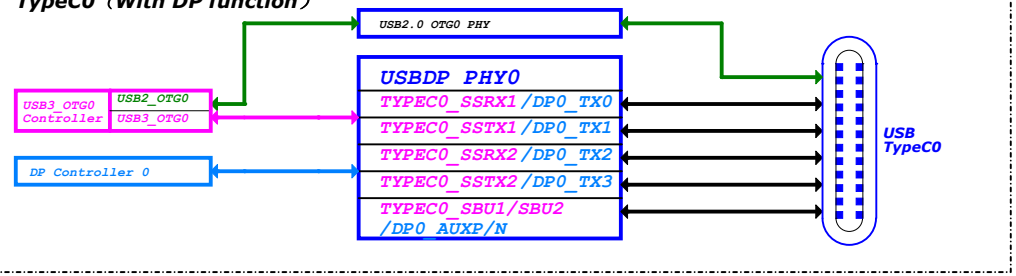
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Tablet_REF
File:	06.Lower-Speed Bus Map
Date:	Monday, November 07, 2022
Rev:	V12
Designed by:	Joseph
Reviewed by:	<Checker>
Sheet	7 of 54

USB Controller Configure Table

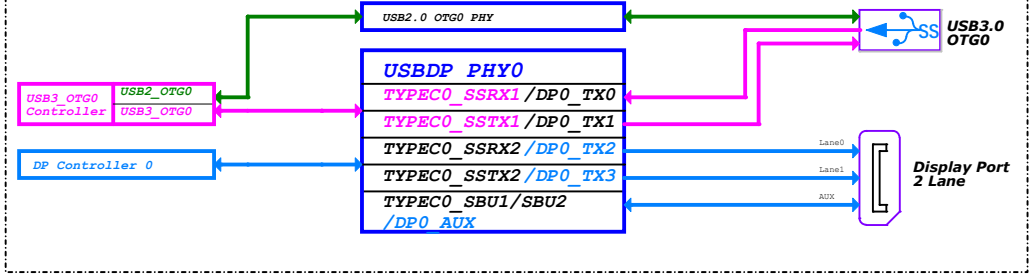
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N			DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N			DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM		TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM		TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST					
USB30 OTG2 Device or Host	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN					
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN					
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

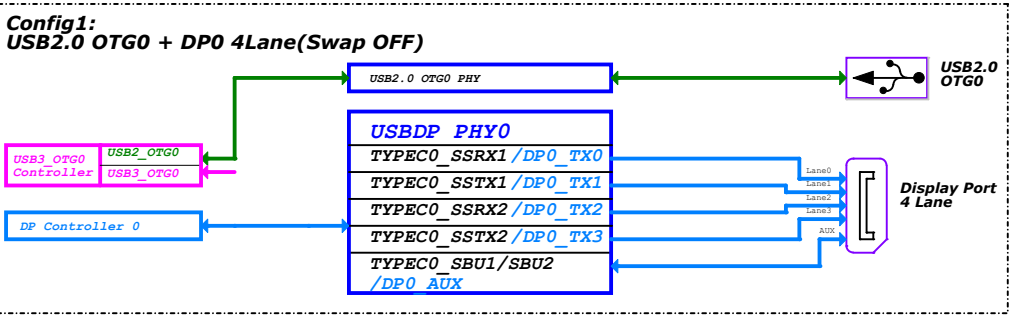
Config0:
TypeC0（With DP function）



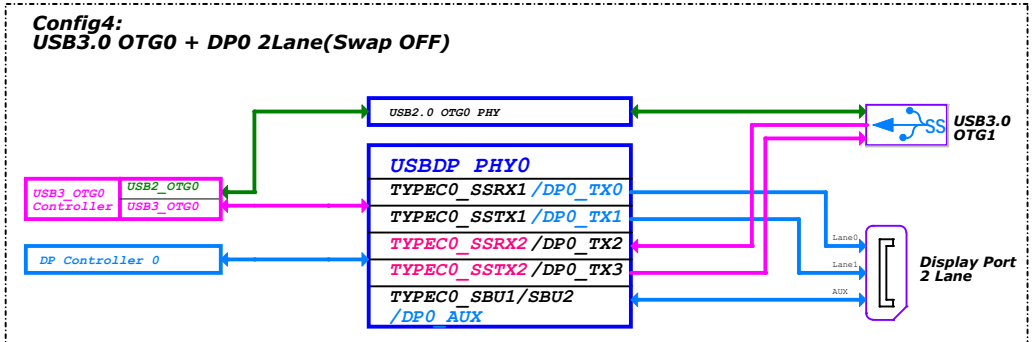
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



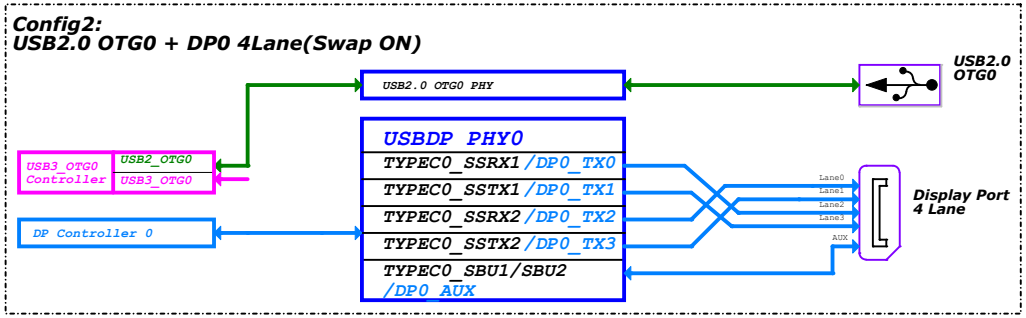
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Tablet_REF
File:	07.USB Controller Configure Tab
Date:	Thursday, November 03, 2022
Designed by:	Joseph
Reviewed by:	<Checker>
Rev:	V13
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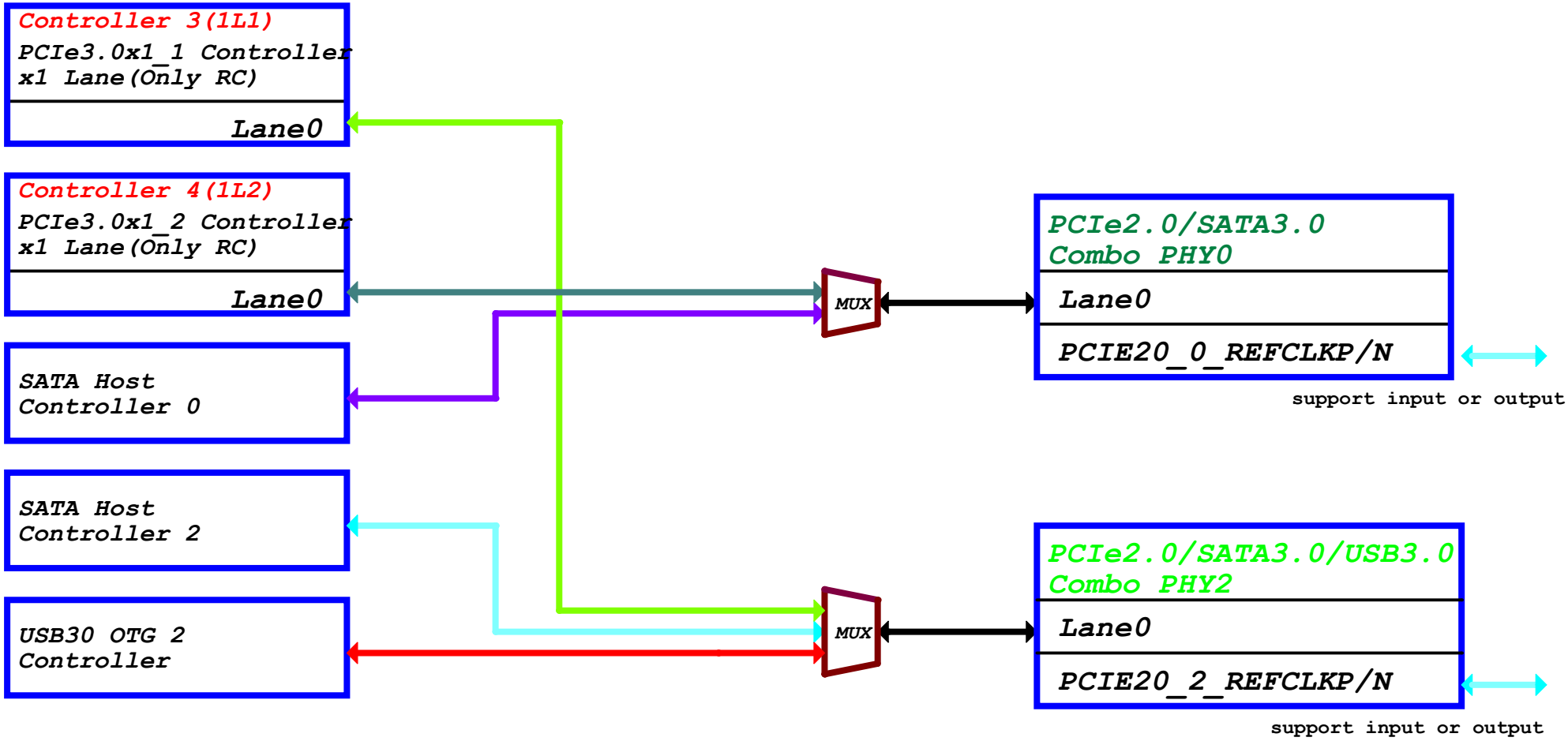
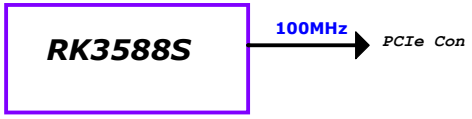
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

PCIe2.0 REFCLK



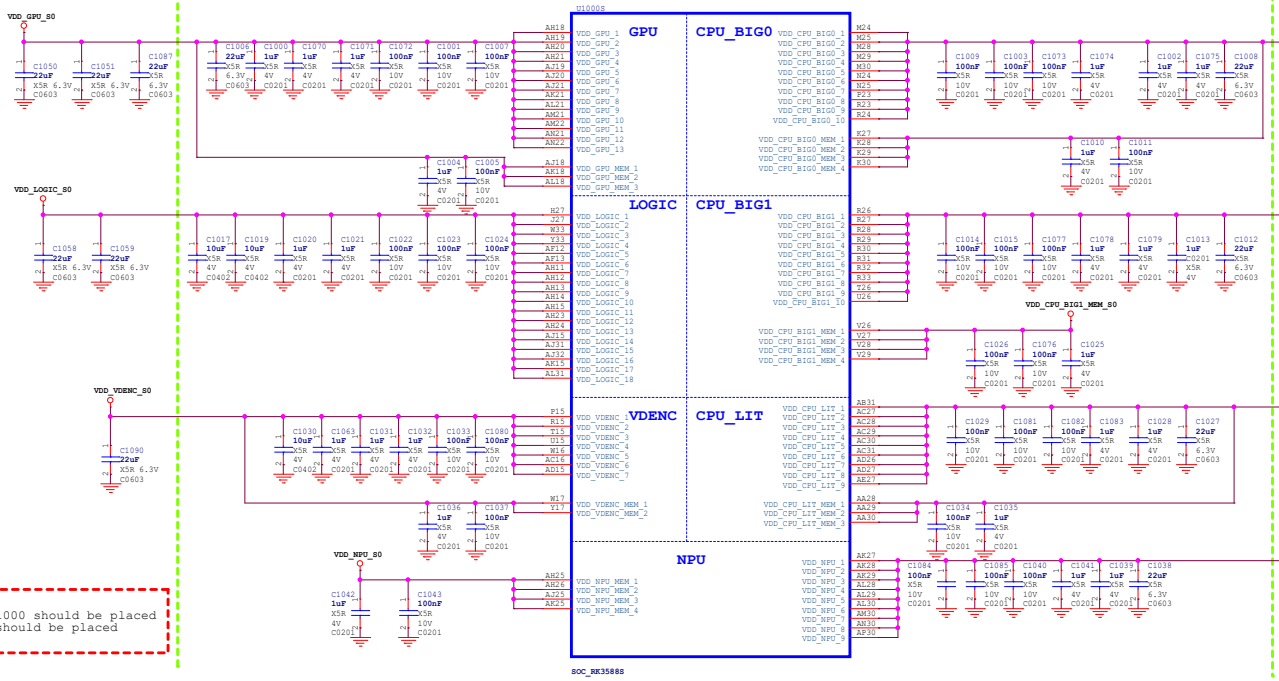
Note:

PCIE20_*_REFCLKP/N is output or input gpio

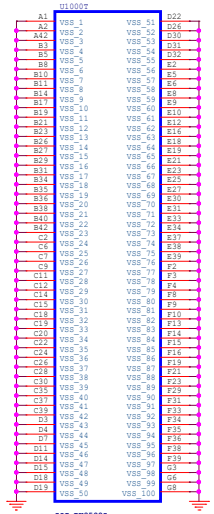
M*=Mean to M0 or M1 or M2,It's the same source,Just multiplex to M0 or M1 or M2,Only use one at the same time.

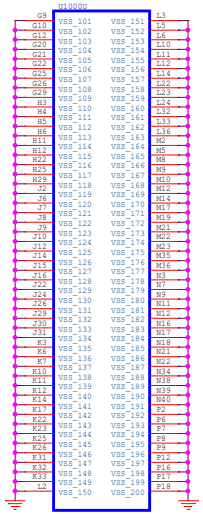
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	08.PCIE Fun Map				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	9 of 54

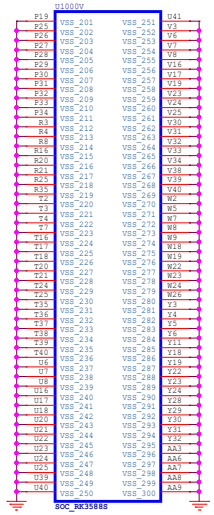
RK3588S(Power&Gnd)

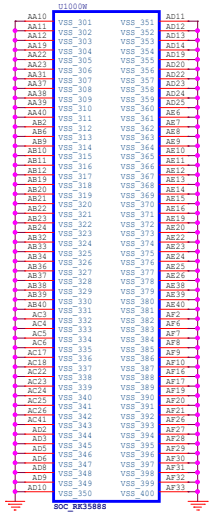


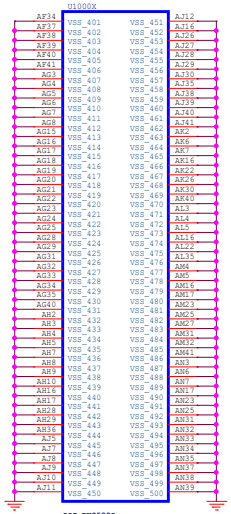
Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

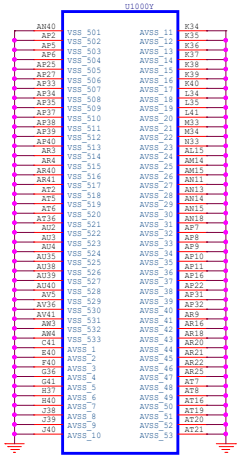












Rockchip Confidential

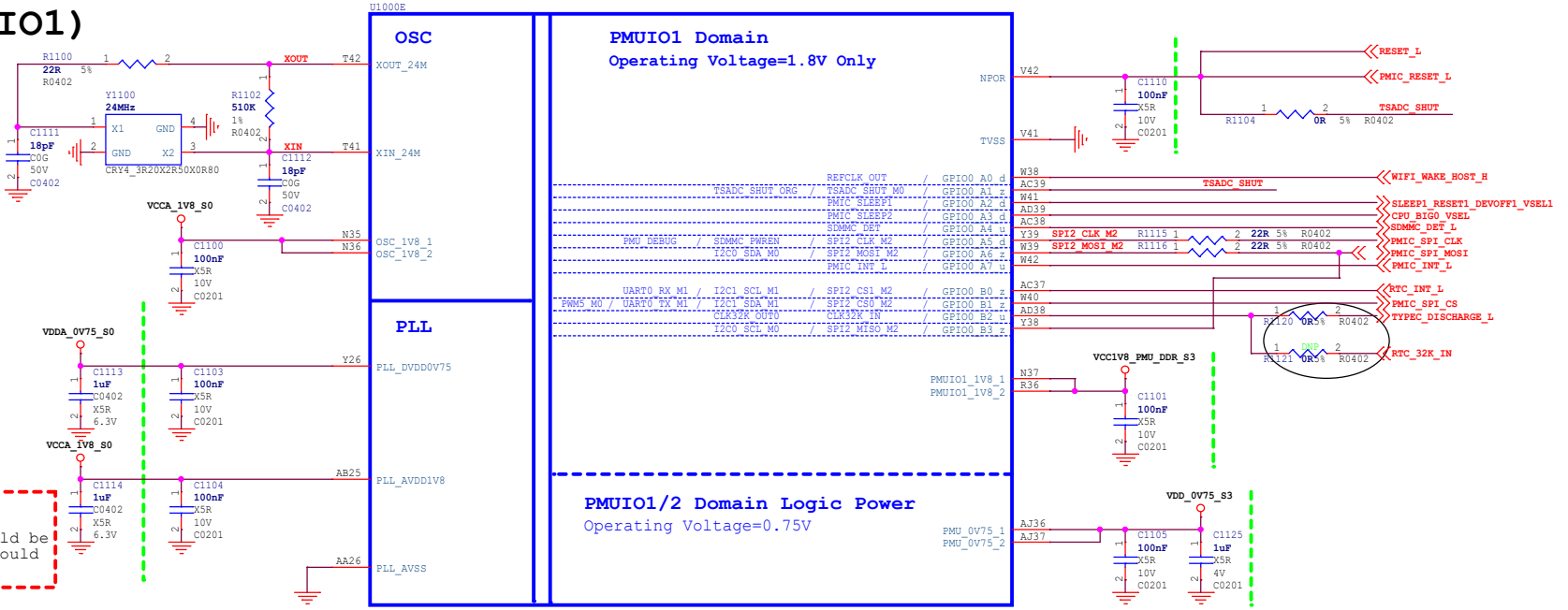
Rockchip Electronics Co., Ltd			
Project:	RK3588S_Tablet_REF		
File:	10.RK3588S_Power&GND		
Date:	Thursday, November 03, 2022	Rev:	V12
Designed by: Joseph	Reviewed by: <Checker>	Sheet	10 of 54

RK3588S(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

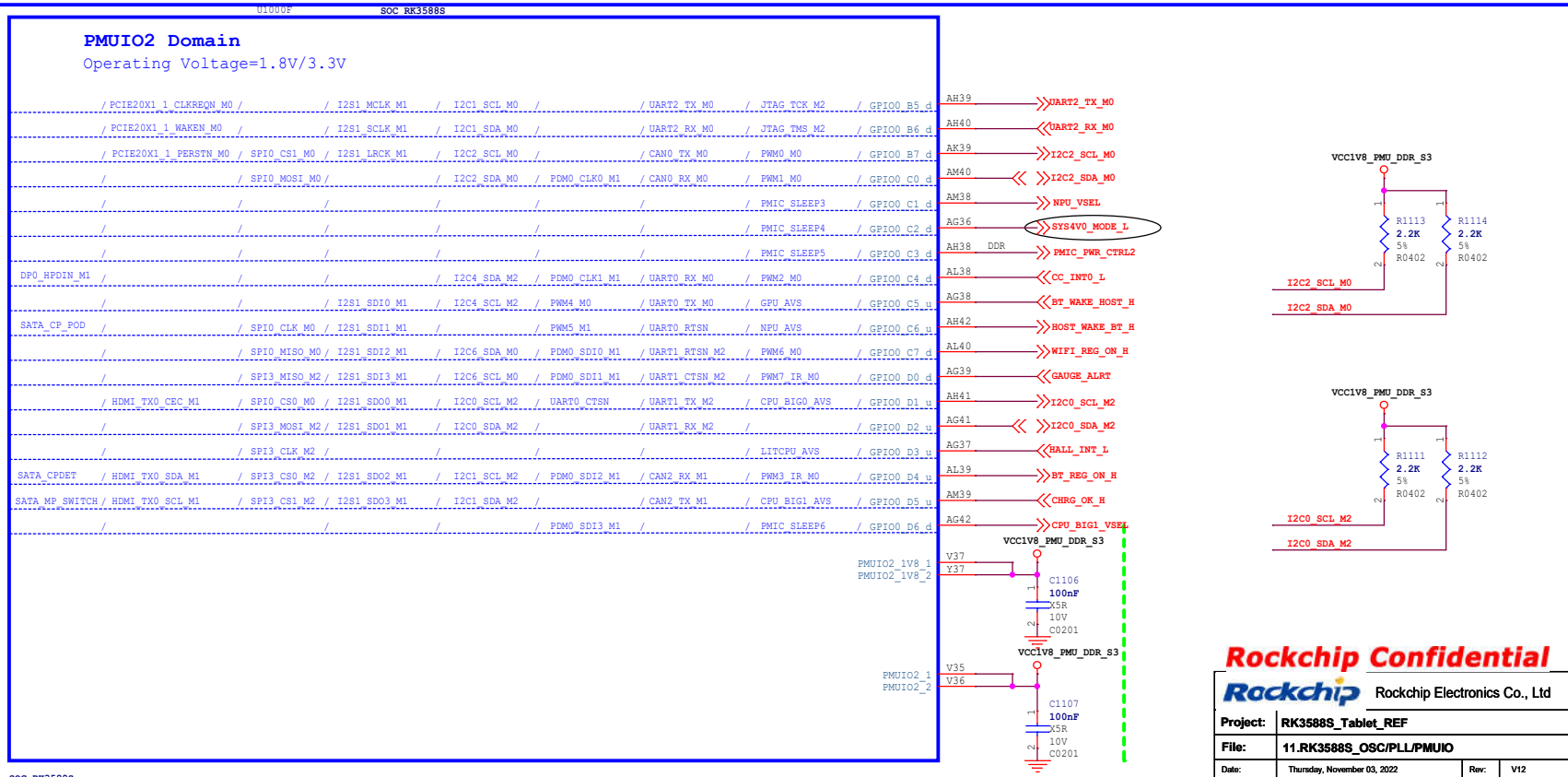
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

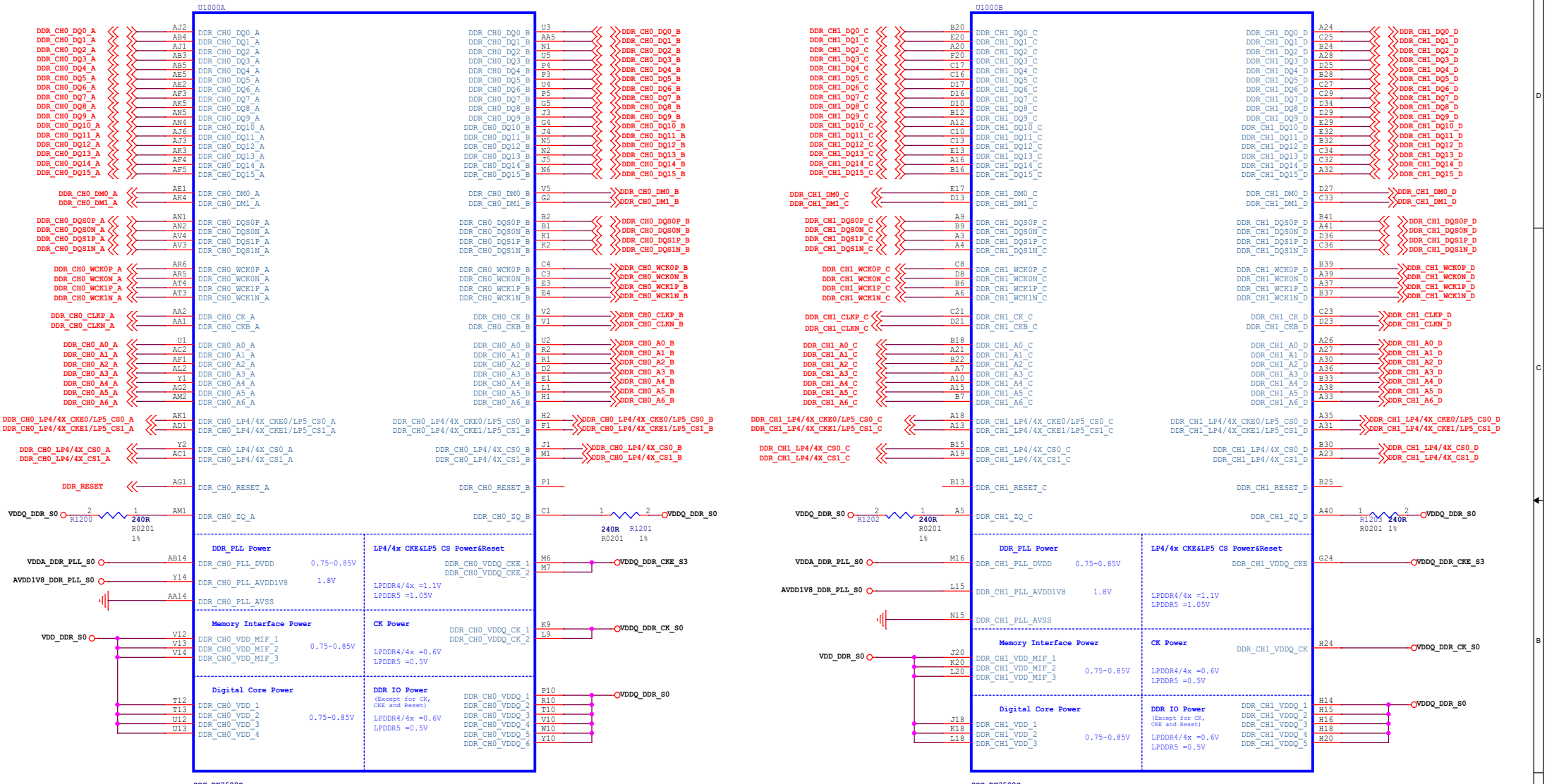
RK3588S(PMUIO2)



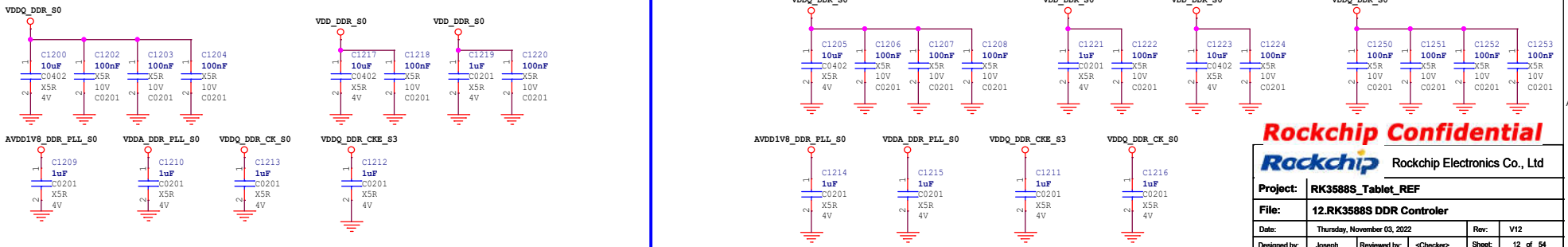
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	11.RK3588S_OSC/PLL/PMUIO				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	11 of 54

RK3588S(DDR PHY)

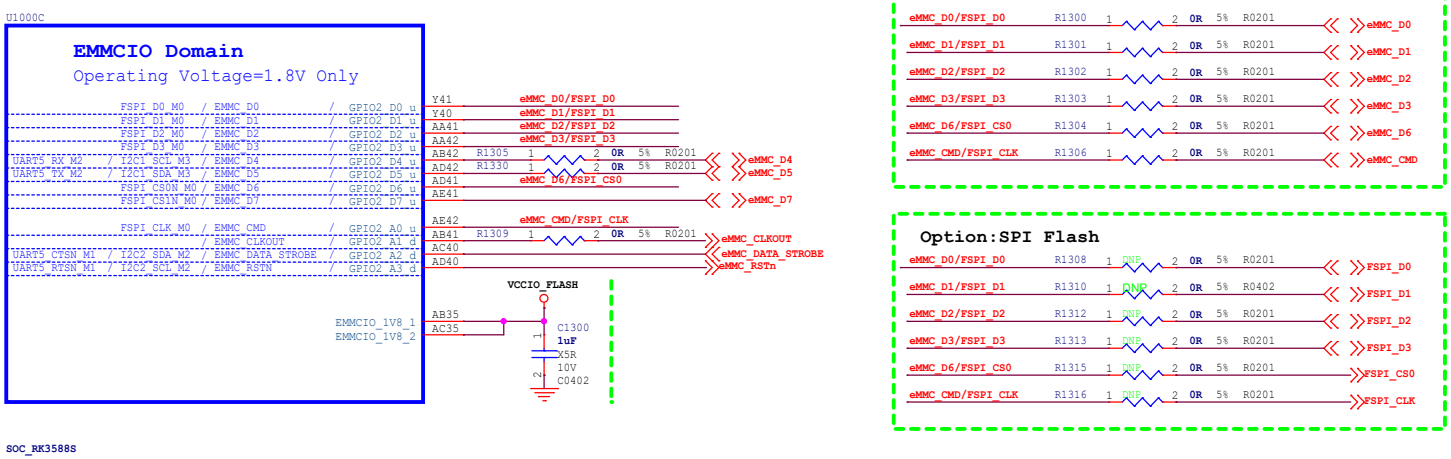


DDR FILTER

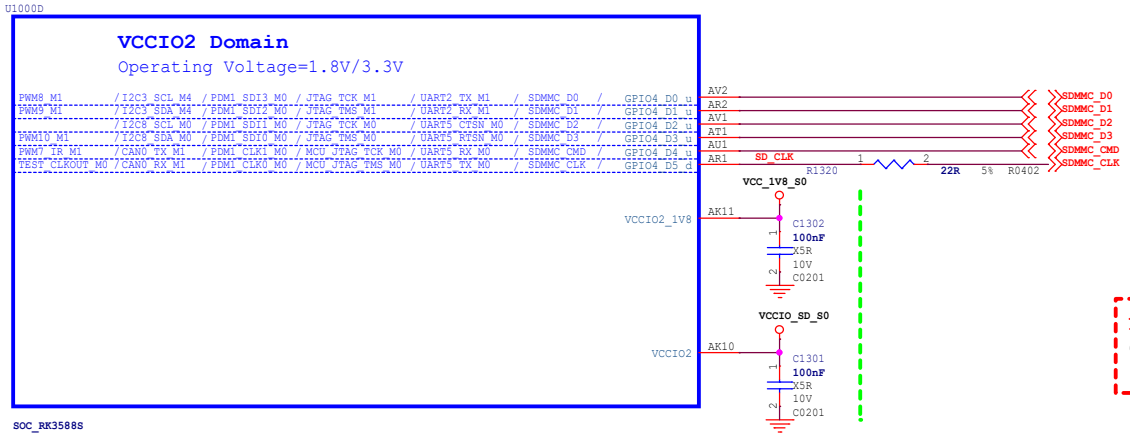


Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	12.RK3588S DDR Controler				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	12 of 54

RK3588S(EMMCIO Domain)



RK3588S(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

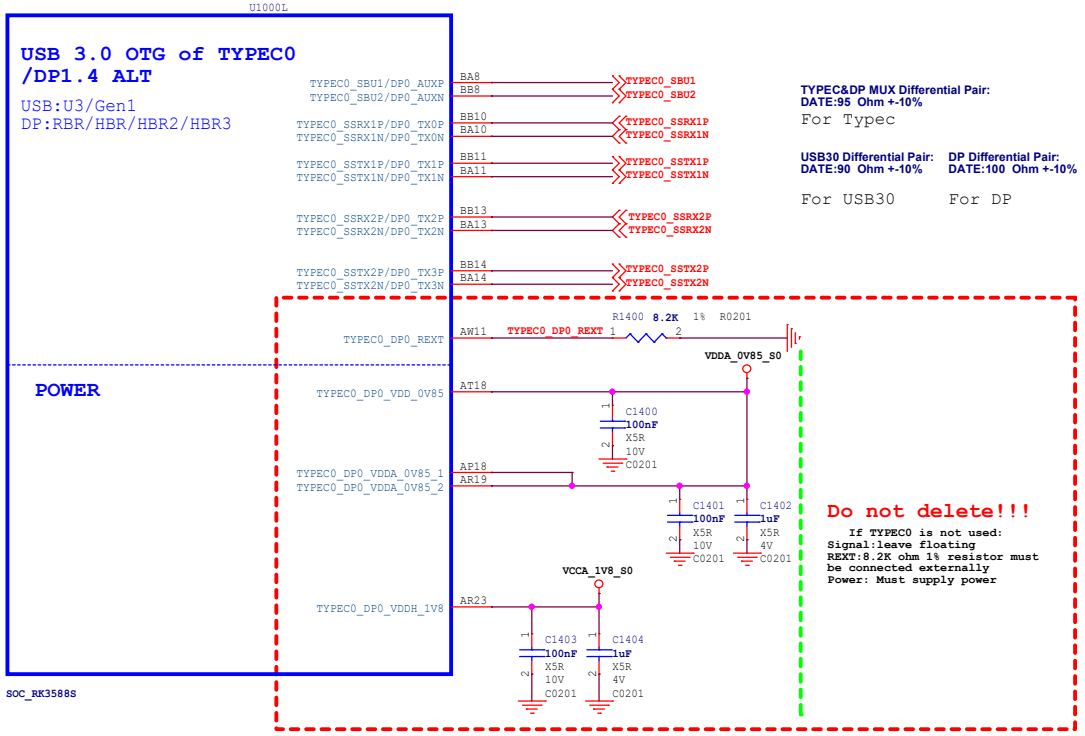
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	13.RK3588S Flash/SD Controller				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	13 of 54

RK3588S(USB3.0/DP1.4)

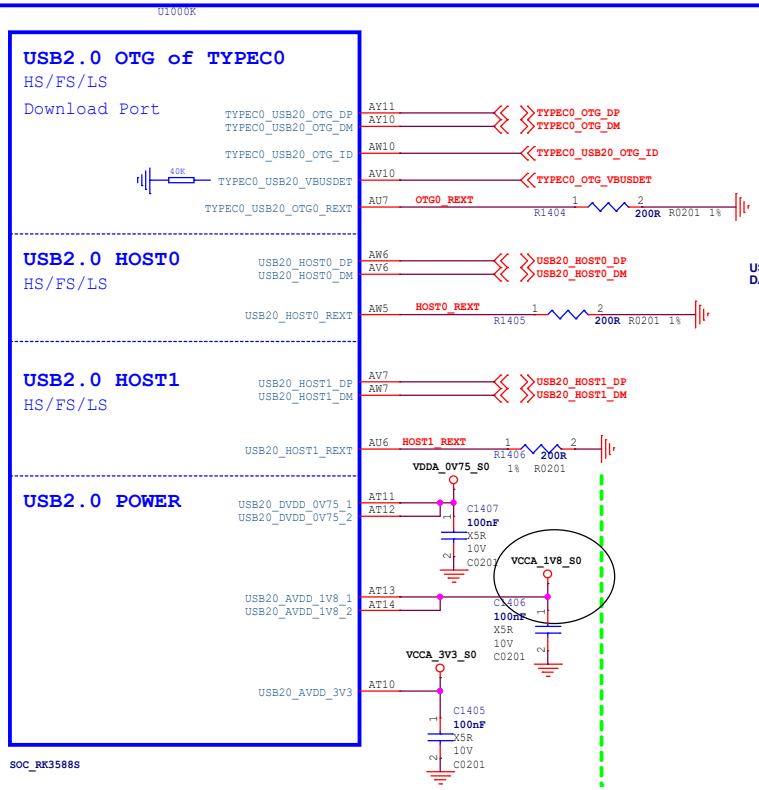
USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N



RK3588S(USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:

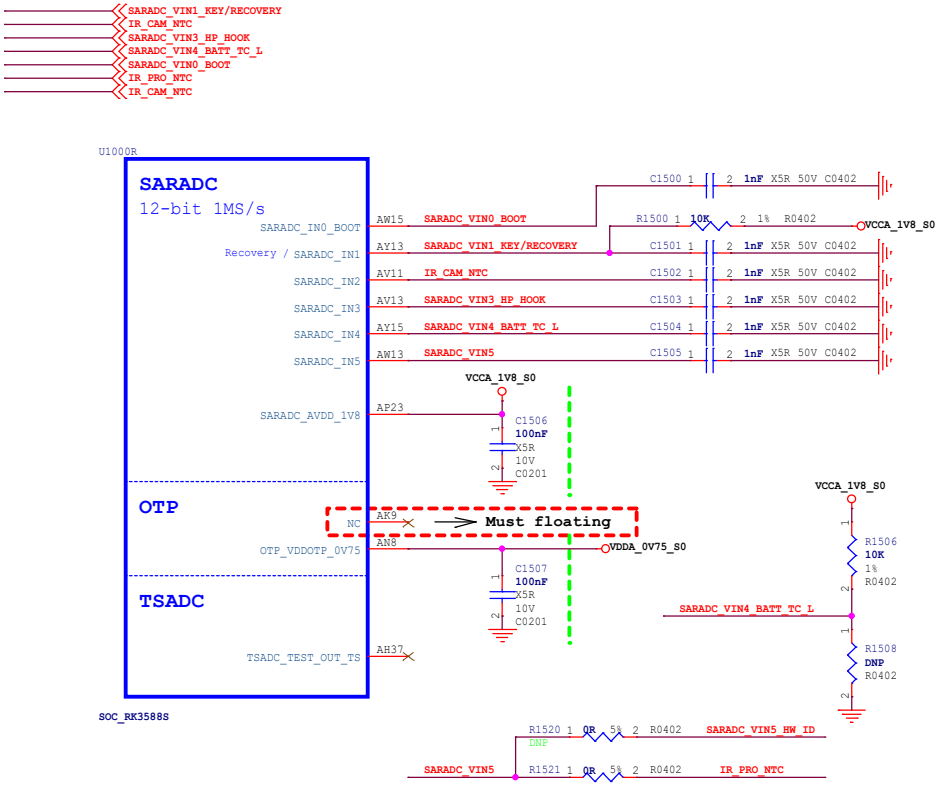
If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

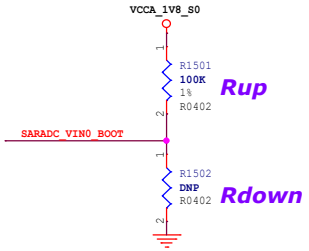
Rockchip Electronics Co., Ltd

Project:	RK3588S_Tablet_REF				
File:	14.RK3588S_USB20/USB30/DP PHY				
Date:	Friday, November 04, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	14 of 54

RK3588S(SARADC/OTP/TSADC)

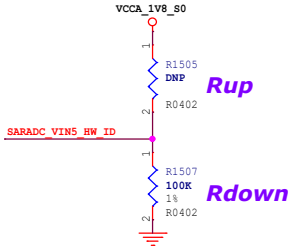


BOOT MODE CONFIG



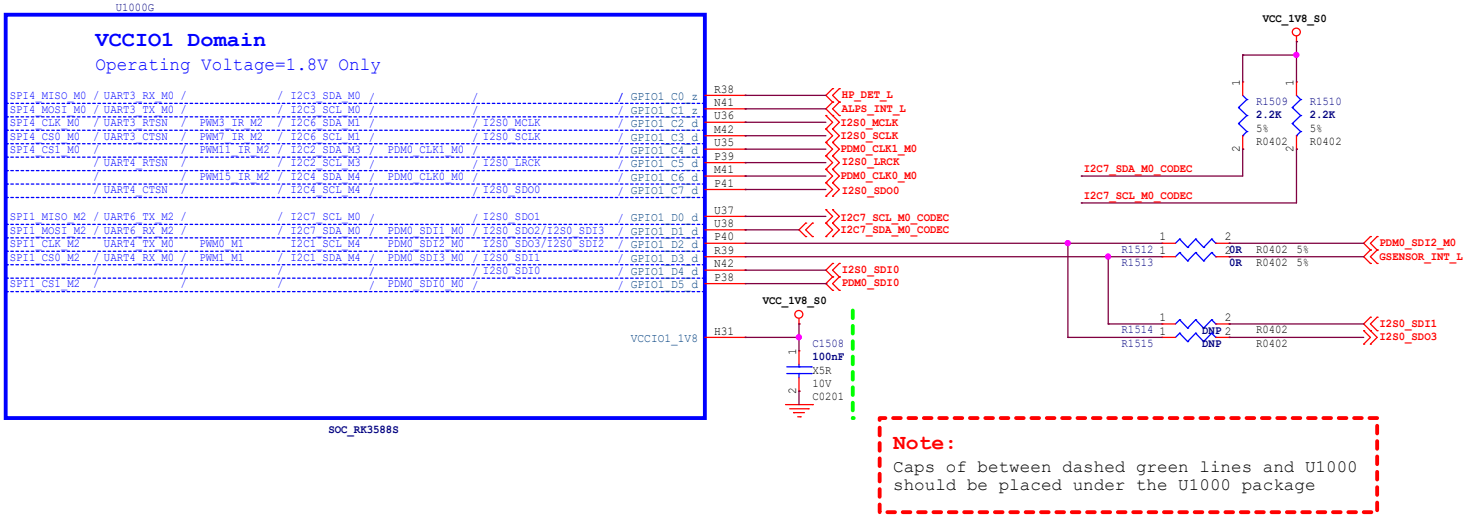
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

BOARD ID CONFIG



Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V1.0
LEVEL2	100K	20K	682	V2.0
LEVEL3	100K	51K	1365	V3.0
LEVEL4	100K	100K	2047	V4.0
LEVEL5	100K	200K	2730	V5.0
LEVEL6	100K	499K	3412	V6.0
LEVEL7	100K	DNP	4095	V7.0

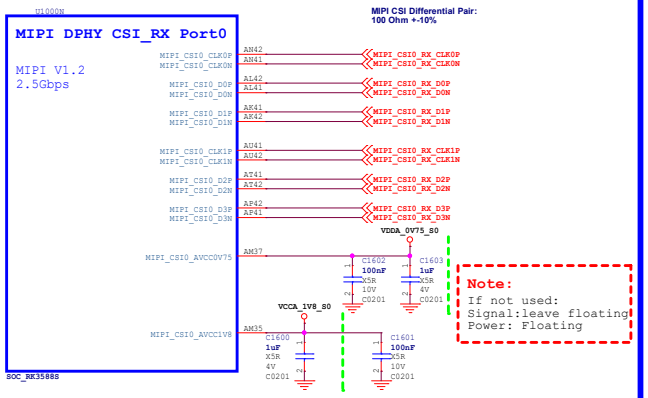
RK3588S(VCCIO1 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	15.RK3588S_SARADC/1.8V GPIO				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	15 of 54

RK3588S(MIPI_DPHY CSI0 RX)



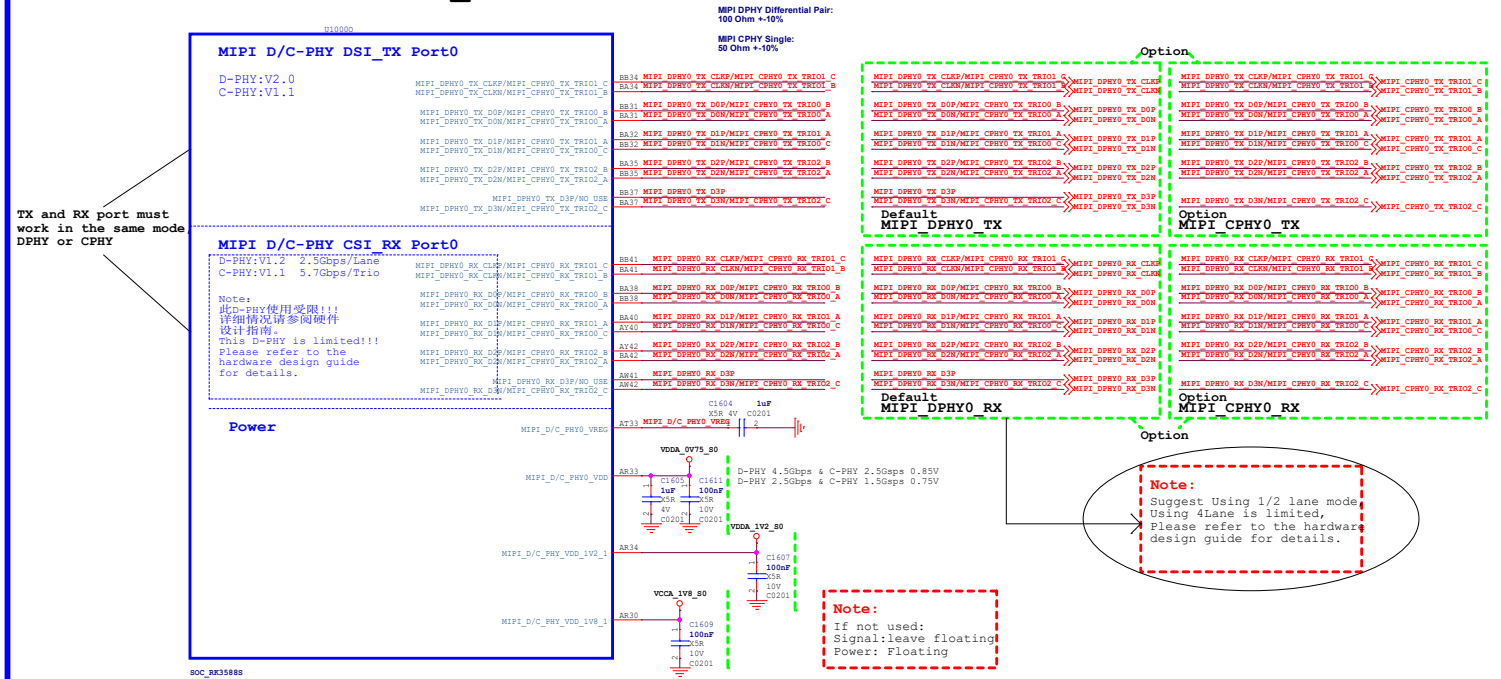
Note:
If not used:
Signal:leave floating
Power: Floating

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

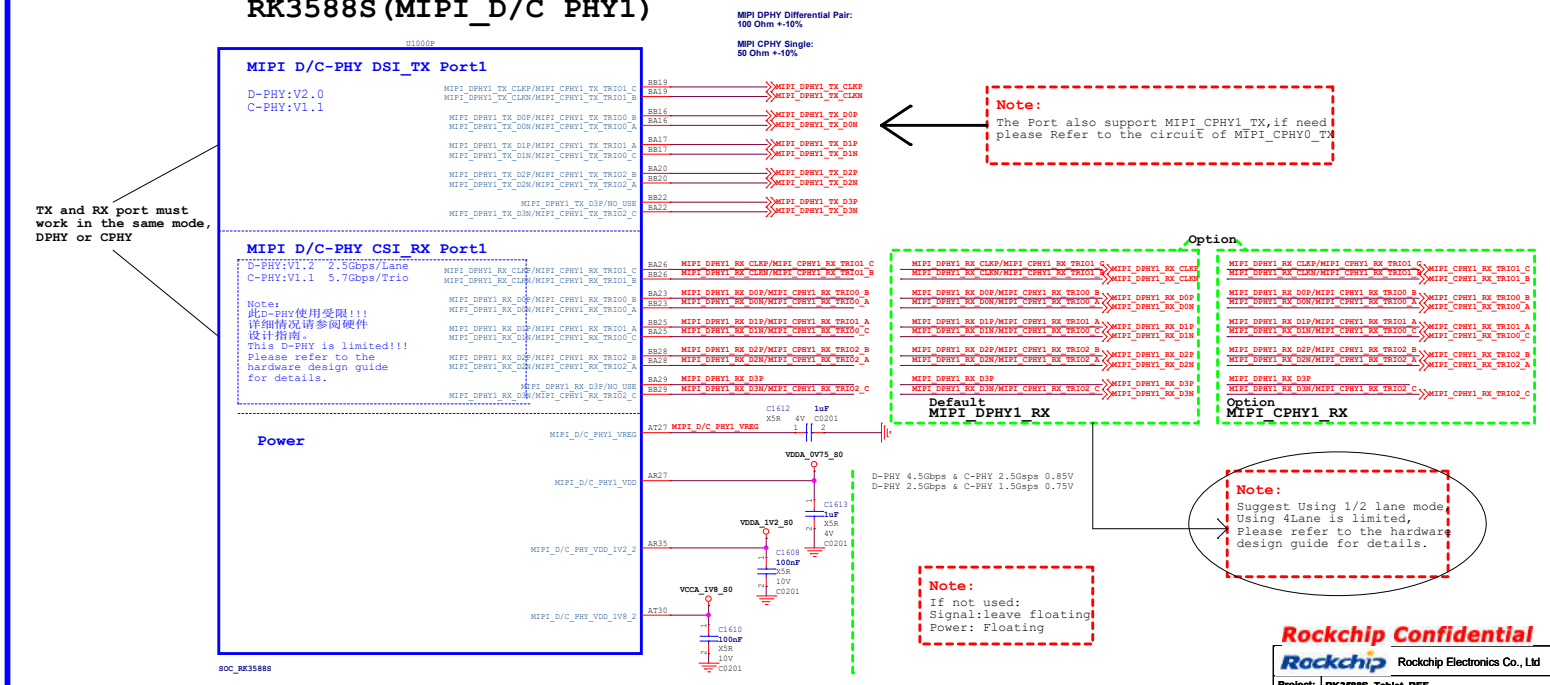
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(MIPI_D/C PHY0)



Note:
If not used:
Signal:leave floating
Power: Floating

RK3588S(MIPI_D/C PHY1)



Note:
If not used:
Signal:leave floating
Power: Floating

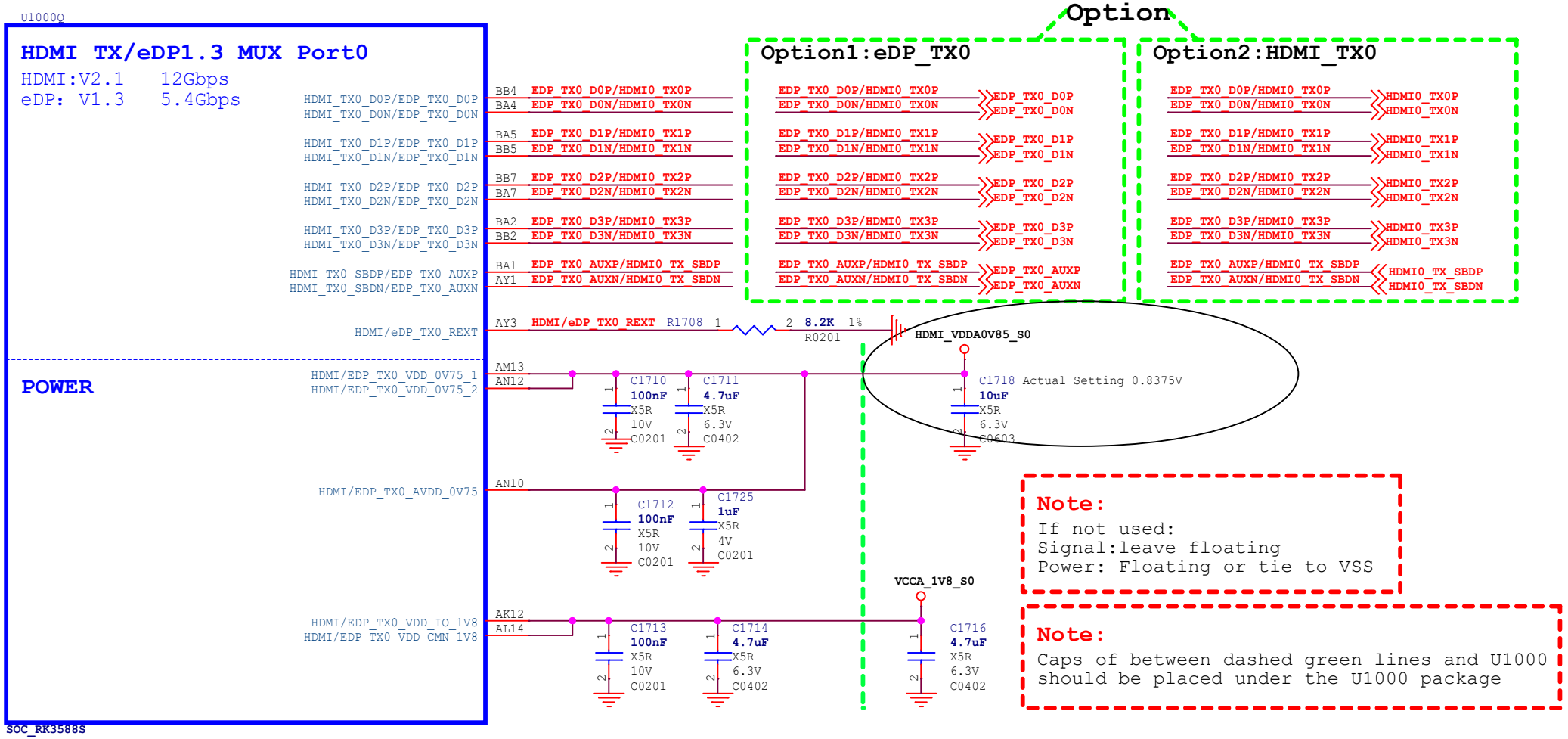
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Tablet_REF
File:	16.RK3588S_MIPI Interface
Date:	Thursday, November 03, 2022
Rev:	V12
Designed by:	Joseph
Reviewed by:	<Checker>
Sheet	16 of 54

RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

eDP TX
100 Ohm ±10%

HDMI TX
100 Ohm ±10%



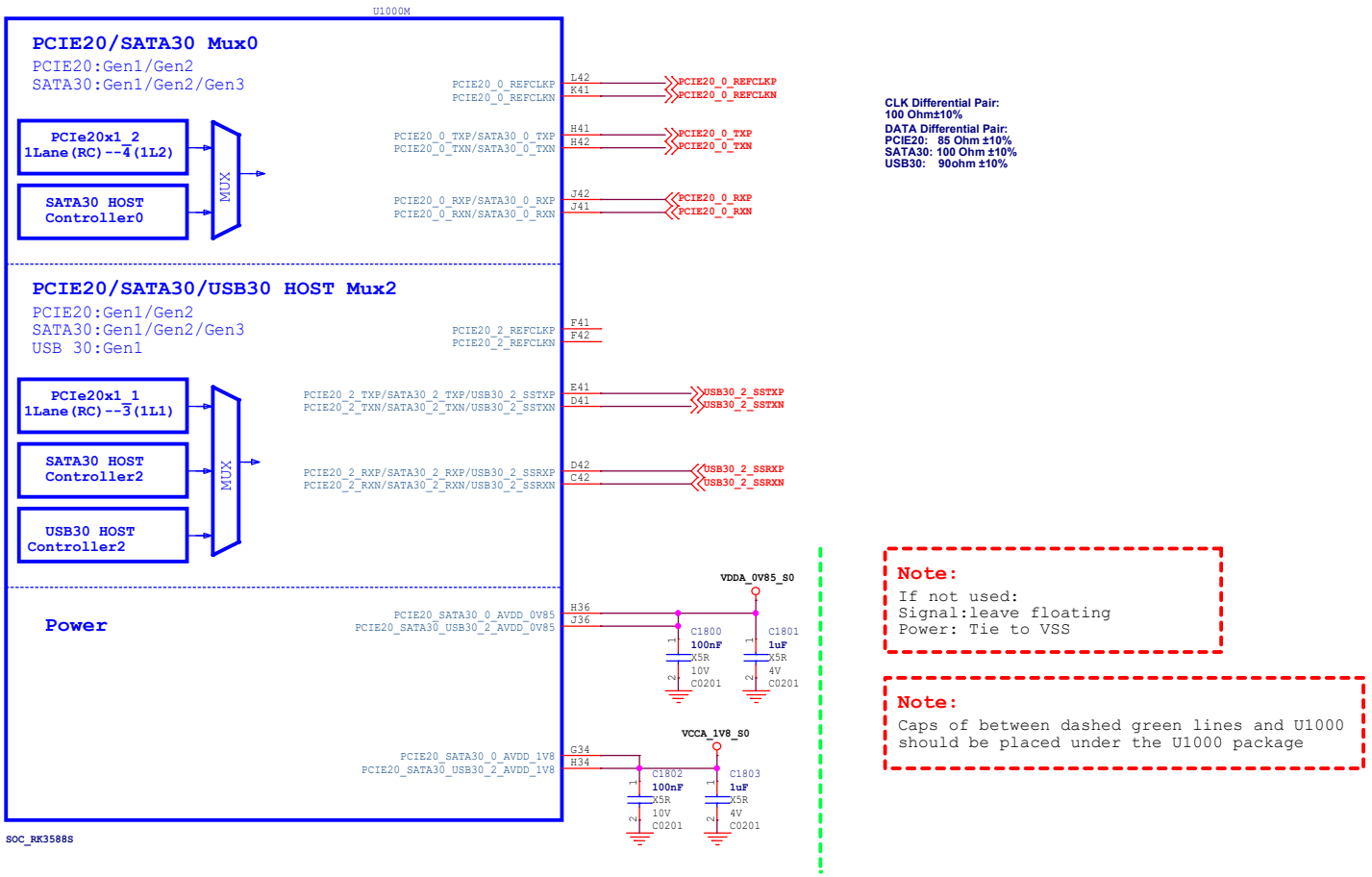
Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	17.RK3588S_HDMI/eDP Interface				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	17 of 54

RK3588S(PCIE20/SATA30/USB30)



Note:
If not used:
Signal:leave floating
Power: Tie to VSS

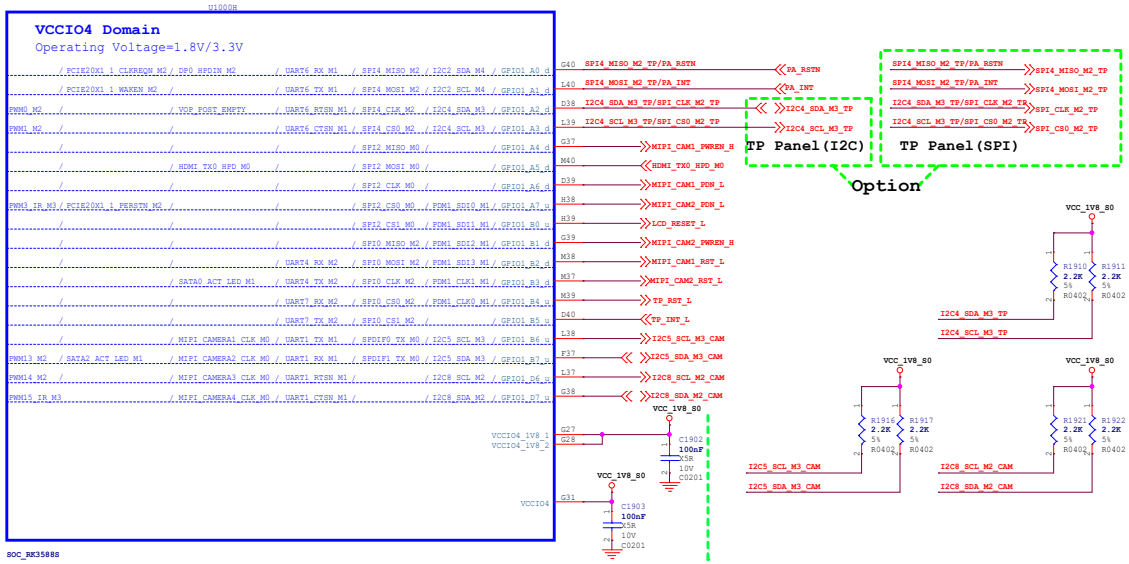
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PCIe2.0 PHY

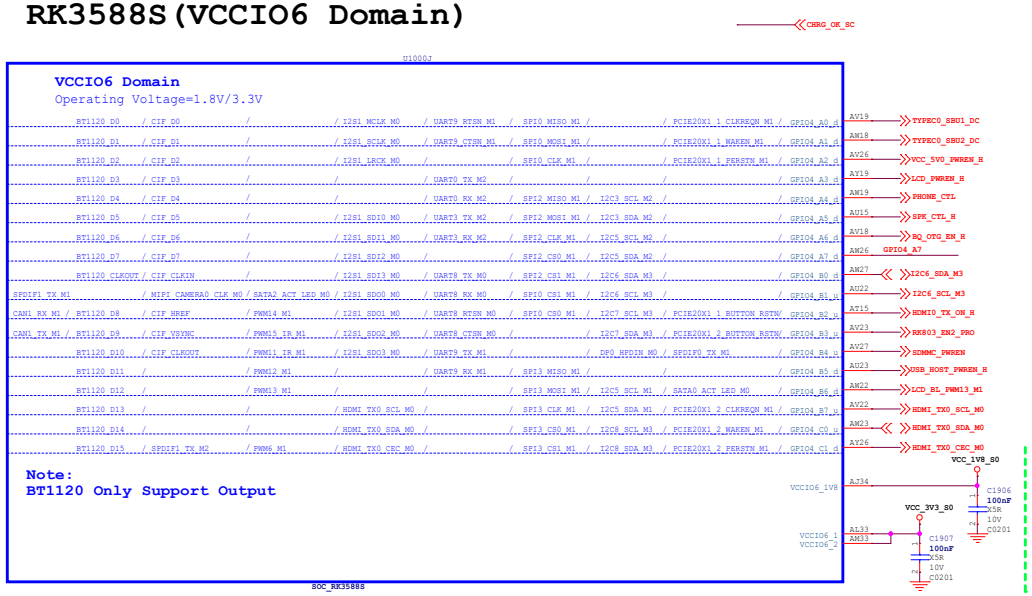
Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	18.RK3588S PCIE2/SATA3/USB3 PHY				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	18 of 54

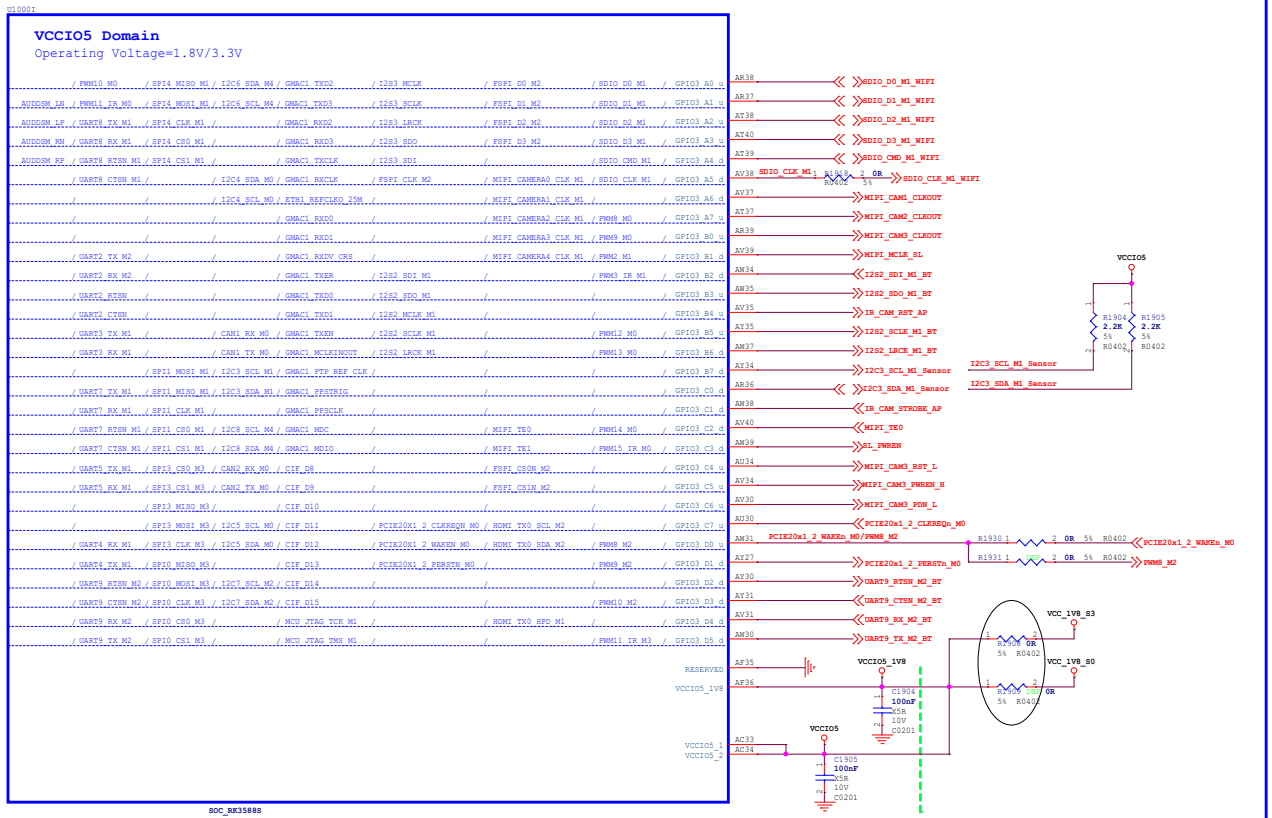
RK3588S(VCCIO4 Domain)

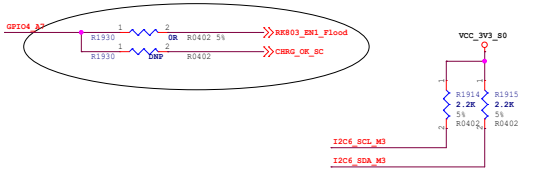


RK3588S(VCCIO6 Domain)



RK3588S(VCCIO5 Domain)





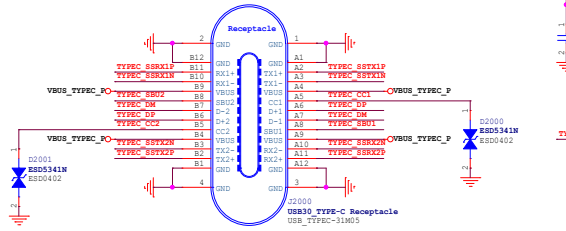
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

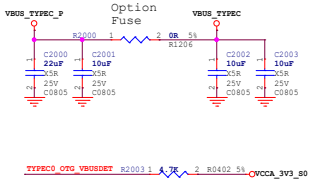
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588S_Tablet_REF		
File:	19.RK3588S 1.8V/3.3V GPIO		
Date:	Friday, November 04, 2022	Rev:	V12
Designed by: Joseph	Reviewed by: <Checker>	Sheet	19 of 54

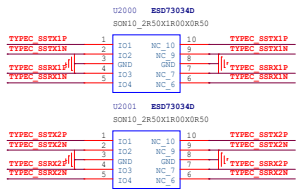
Power_1Cell_QC

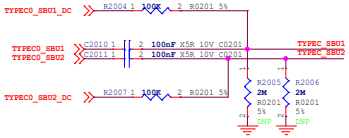
USB Type-C Port

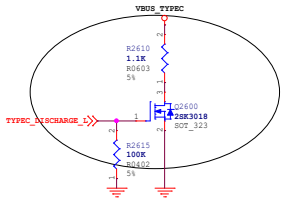




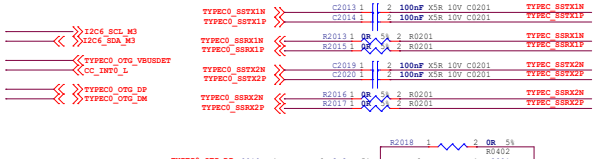
ESD

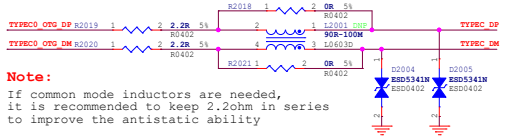




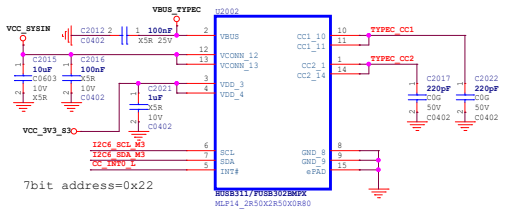


USB Type-C Controller(PD)





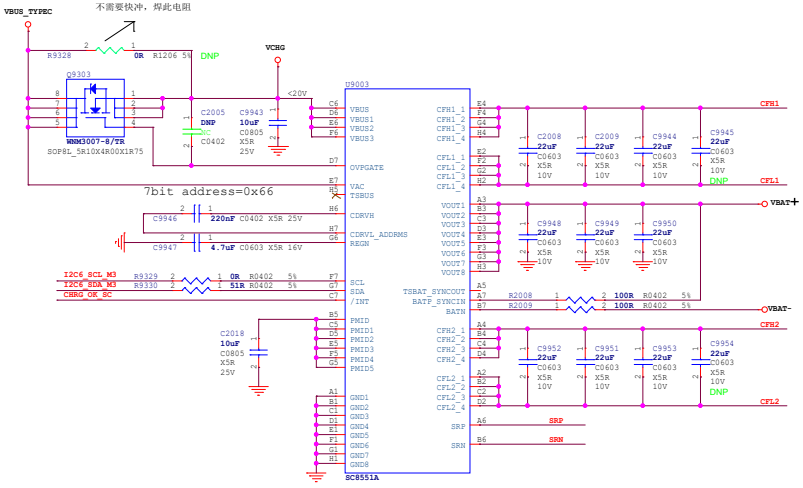
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability



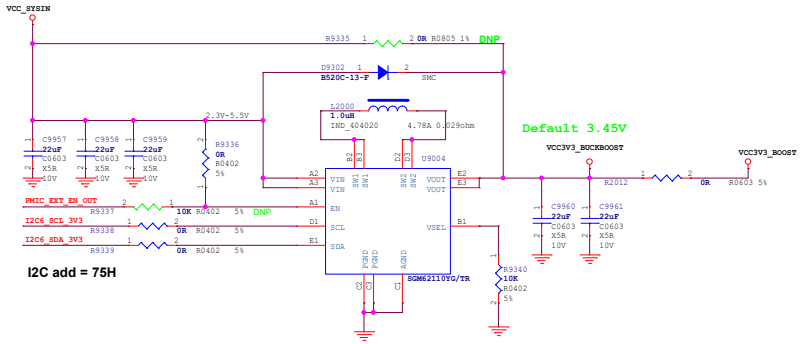
7bit address=0x22

VBUS of FUSB302BMPX: 4 to 21 TYP = 5V
VDD of FUSB302BMPX: 3 to 5.5 TYP = 3.3V
VCONN of FUSB302BMPX: 3 to 5.5

CP QUICK CHARGE(20W/45W)



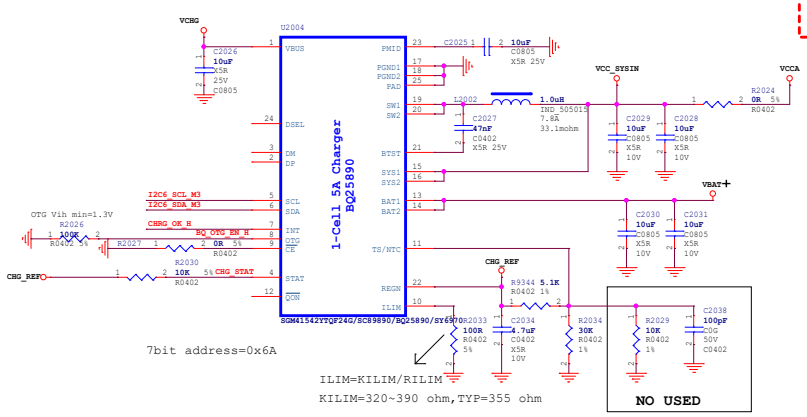
3.3V BUCK-BOOST

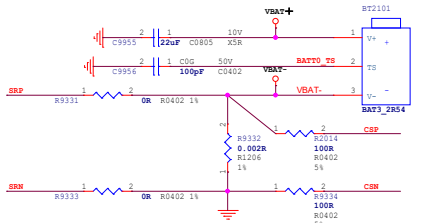


I2C add = 75H

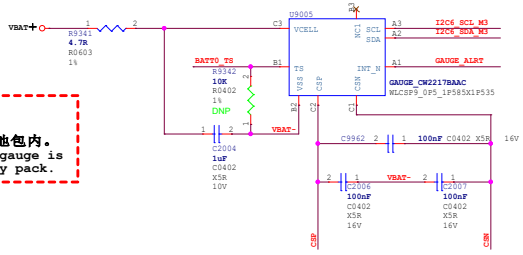
Charger IC

Note:
电池内阻小于80mR,满充电压4.4V，电池在3.6V—4.4V时最大充电电流10A。
The internal resistance of battery is less than 80mR, The maxium charging current no more than 10A during the battery voltage is 3.6V-4.4V and the full charge voltage is 4.4V.



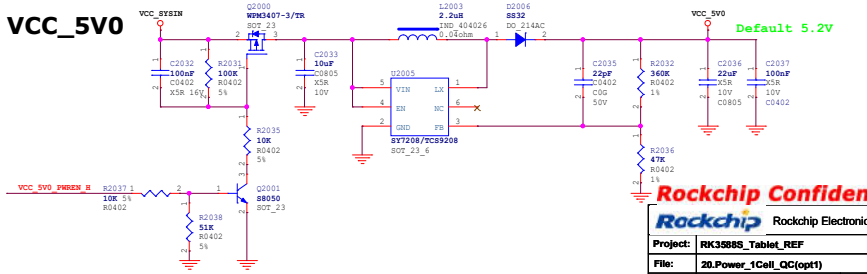


Gas Gauge

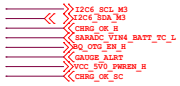


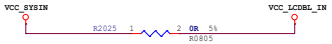
Note:
电量计建议放在电池包内。
Suggest the fuel gauge is built in the battery pack.

VCC_5V0



LCD Backlight power input source





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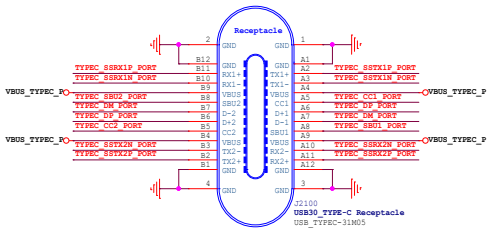
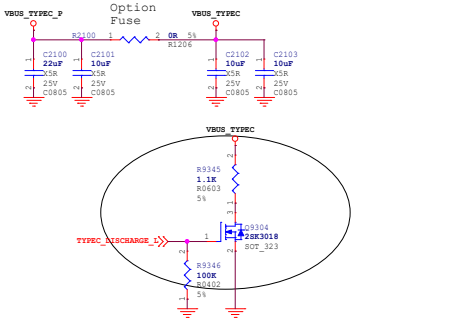
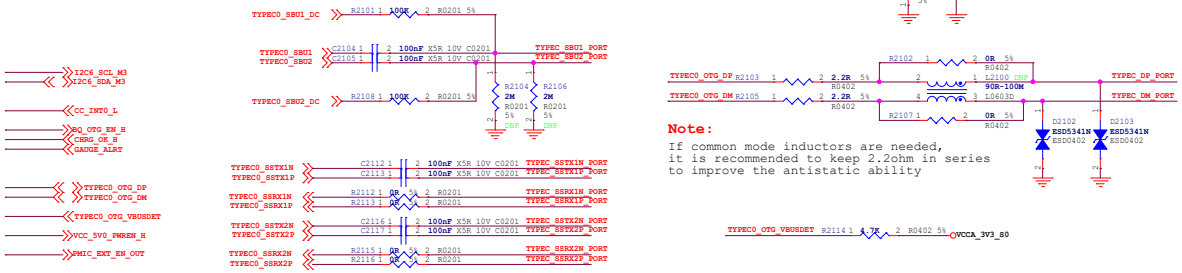
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Tablet_REF
File:	20.Power_1Cell_QC(opt1)
Date:	Friday, November 11, 2022
Rev:	V12
Designed by:	Joseph
Reviewed by:	Default
Sheet	20 of 54

Power_2Cell_QC

USB Type-C Port

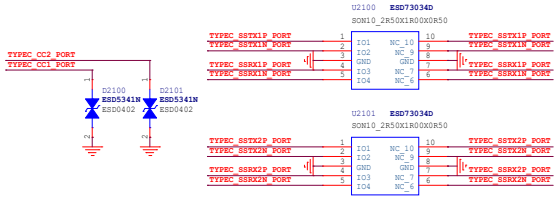




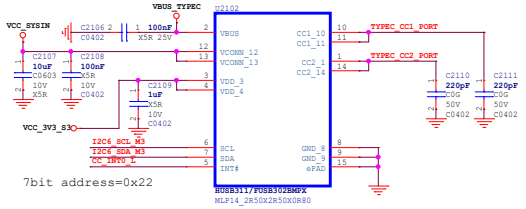


Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability

ESD



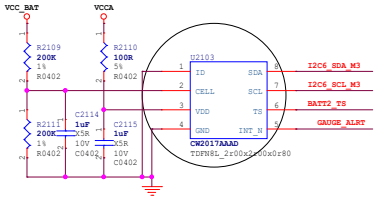
USB Type-C Controller(PD)



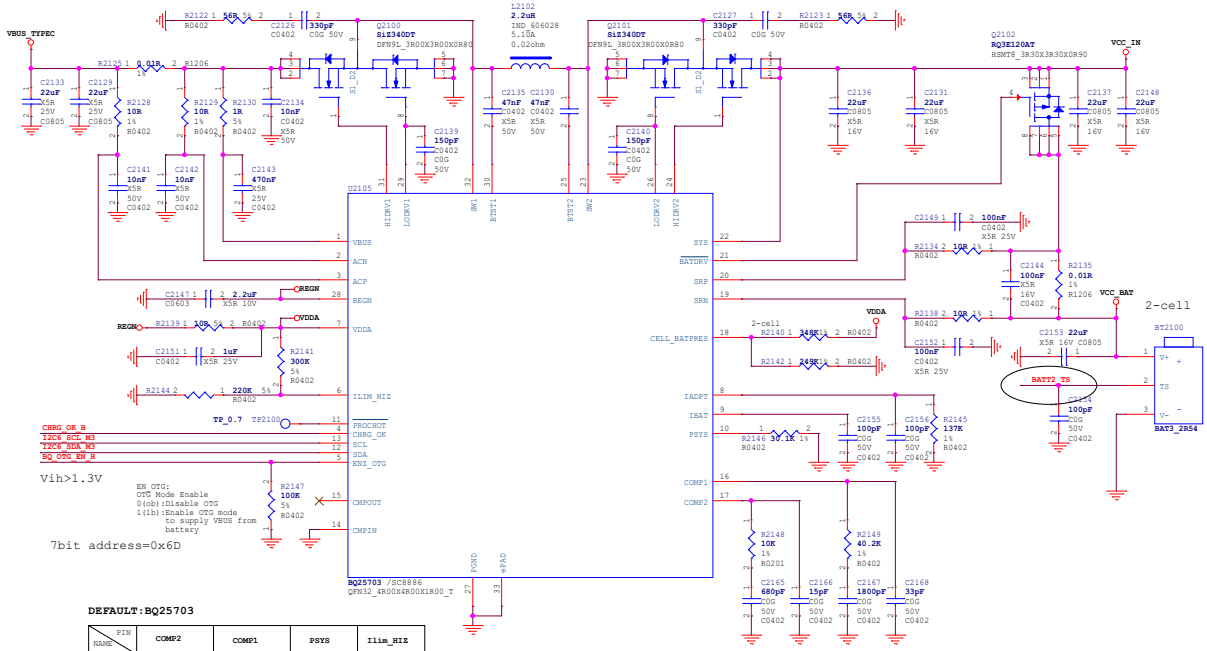
7bit address=0x22

VBUS of FUSB302BMPX: 4 to 21 TYP = 5V
VDD of FUSB302BMPX: 3 to 5.5 TYP = 3.3V
VCONN of FUSB302BMPX: 3 to 5.5

Gas Gauge



Charger IC



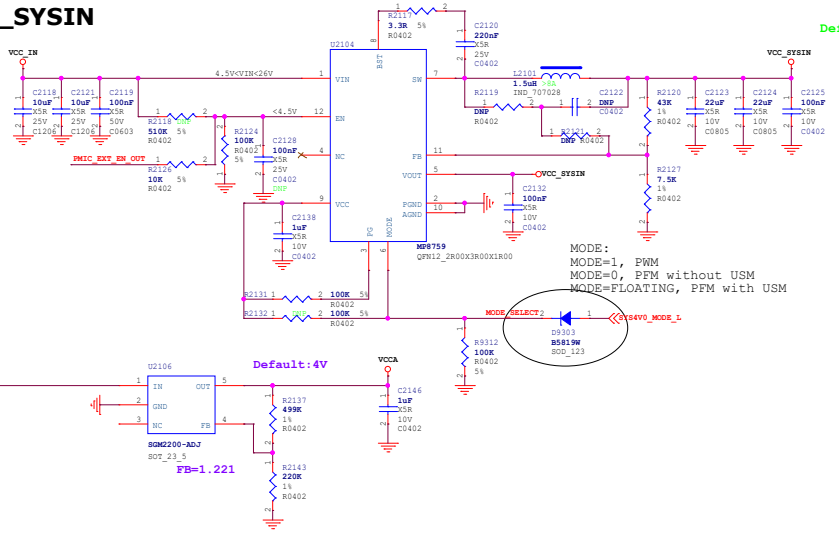
EN_OTG:
OTG Mode Enable
0(ob):Disable OTG
1(ib):Enable OTG mode
to supply VBUS from
battery

DEFAULT:BQ25703

PIN / NAME	COMP2	COMP1	PSYS	Ilim_HIZ
BQ25703	R2148=10K C2165=680pf C2166=15pf	R2149=40.2K C2167=1800pf C2168=33pf	R2146=30.1K	R2144=220K
SC8886	R2148=330K C2165=inf C2166=220pf	R2149=100K C2167=inf C2168=10pf	R2146=33K	R2144=160K

VCC_SYSIN

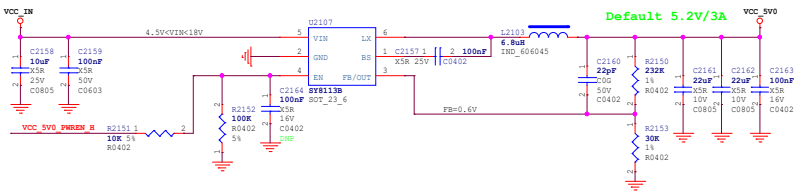
Default 4.0V



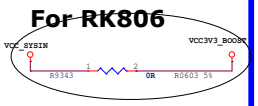
MODE:
MODE=1, PWM
MODE=0, PFM without USM
MODE=FLOATING, PFM with USM

VCC_5V0

Default 5.2V/3A



For RK806



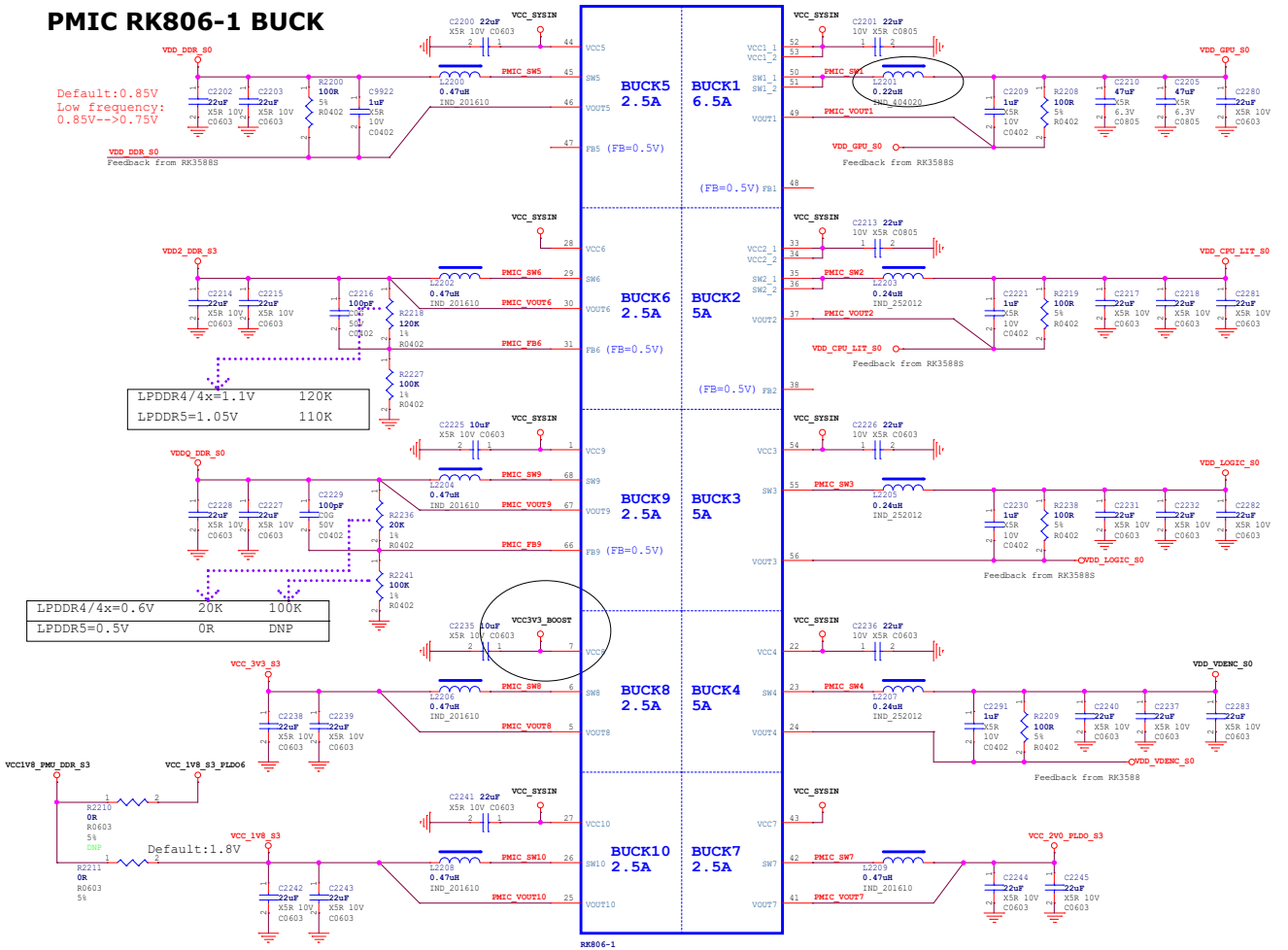
LCD Backlight power input source

Rockchip Confidential

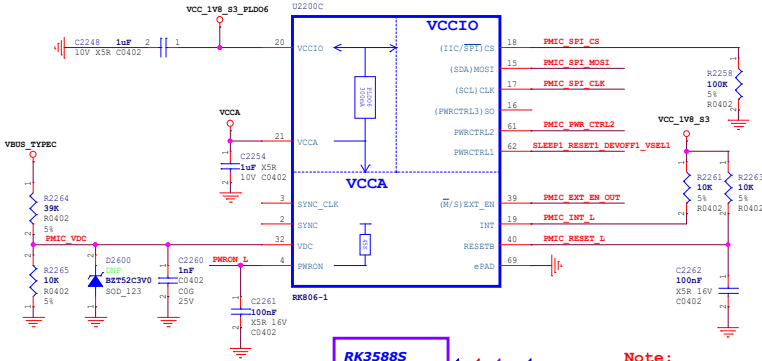
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Tablet_REF
File:	21.Power_2Cell_QC(opt2)
Date:	Friday, November 04, 2022
Rev:	V12
Designed by:	Joseph
Reviewed by:	Default
Sheet	21 of 54

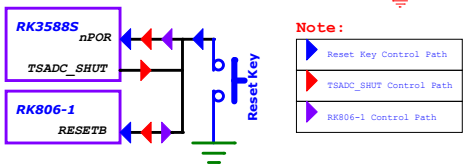
PMIC1 RK806-1

PMIC RK806-1 BUCK



PMIC RK806-1 Managerment

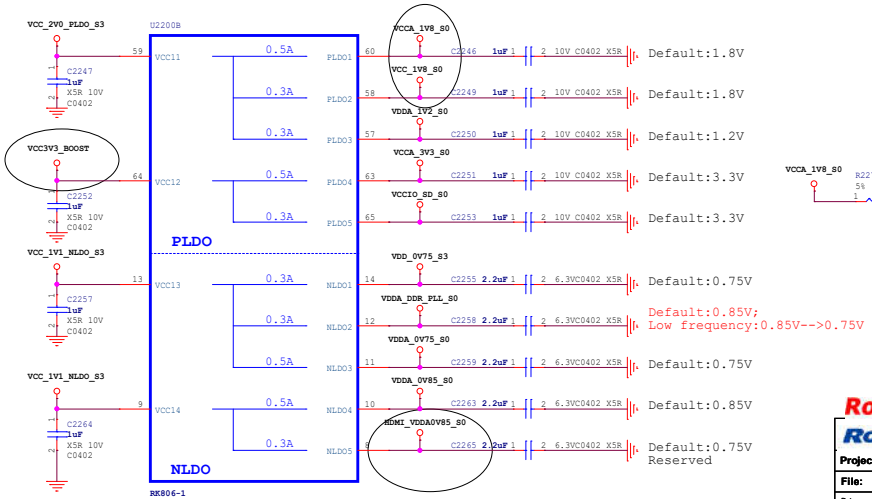




Note:

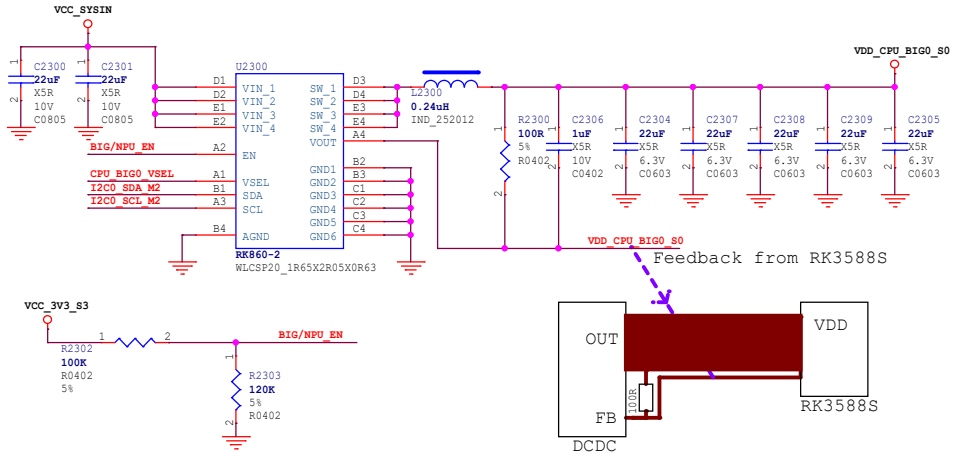
Reset Key Control Path
TSADC_SHUT Control Path
RK806-1 Control Path

PMIC RK806-1 LDO

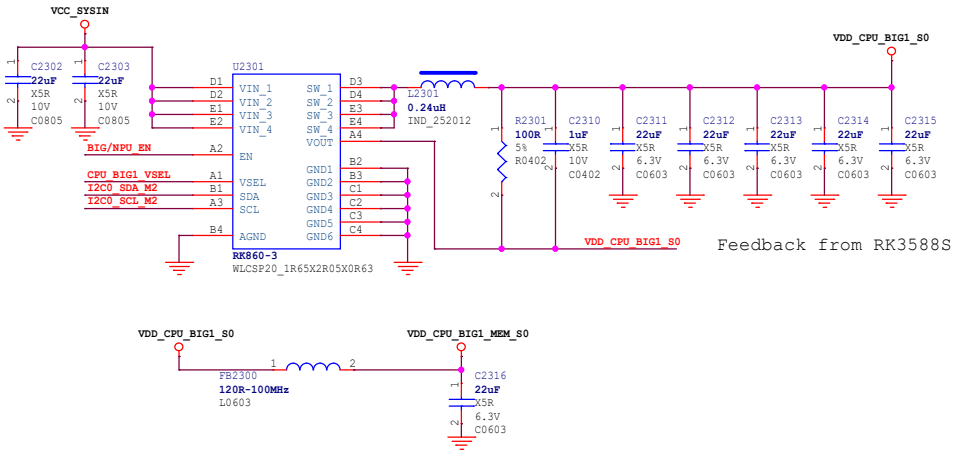


Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588S_Tablet_REF		
File:	22.Power-PMIC_RK806-1		
Date:	Friday, November 04, 2022	Rev:	V12
Designed by:	Joseph	Reviewed by: <Checker>	Sheet: 22 of 54

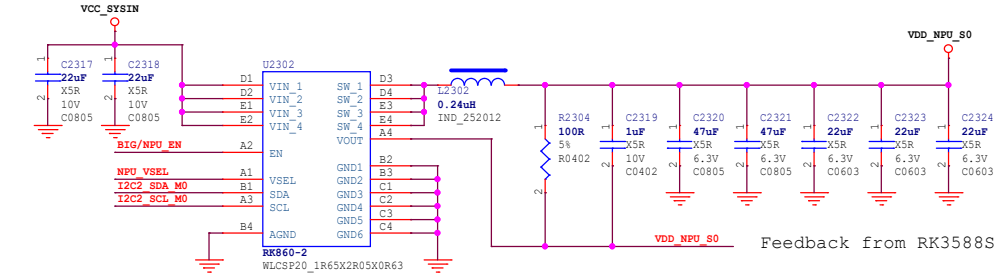
VDD_CPU_BIG0



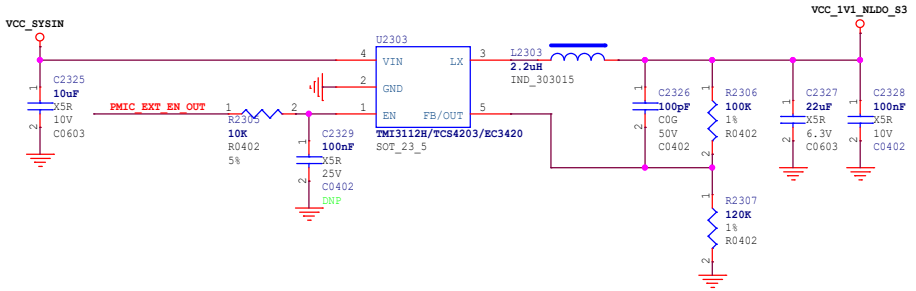
VDD_CPU_BIG1



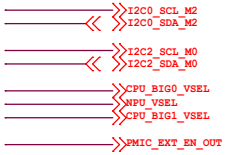
VDD_NPU

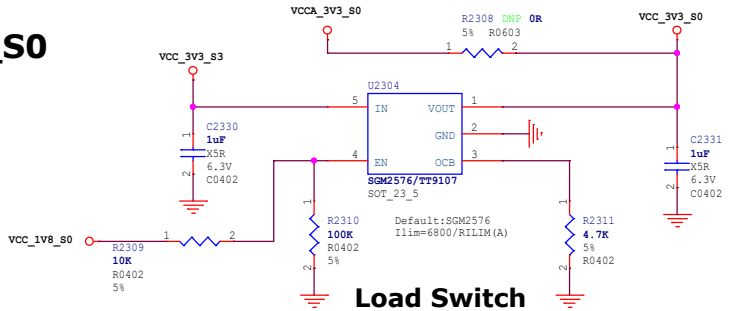


VCC_1V1_NLDO



VCC_3V3_S0



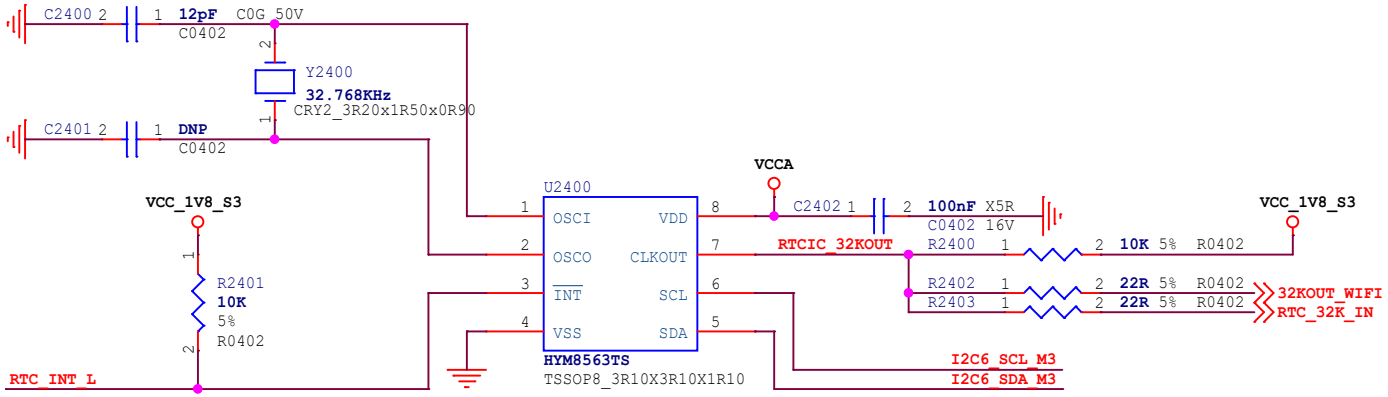


Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	23.Power_Ext Discrete				
Date:	Friday, November 04, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	23 of 54

RTC IC

I2C6_SDA_M3
I2C6_SCL_M3
RTC_INT_L

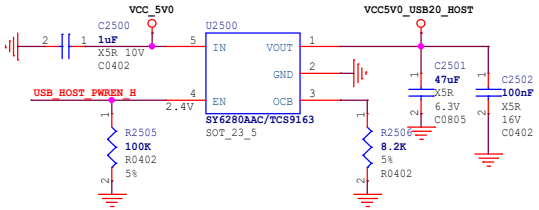


Address:Read A3H,Write A2H

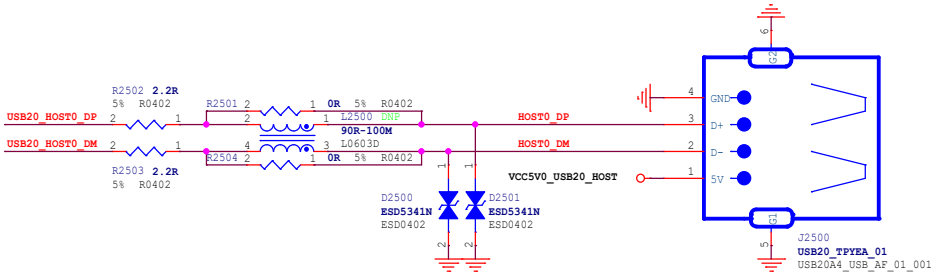
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	24.RTC				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	24 of 54

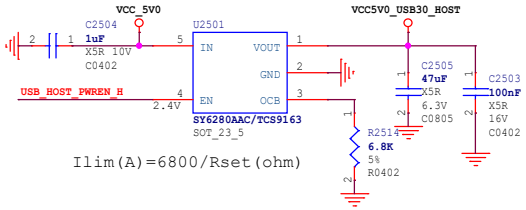
USB2.0 HOST



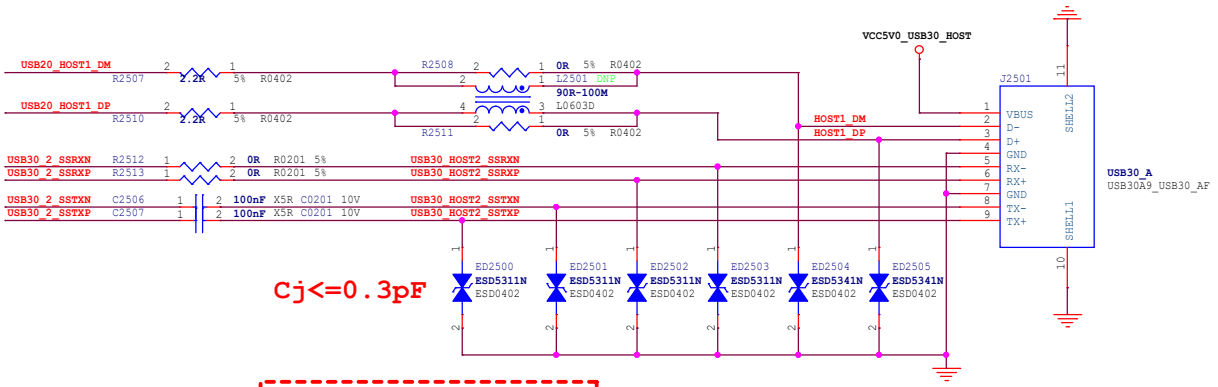
Ilim(A)=6800/Rset(ohm)



USB3.0 HOST



Ilim(A)=6800/Rset(ohm)

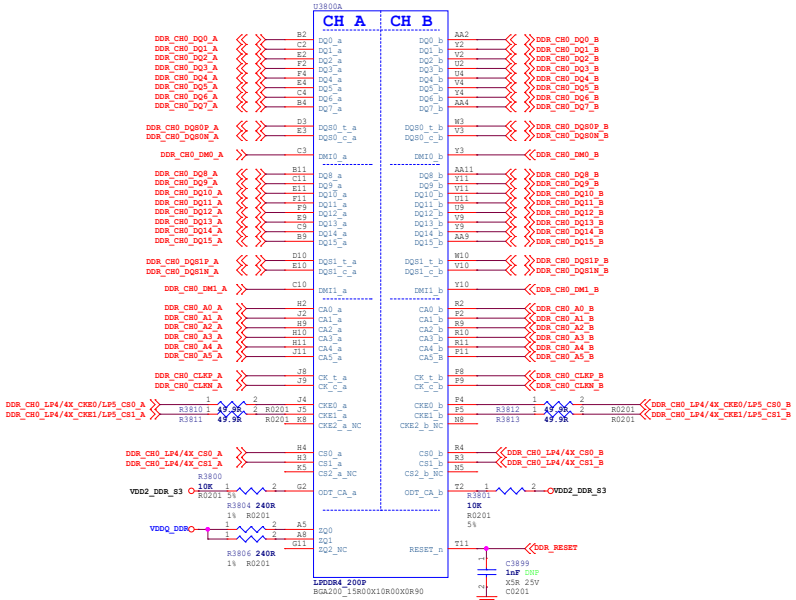


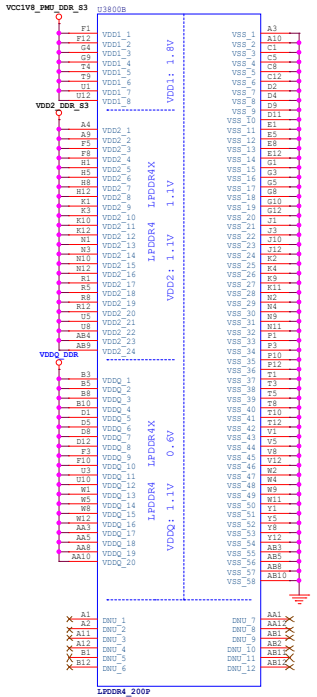
Cj<=0.3pF

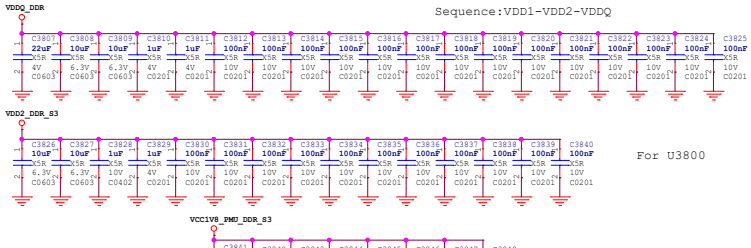
Note:
The Cj of ESD must <=0.3pf

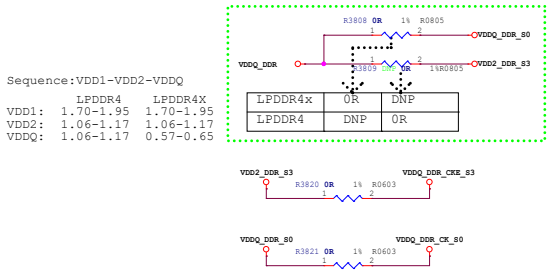
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	25.USB20/USB30 HOST Port				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	25 of 54

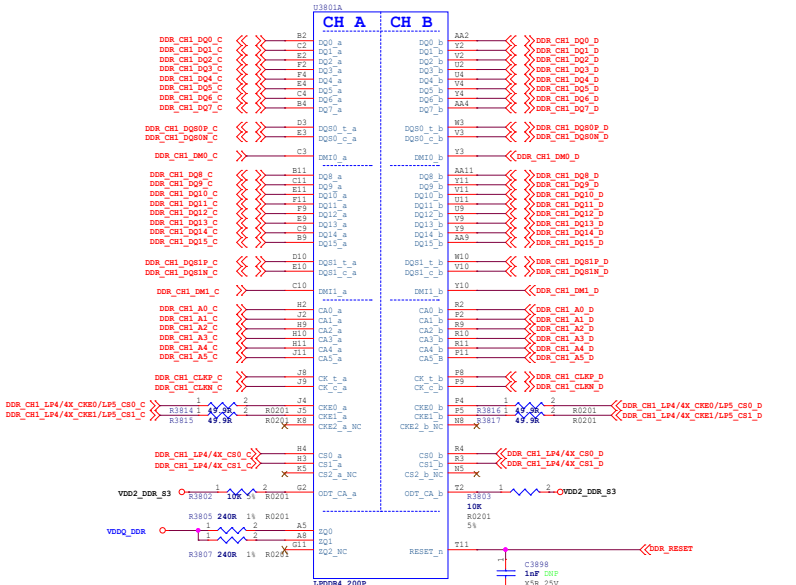
DRAM-LPDDR4/4x_2X32bit

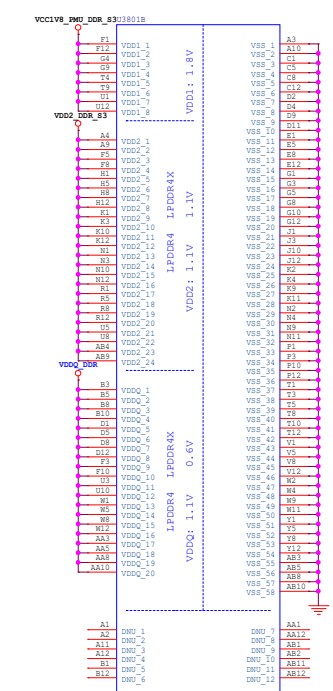


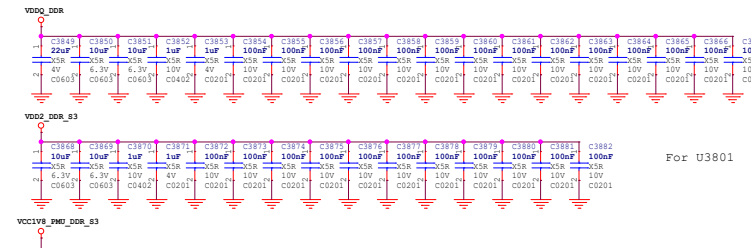








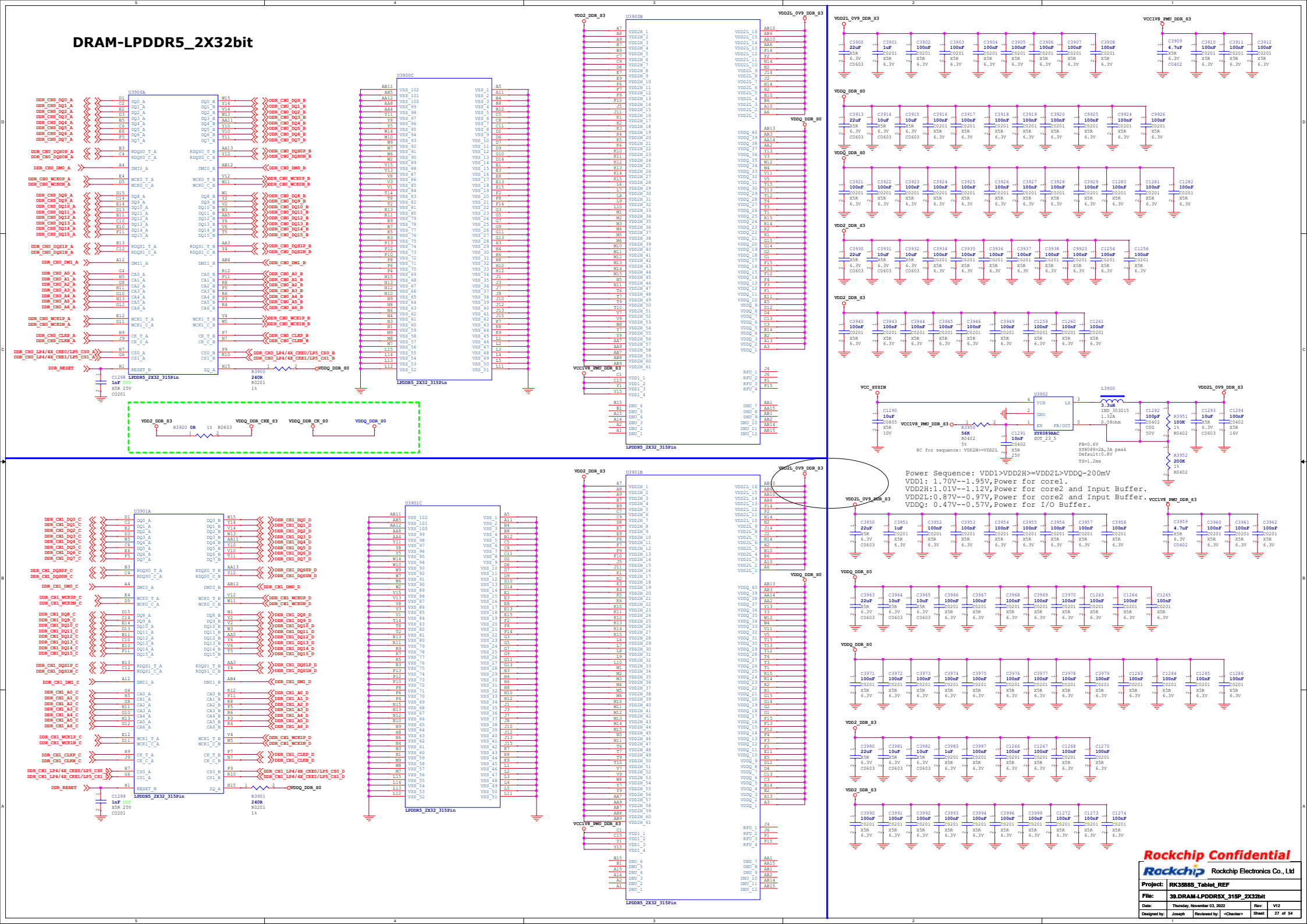




Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588S_Tablet_REF		
File:	38.DRAM-LPDDR4/4X_200P_2X32bit		
Date:	Thursday, November 03, 2022	Rev:	V12
Designed by: Joseph	Reviewed by: <Checker>	Sheet	26 of 54

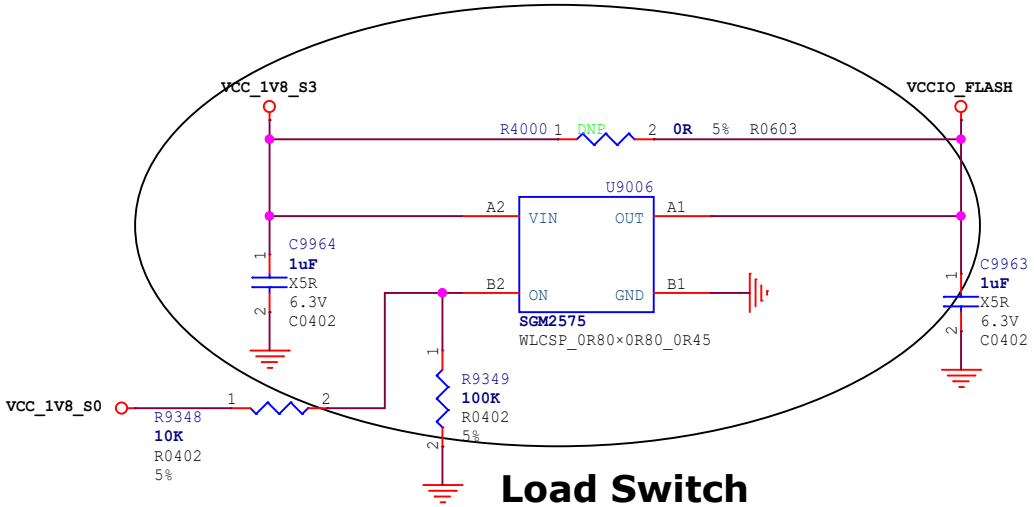
DRAM-LPDDR5_2X32bit



Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588S_Tablet_REF		
File:	39.DRAM-LPDDR5X_315P_2X32bit		
Date:	Thursday, November 03, 2022	Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>
		Sheet	27 of 54

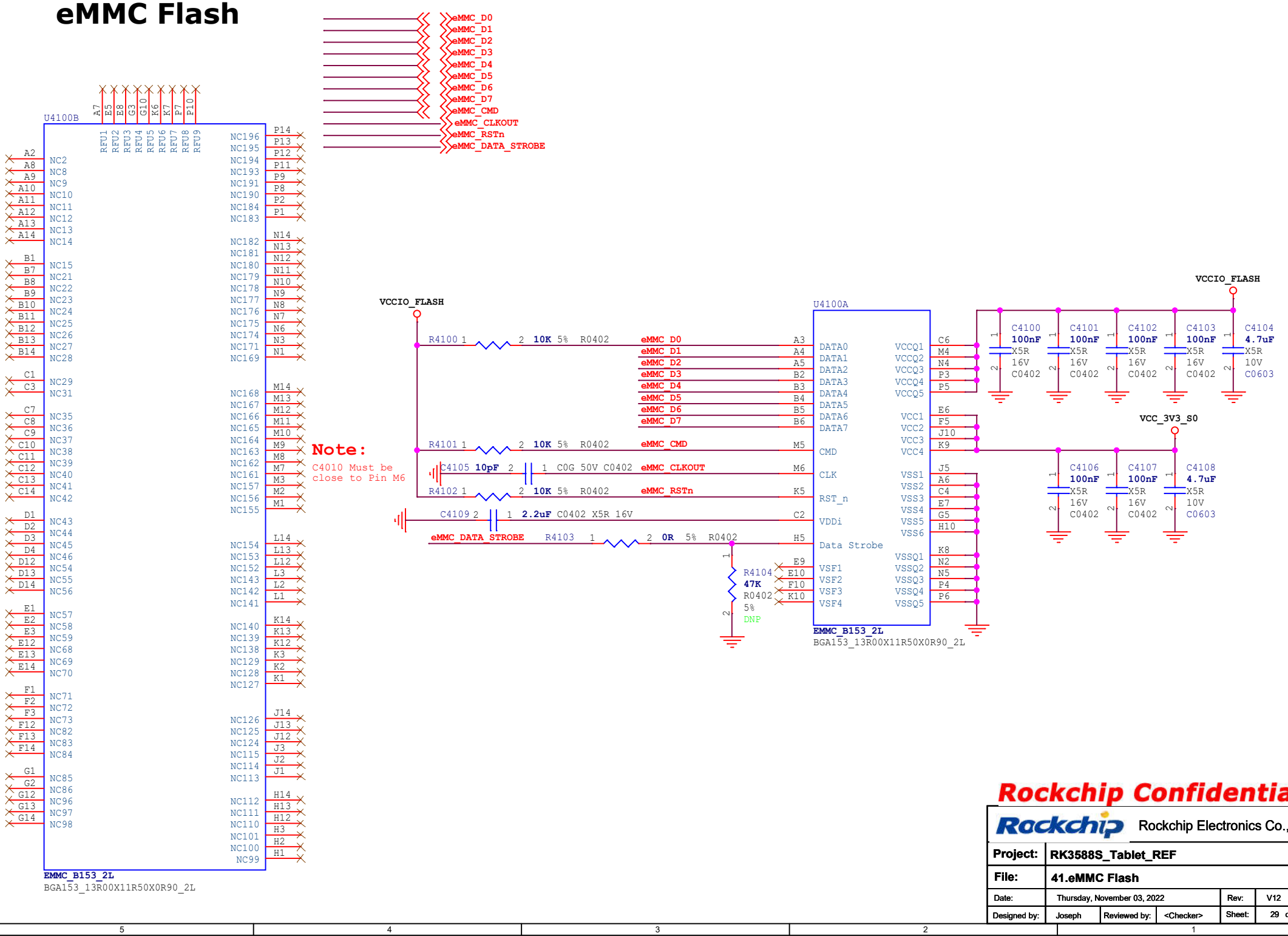
Flash Power



Load Switch

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	40.Flash Power				
Date:	Friday, November 04, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	28 of 54

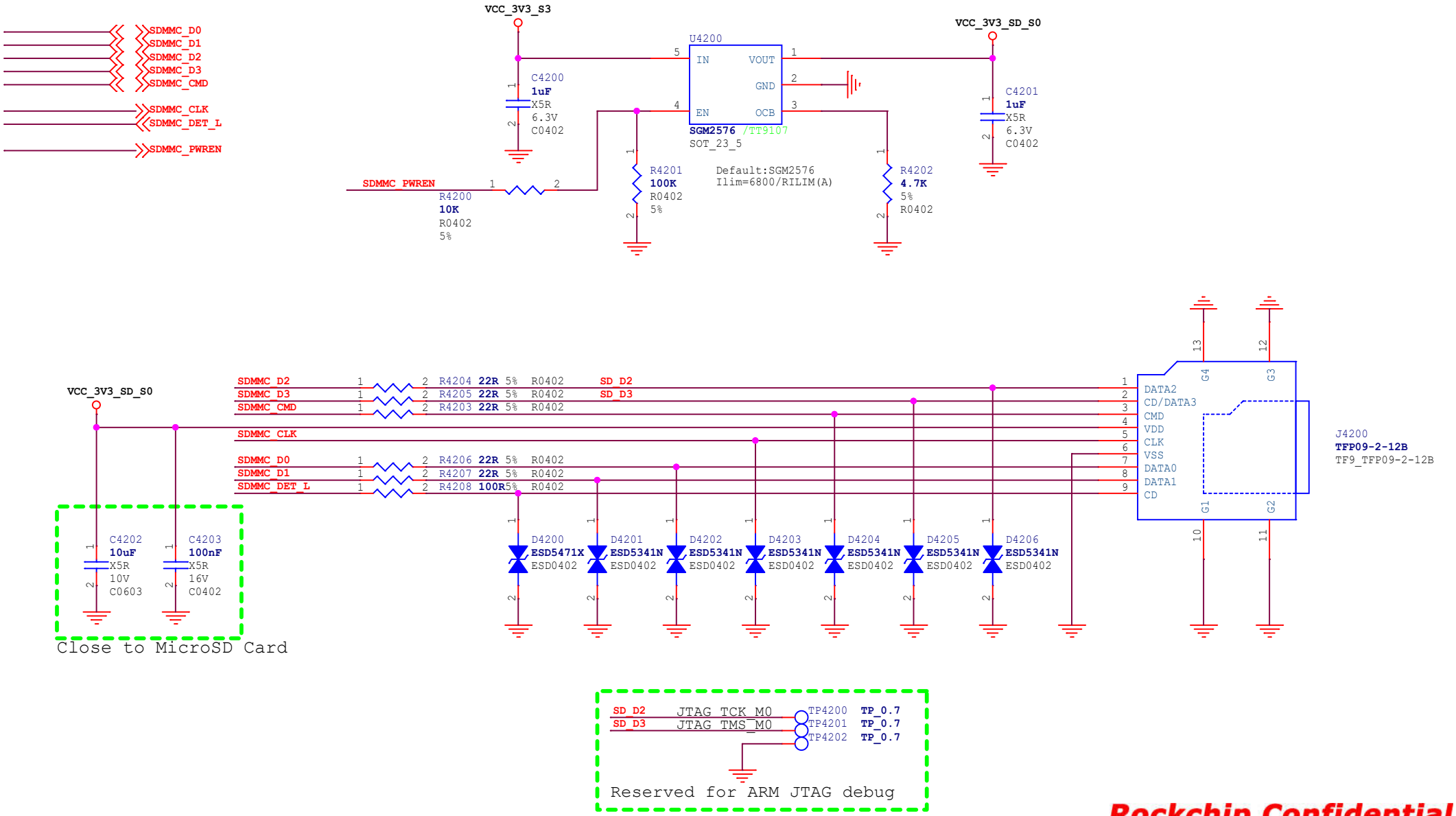
eMMC Flash



Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	41.eMMC Flash				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	29 of 54

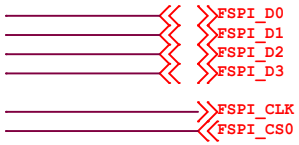
MicroSD Card

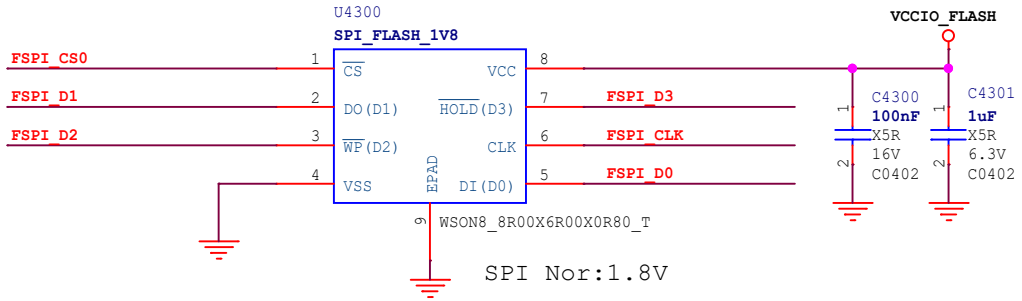


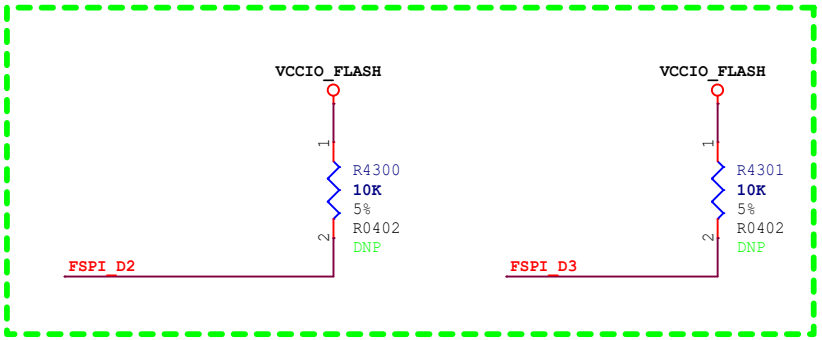
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	42.Flash-Micro-SD Card				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	30 of 54

SPI FLASH





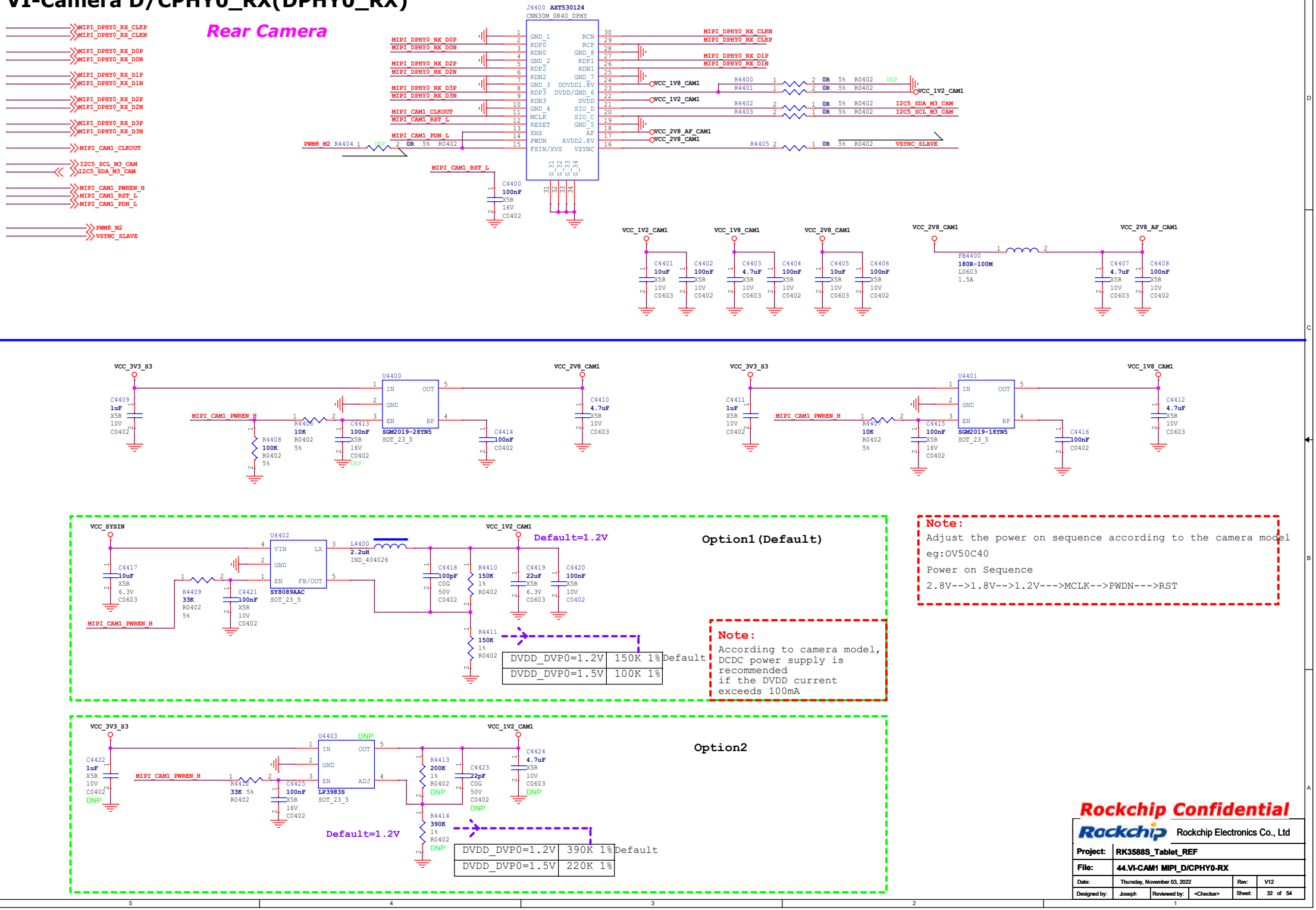


Note:
When using SPI FLASH with only 1 bit, it needs to be stuffed.

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	43.Flash-SPI FLASH(opt)				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	31 of 54

VI-Camera D/CPHY0_RX(DPHY0_RX)

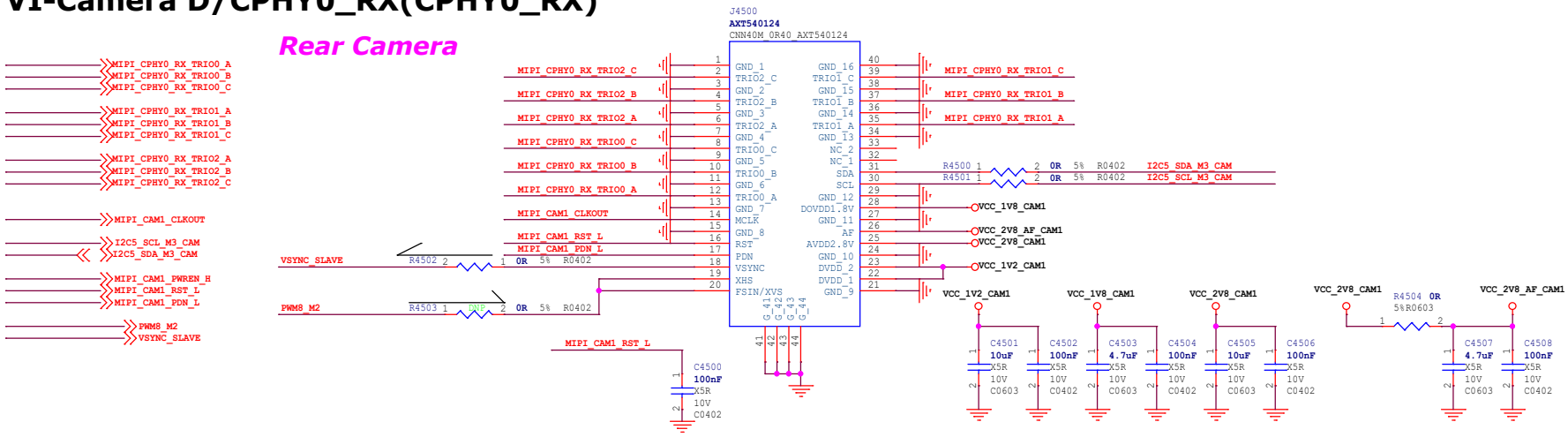


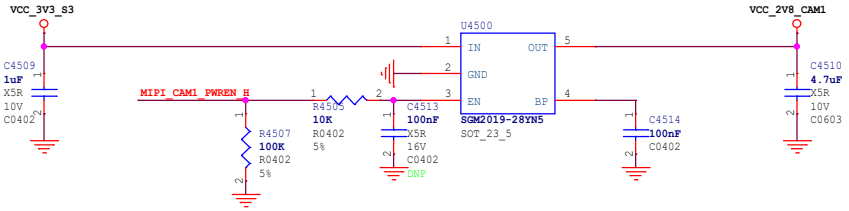
Rockchip Confidential

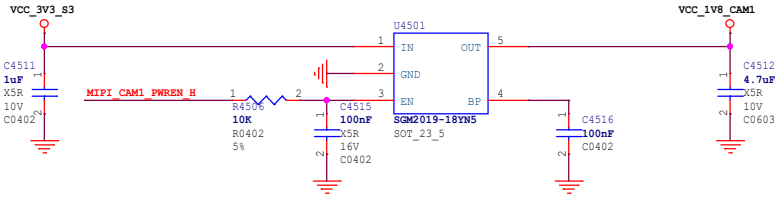
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	44.VI-CAM1 MIPI_D/CPHY0-RX				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	32 of 54

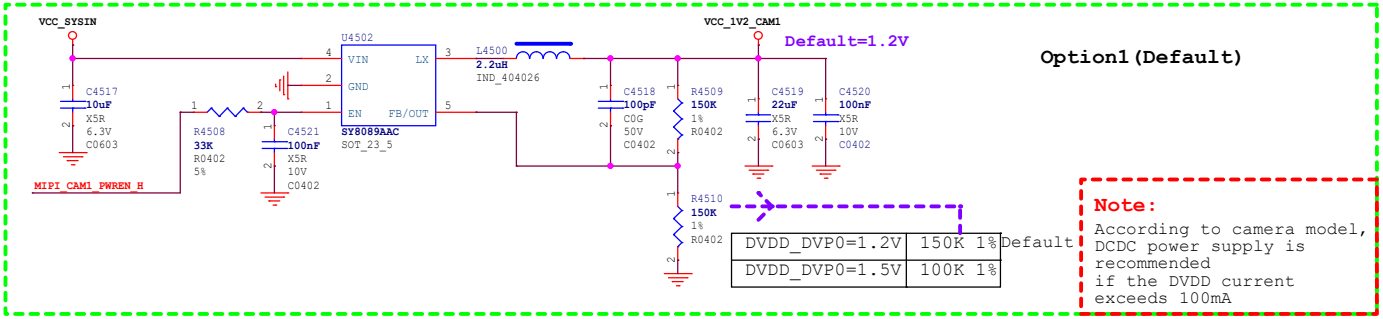
VI-Camera D/CPHY0_RX(CPHY0_RX)

Rear Camera



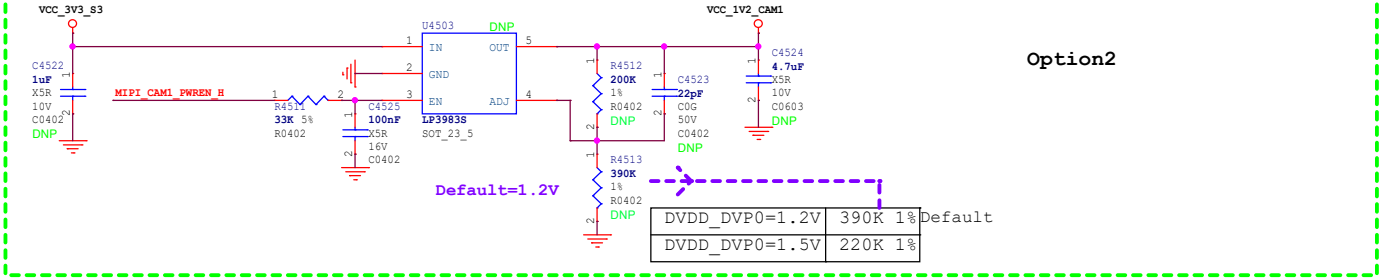






Note:
According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA

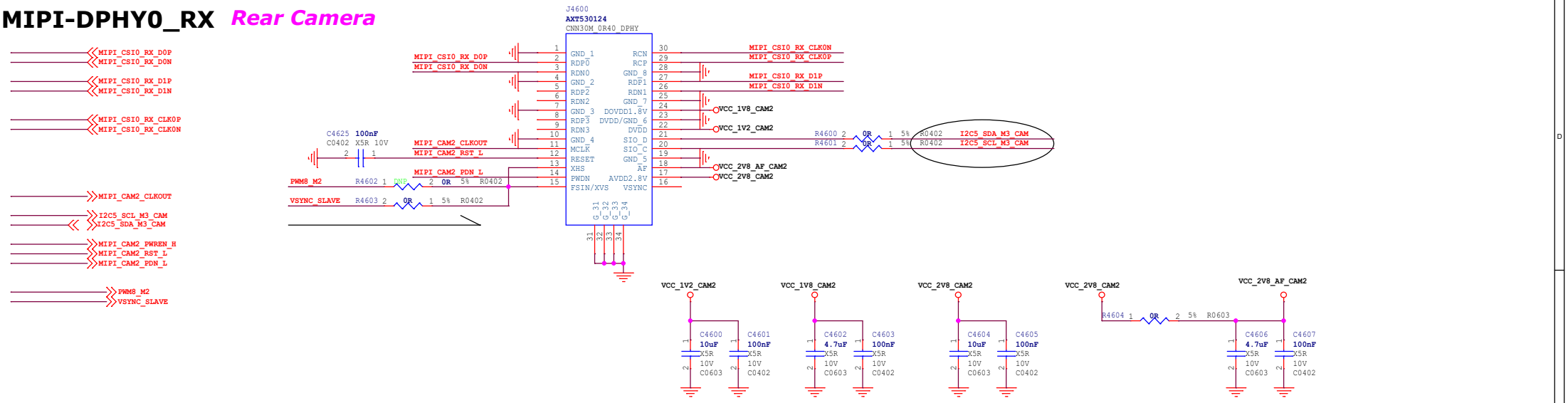
Note:
Adjust the power on sequence according to the camera model
eg:OV50C40
Power on Sequence
2.8V-->1.8V-->1.2V--->MCLK-->PWDN--->RST

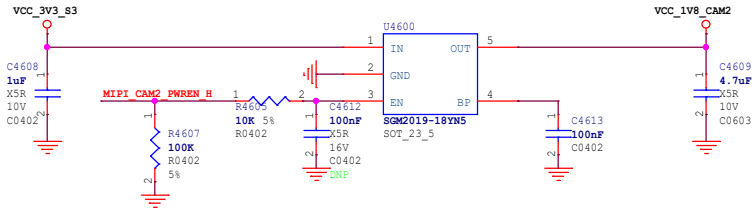


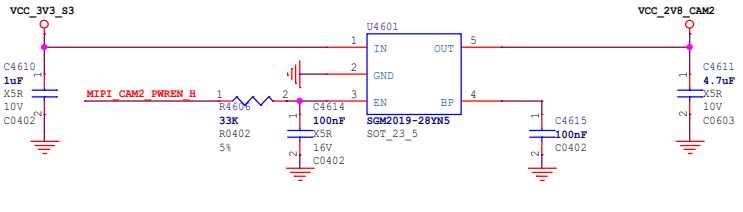
Rockchip Confidential

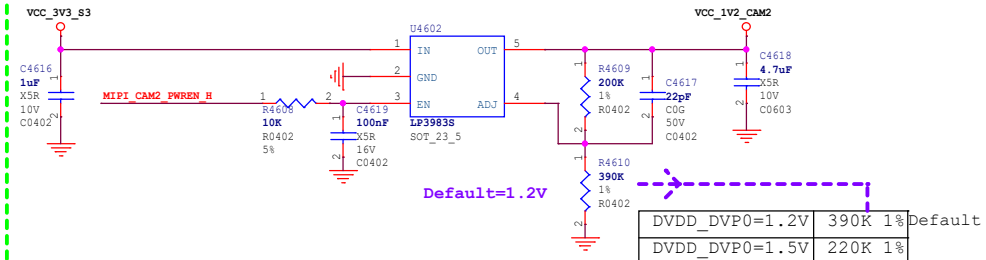
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	45.VI-CAM1 MIPI_D/CPHY0-RX(opt)				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	33 of 54

MIPI-DPHY0_RX *Rear Camera*



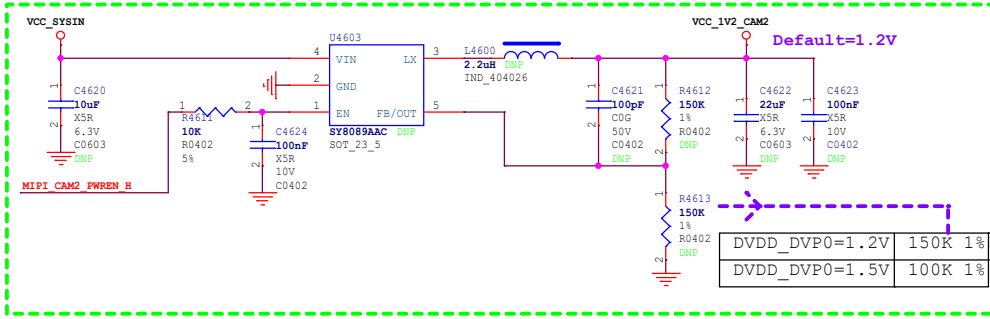






Option1 (Default)

Note:
According to camera model, DCDC power supply is recommended if the DVDD current Below 100mA



Option2

Note:
Adjust the power on sequence according to the camera model
eg:GC8034
Power on Sequence
1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST

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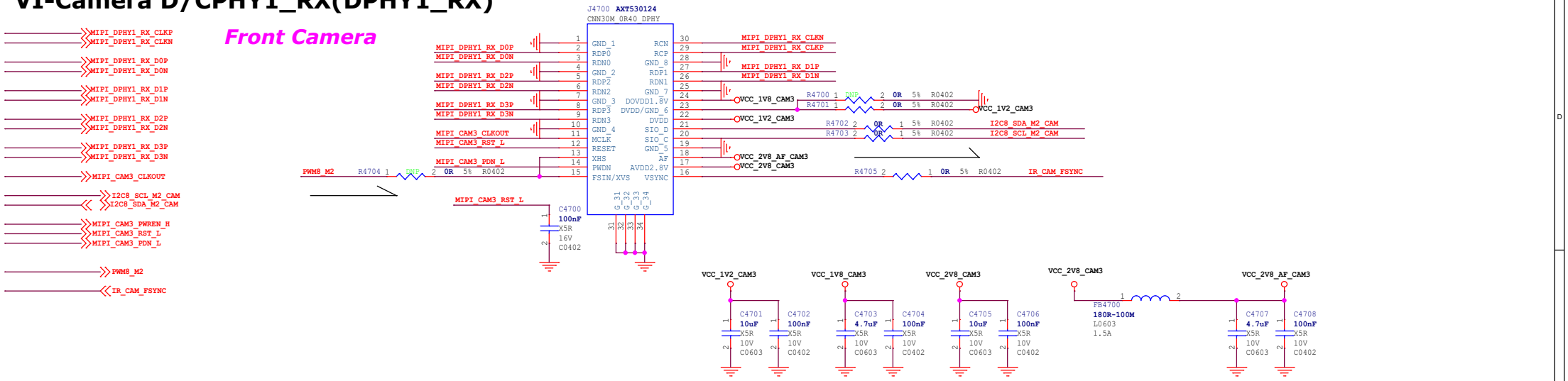
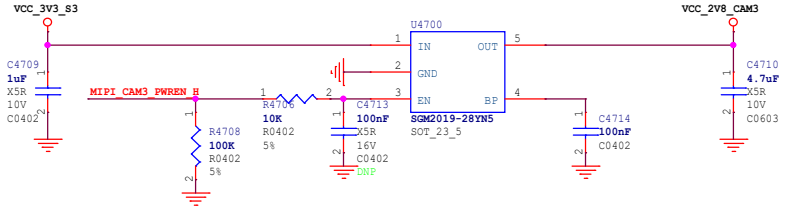
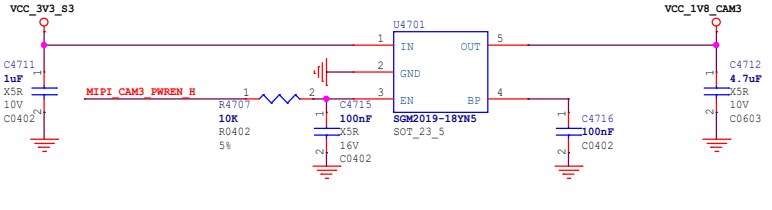
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	46.VI-CAM2 MIPI_DPHY0-RX				
Date:	Friday, November 04, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	34 of 54

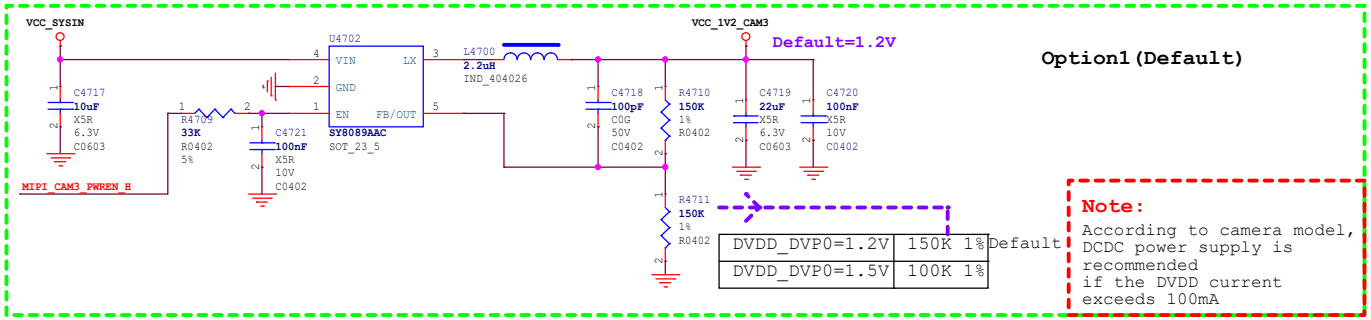
VI-Camera D/CPHY1_RX(DPHY1_RX)

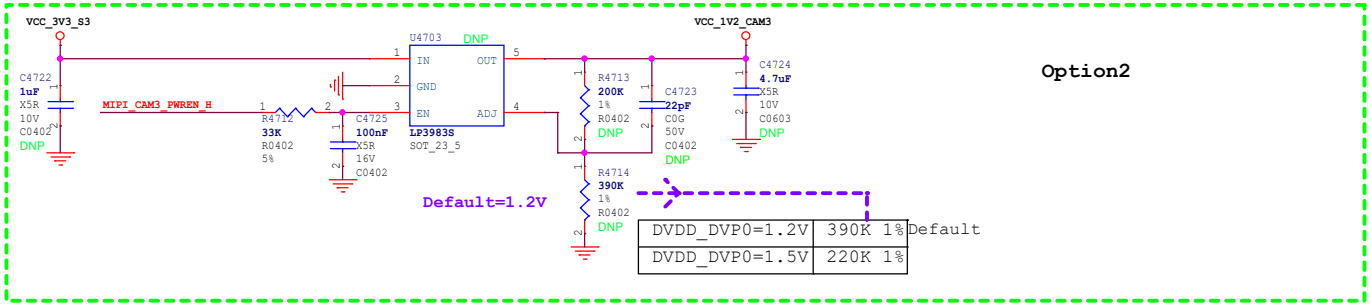
Front Camera









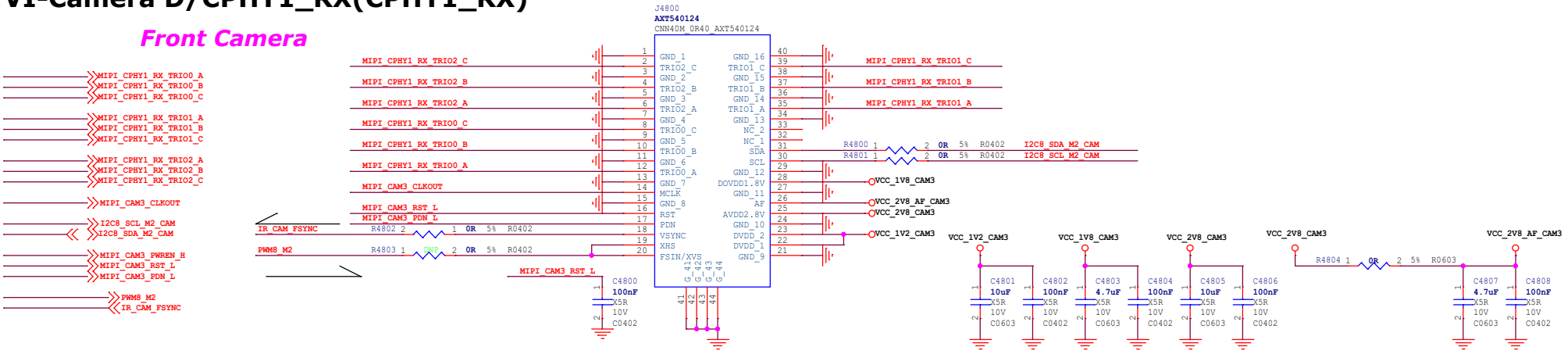


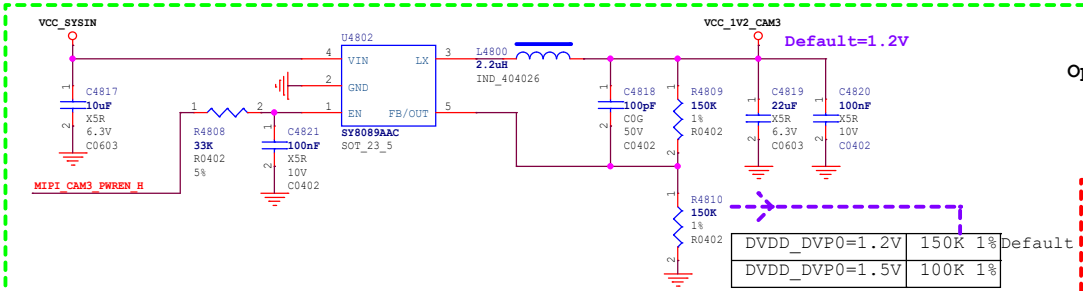
Note:
Adjust the power on sequence according to the camera model
eg:OV50C40
Power on Sequence
2.8V-->1.8V-->1.2V--->MCLK-->PWDN--->RST

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	47.VI-CAM3 MIPI_D/CPHY1-RX				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	35 of 54

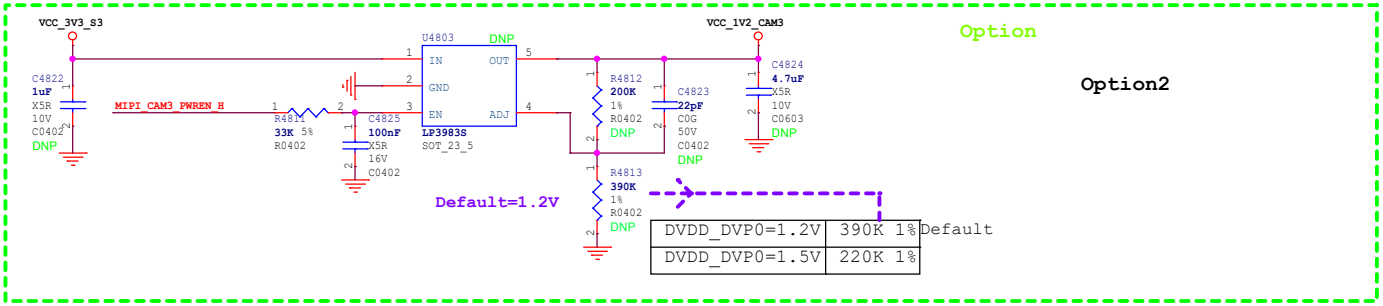
VI-Camera D/CPHY1_RX(CPHY1_RX)

Front Camera





Note:
According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA



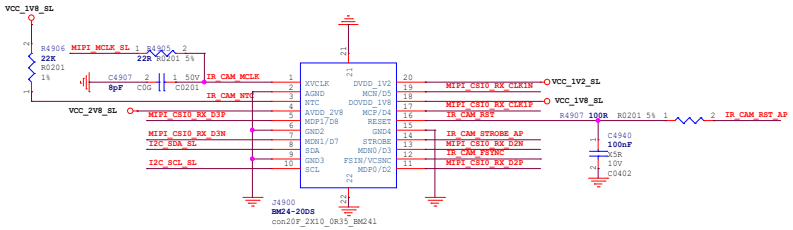
Note:
Adjust the power on sequence according to the camera model
eg:OV50C40
Power on Sequence
2.8V-->1.8V-->1.2V--->MCLK-->PWDN--->RST

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	48.VI-CAM3 MIPI_D/CPHY1-RX(opt)				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	36 of 54

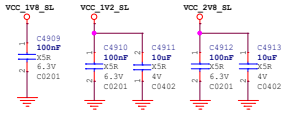
MIPI SL(Structured light) Module (DPHY0_RX) *Front Camera*

MIPI_CSI0_RX_CLK1P
MIPI_CSI0_RX_CLK1N
MIPI_CSI0_RX_D2P
MIPI_CSI0_RX_D2N
MIPI_CSI0_RX_D3P
MIPI_CSI0_RX_D3N
MIPI_MCLK_SL
I2C8_SCL_M2_CAM
I2C8_SDA_M2_CAM
RK803_EN2_PRO
RK803_EN1_Flood
SL_PWREN
IR_CAM_STROBE_AP
IR_CAM_RST_AP
IR_CAM_NTC
IR_PRO_NTC
IR_CAM_FSYNC

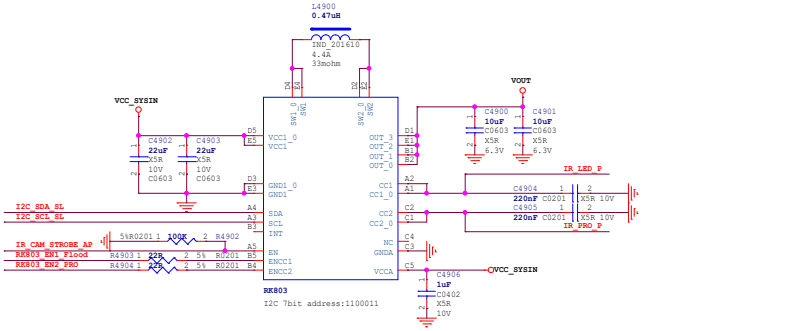
IR Camera



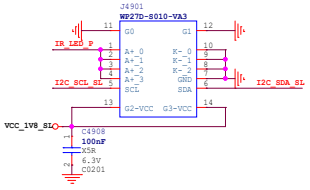
广濑母座BM24-20DS/2-0.35V(51)



Note:
IR SENSOR:OV9282
AVDD=2.8V
DVDD=1.2V
DOVDD=1.8V

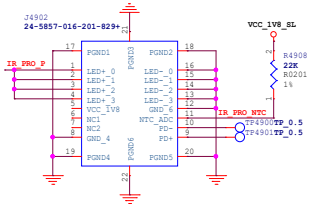


IR Flood

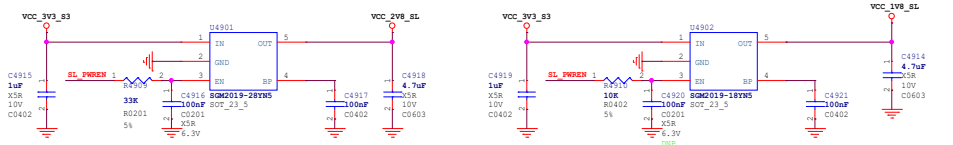


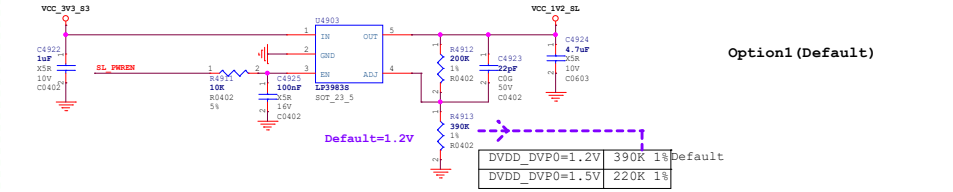
JAE母座WP27D-S010-VA3

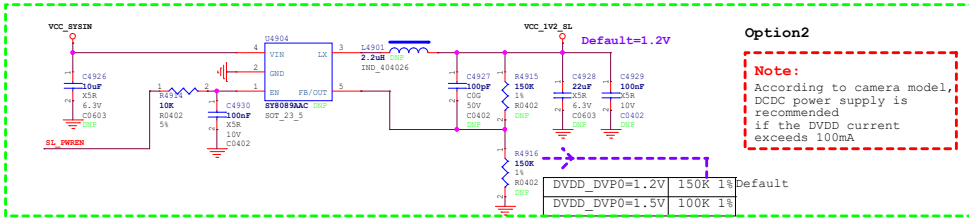
IR Projector



京瓷母座24-5857-016-201-829+



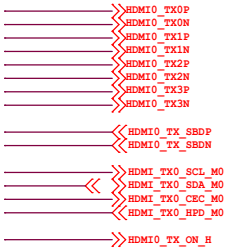


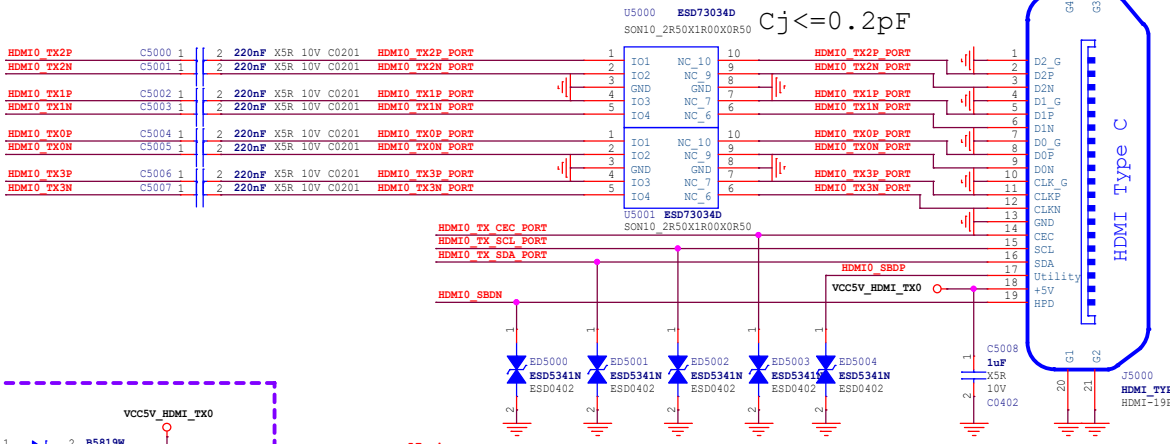


Note:
According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588S_Tablet_REF		
File:	49. VI-CAM4 SL Module		
Date:	Thursday, November 03, 2022	Rev:	V12
Designed by: Joseph	Reviewed by: <Checker>	Sheet	37 of 54

HDMI2.1 TX0

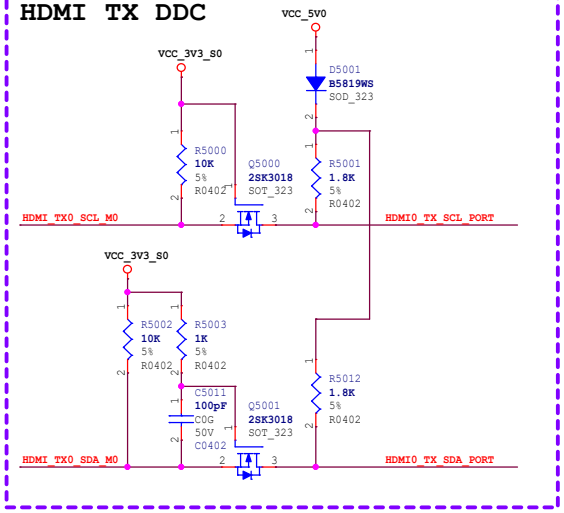


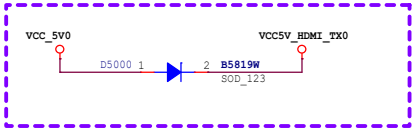


Note:

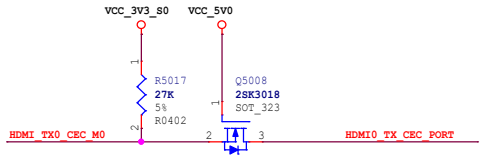
This reference circuit use TYPE C by default
If the project needs TYPE A, you must replace the library with TYPE A.

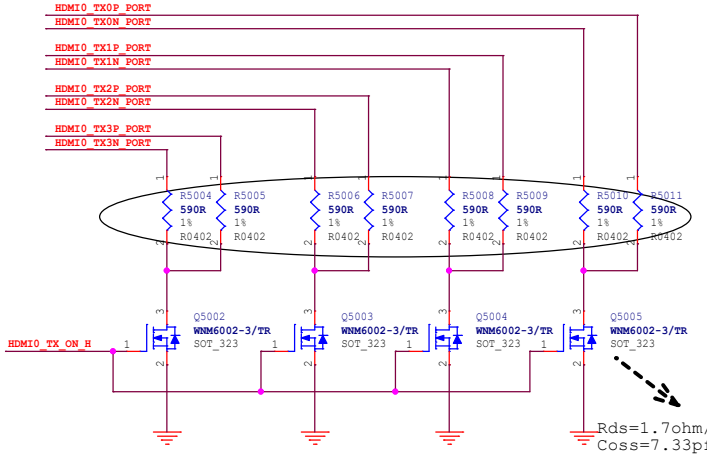
HDMI TX DDC





HDMI TX CEC

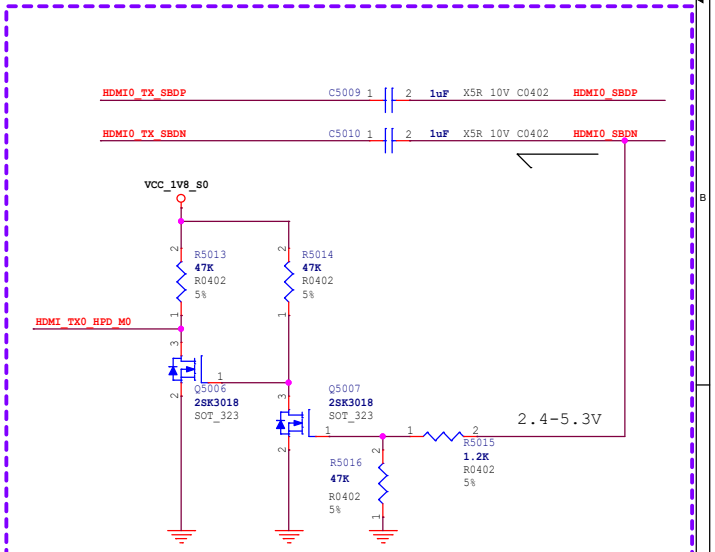




Note:

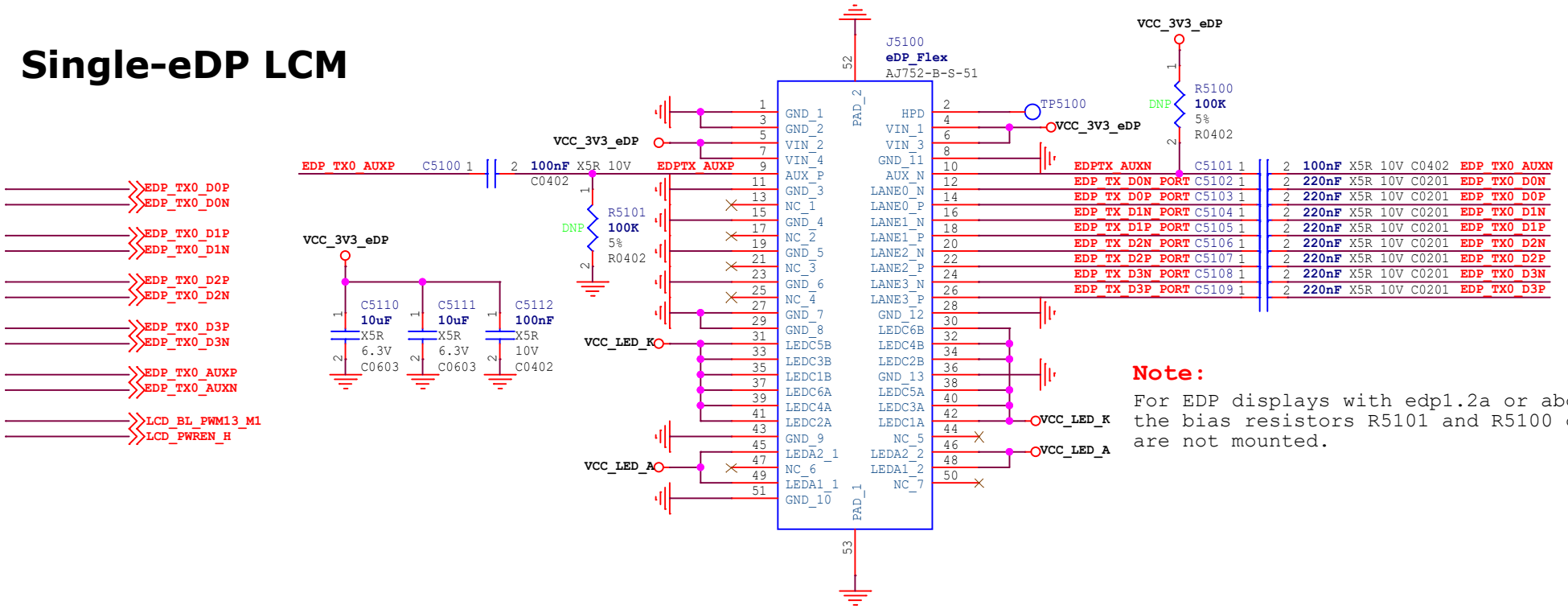
The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.



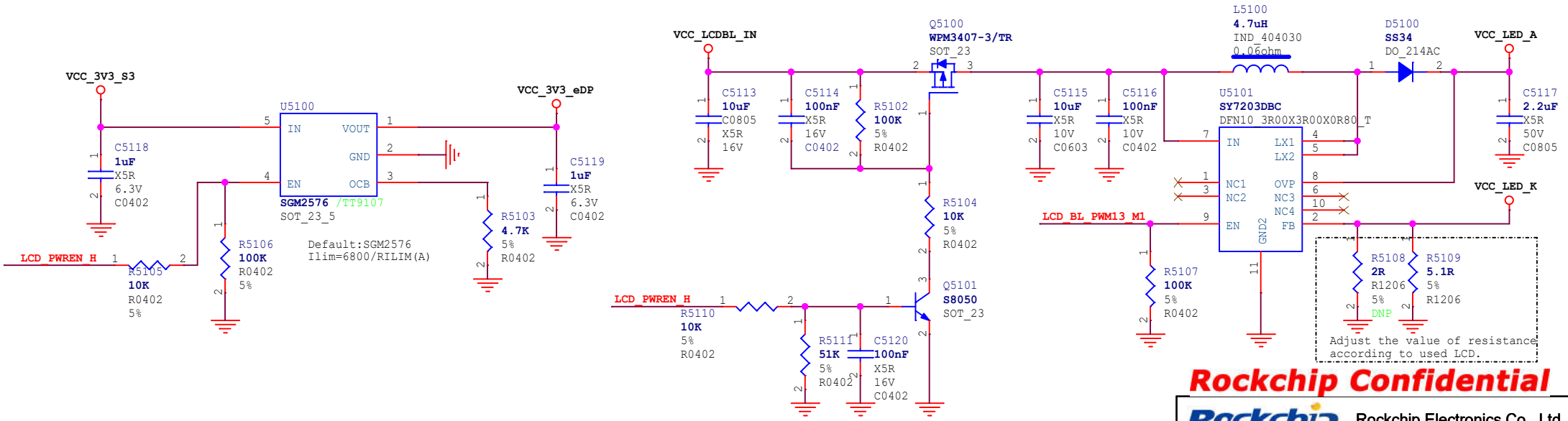
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	50.VO-HDMI2.1 TX				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	38 of 54

Single-eDP LCM



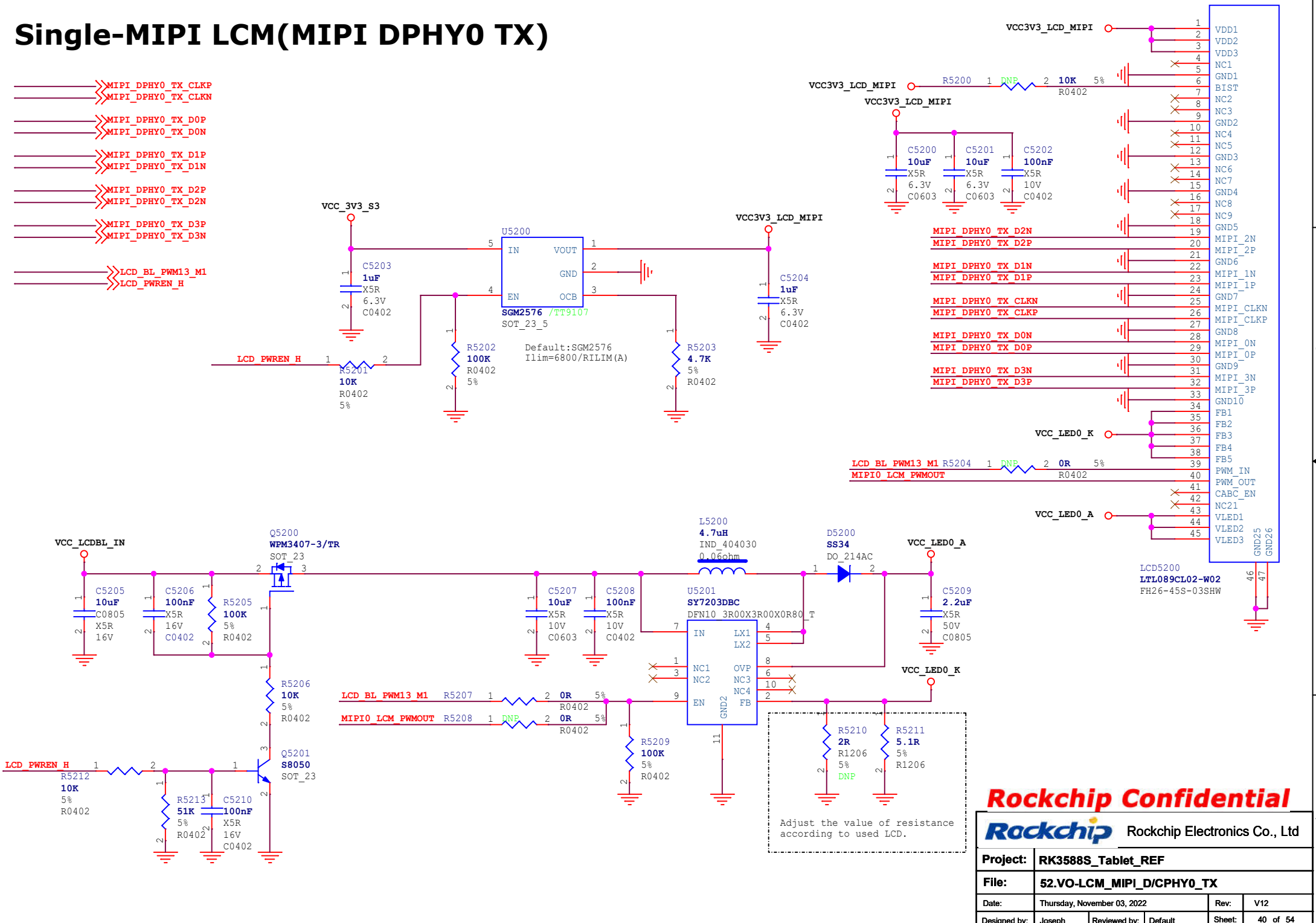
Note:

For EDP displays with edp1.2a or above, the bias resistors R5101 and R5100 of aux are not mounted.



Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	51.VO-LCM_eDP1.3 TX				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	Default	Sheet:	39 of 54

Single-MIPI LCM(MIPI DPHY0 TX)



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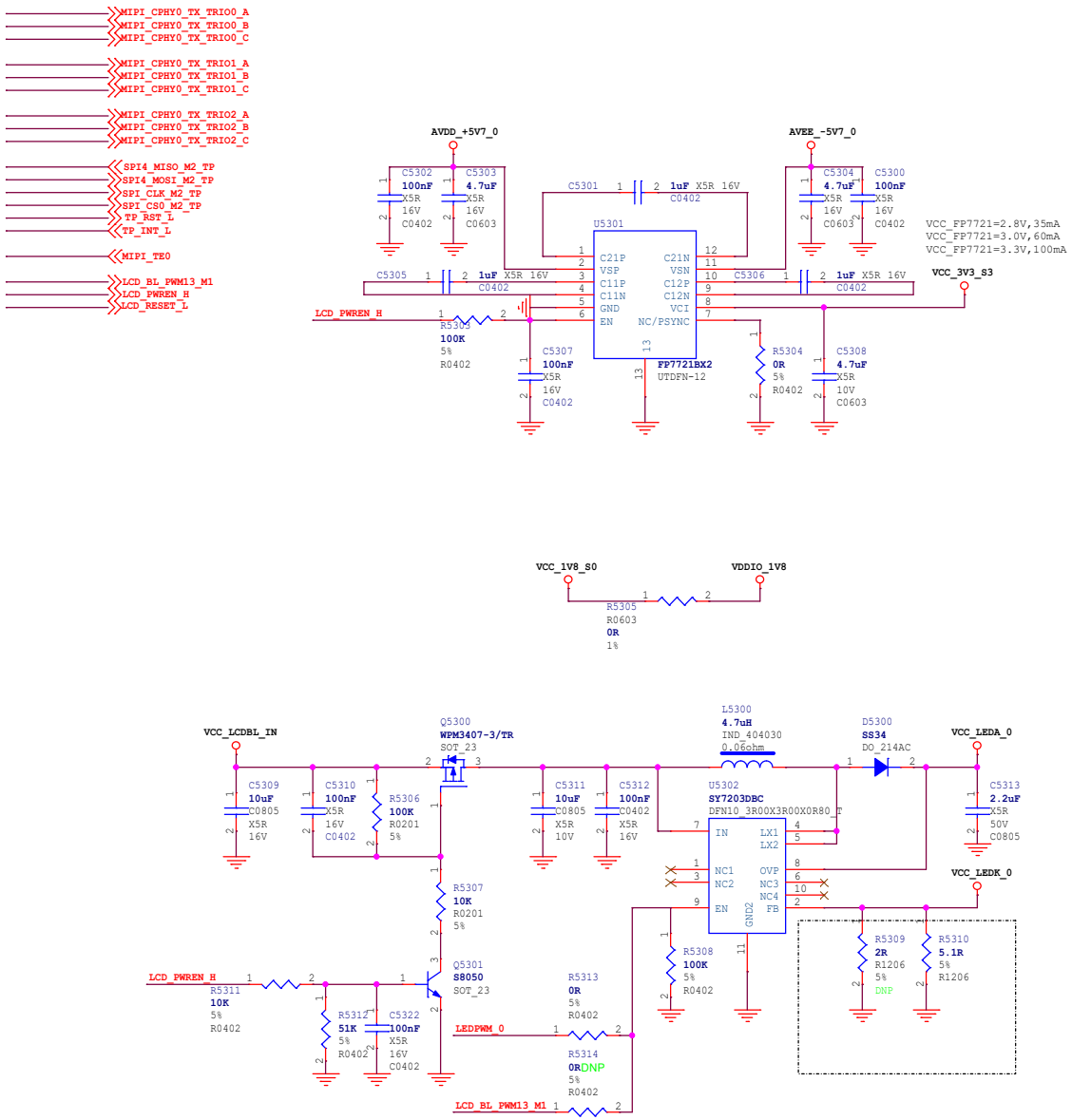
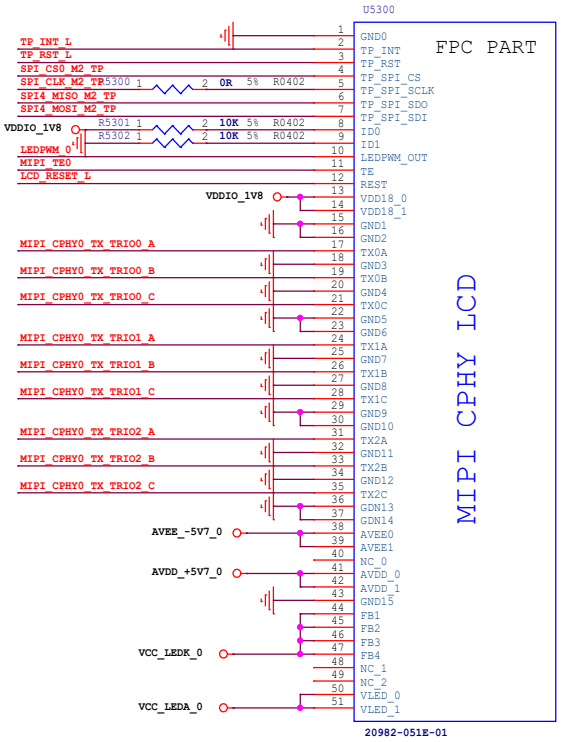
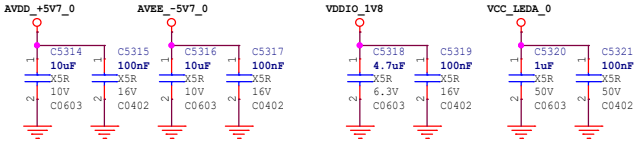
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	52.VO-LCM_MIPI_D/CPHY0_TX				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	Default	Sheet:	40 of 54

Single-MIPI LCM(MIPI CPHY0 TX)

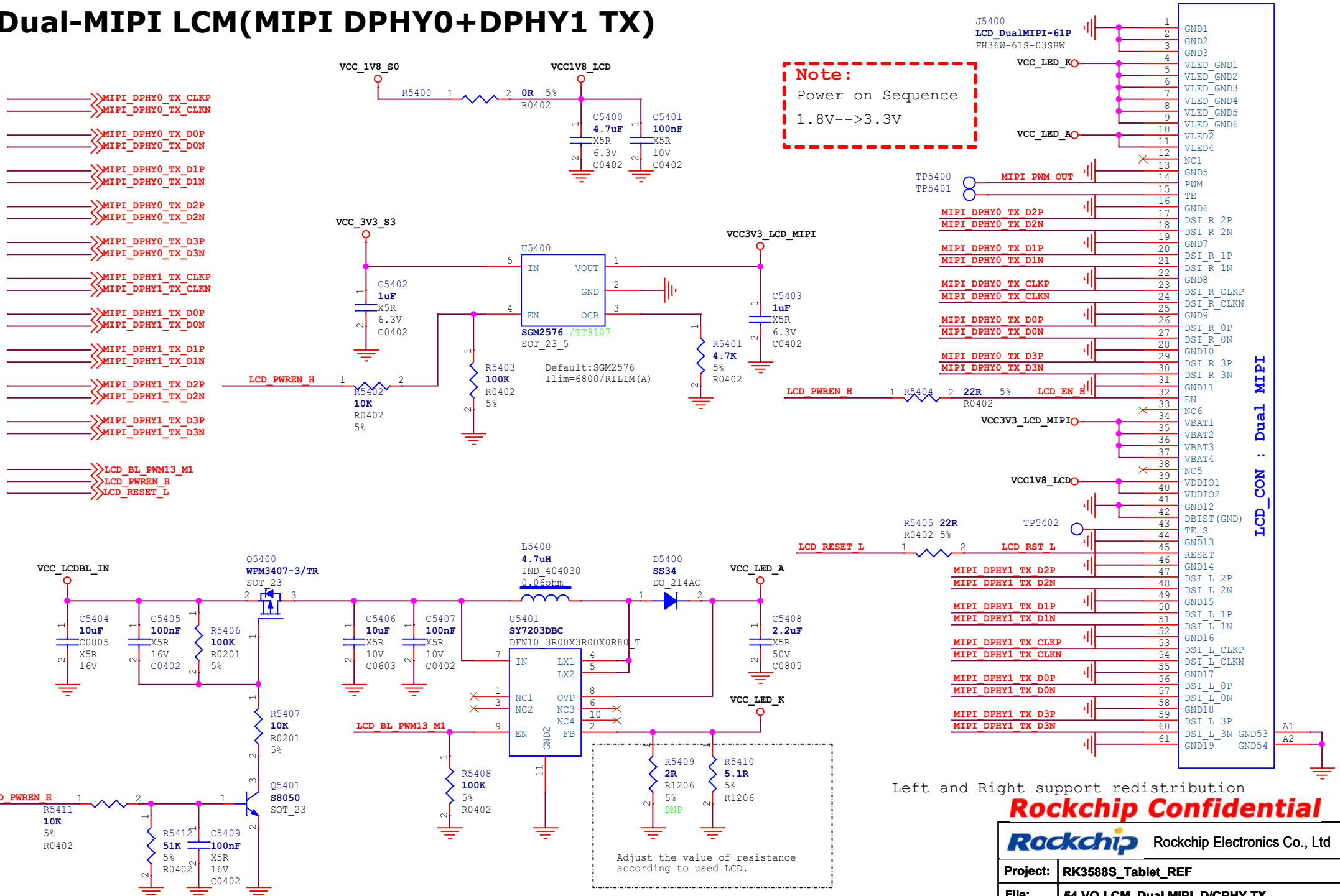






Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	53.VO-LCM_MIPI_D/CPHY0_TX(opt)				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	Default	Sheet:	41 of 54

Dual-MIPI LCM(MIPI DPHY0+DPHY1 TX)

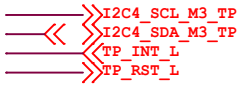


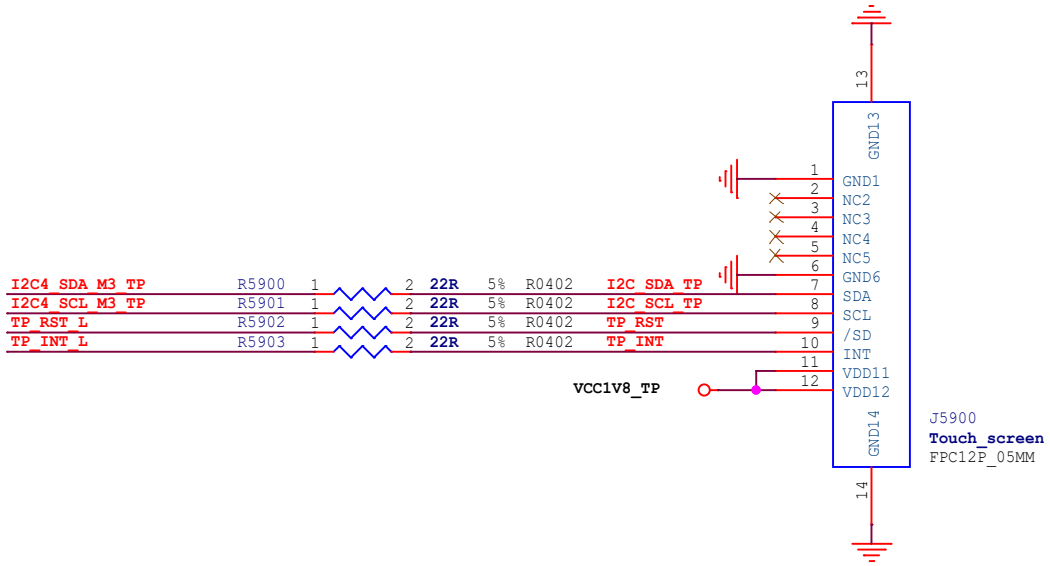
Left and Right support redistribution

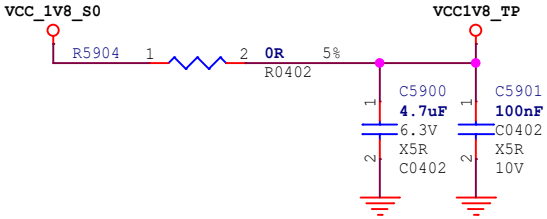
Rockchip Confidential

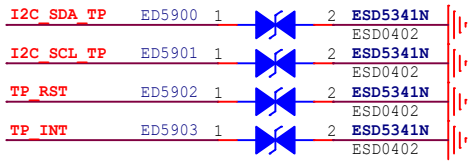
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	54.VO-LCM_Dual MIPI_D/CPHY TX				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	Default	Sheet:	42 of 54

Touch Panel connector



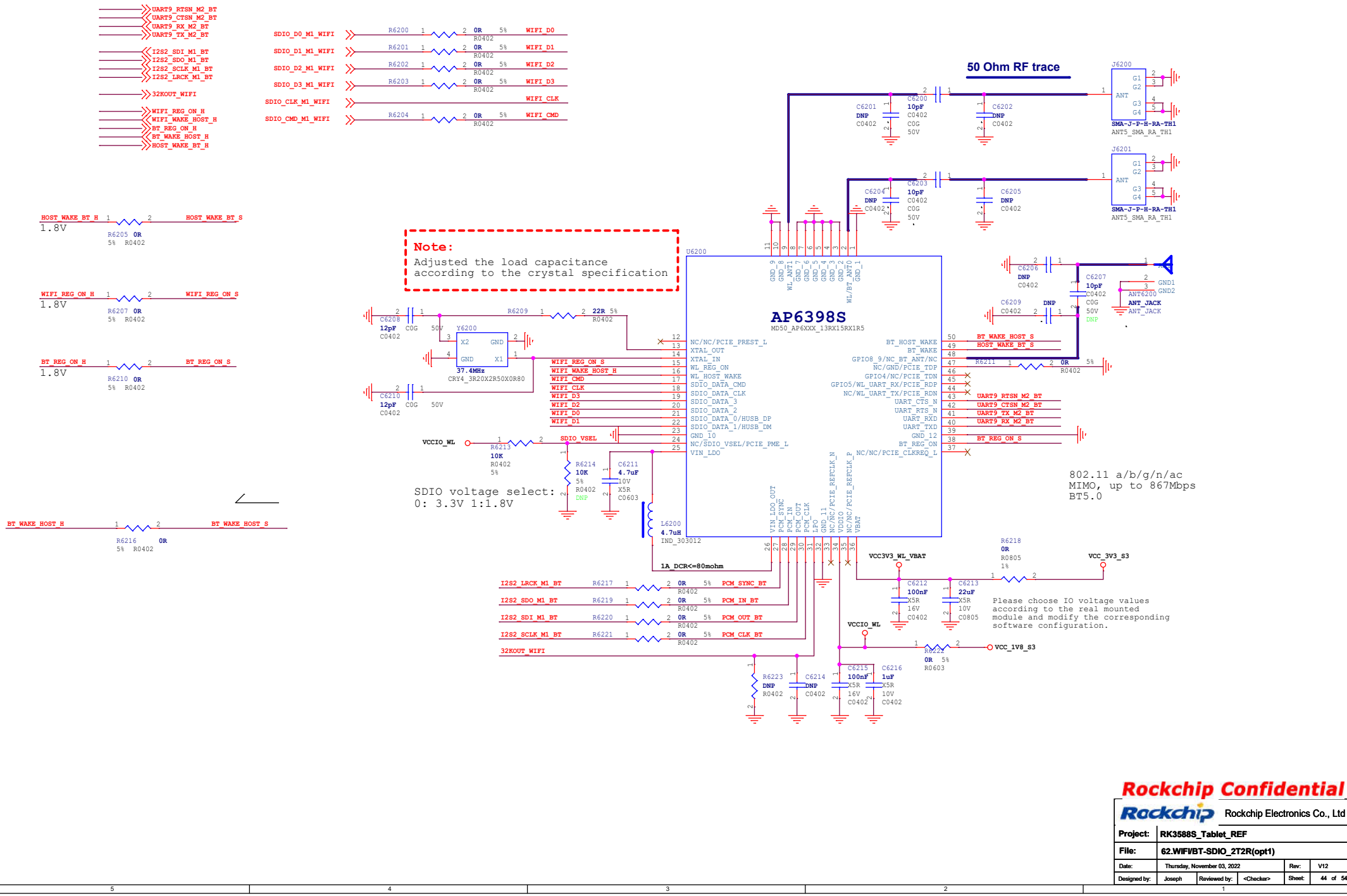






Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	59.TP Connector_COF(I2C)				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	Default	Sheet:	43 of 54

SDIO WIFI/BT Module-2T2R

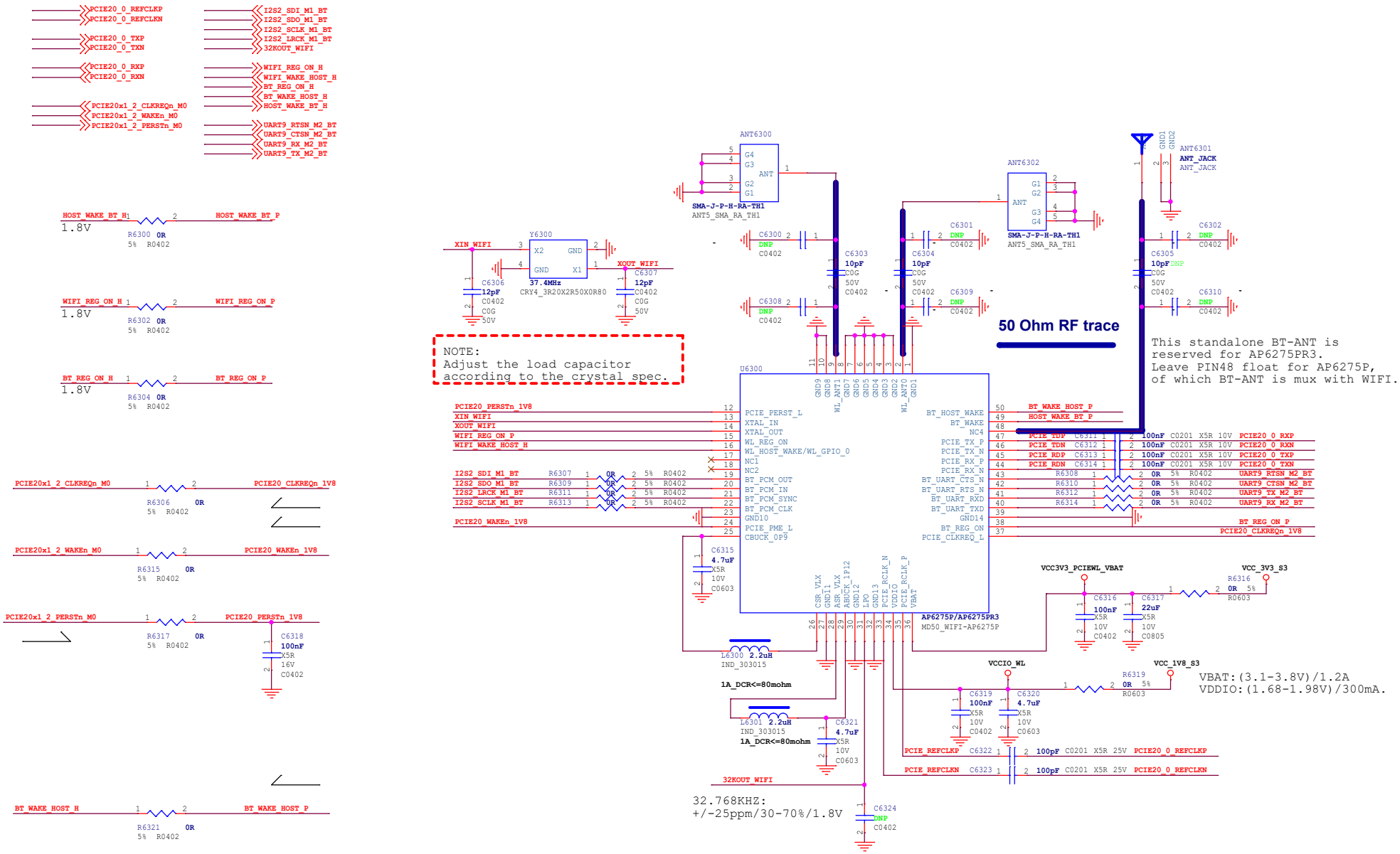


Rockchip Confidential

Rockchip Electronics Co., Ltd

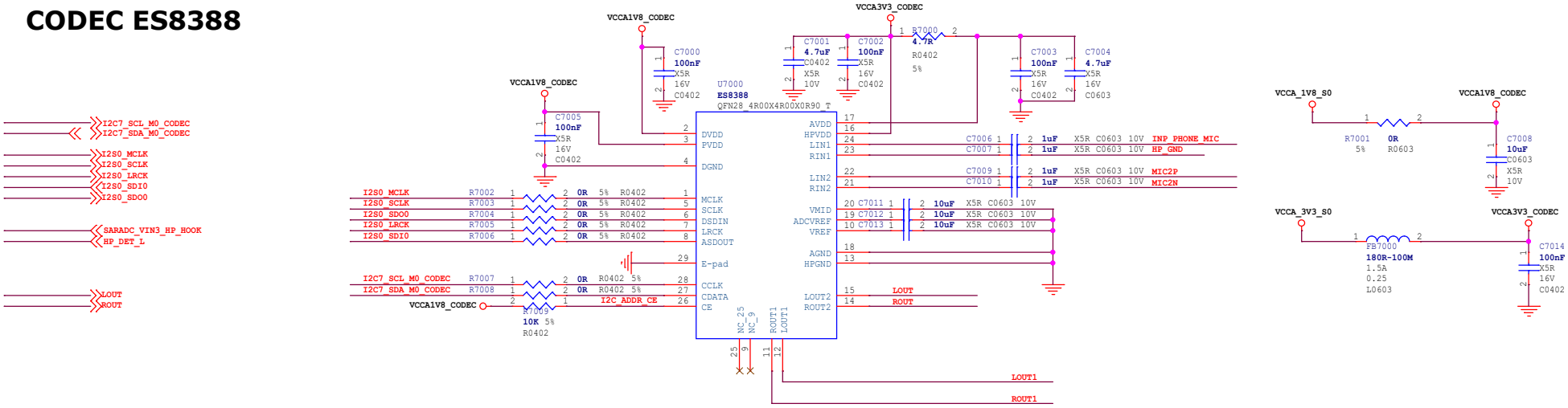
Project:	RK3588S_Tablet_REF				
File:	62.WIFI/BT-SDIO_2T2R(opt1)				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	44 of 54

PCIe WIFI6/BT Module-2T2R

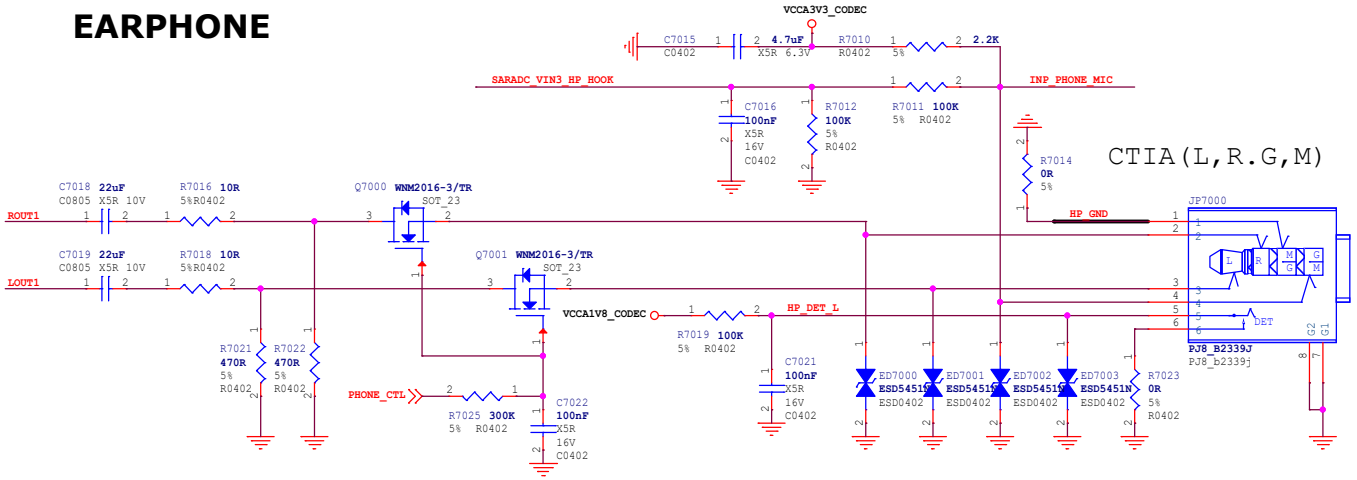


Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	63.WIFI/BT-PCIe_2T2R(opt2)				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	45 of 54

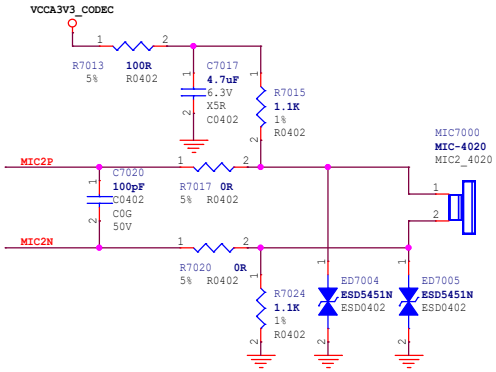
CODEC ES8388



EARPHONE



Analog MIC



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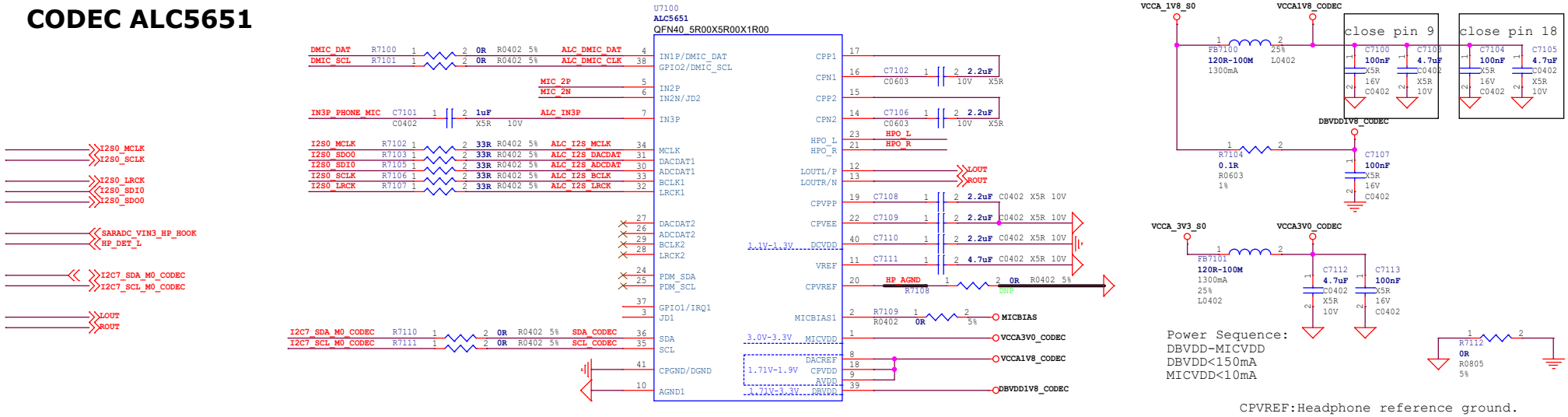
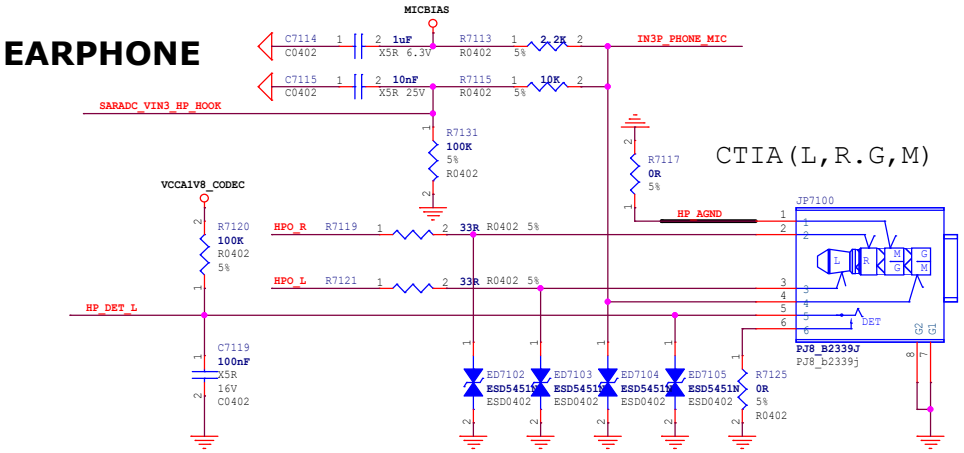
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	70.Audio Codec				
Date:	Friday, November 04, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	46 of 54

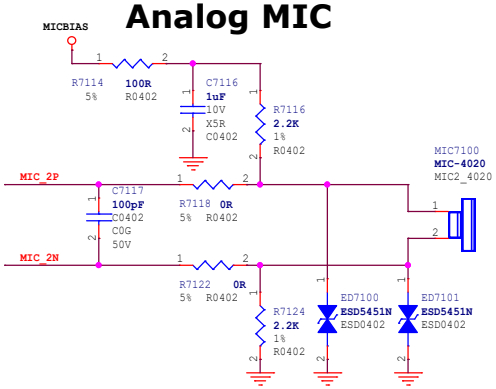
CODEC ALC5651



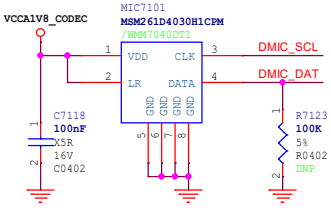
EARPHONE



Analog MIC



DIGITAL MIC



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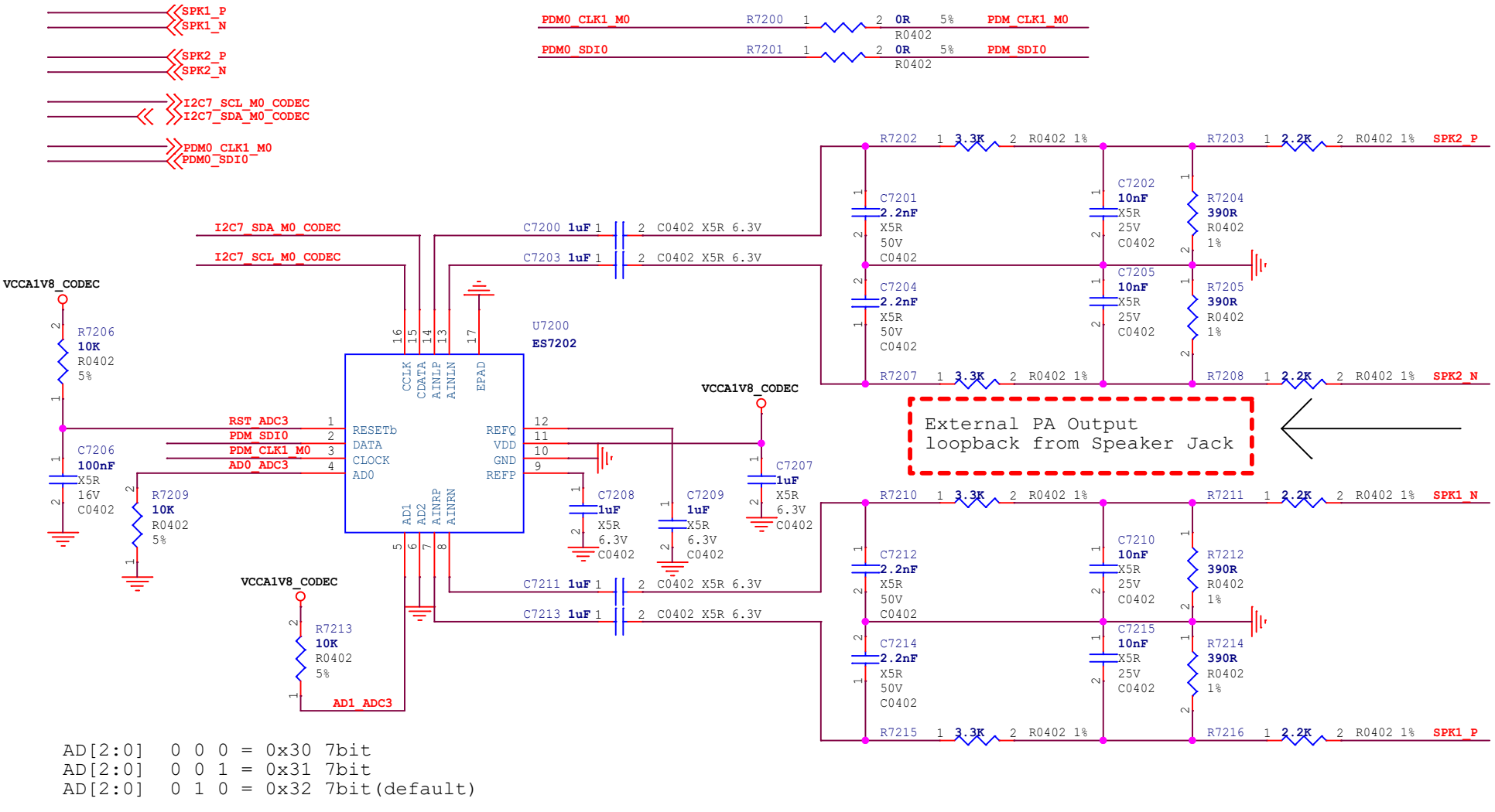
Rockchip Electronics Co., Ltd

Project:	RK3588S_Tablet_REF				
File:	71.Audio Codec(opt)				
Date:	Friday, November 04, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	Default	Sheet:	47 of 54

Loopback



AD[2:0] 0 0 0 = 0x30 7bit
AD[2:0] 0 0 1 = 0x31 7bit
AD[2:0] 0 1 0 = 0x32 7bit(default)

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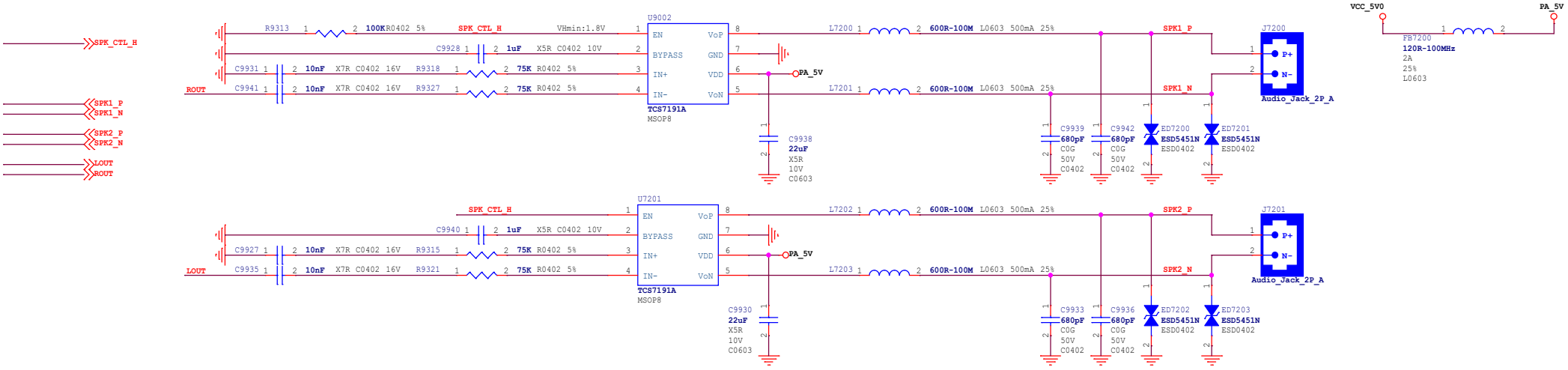
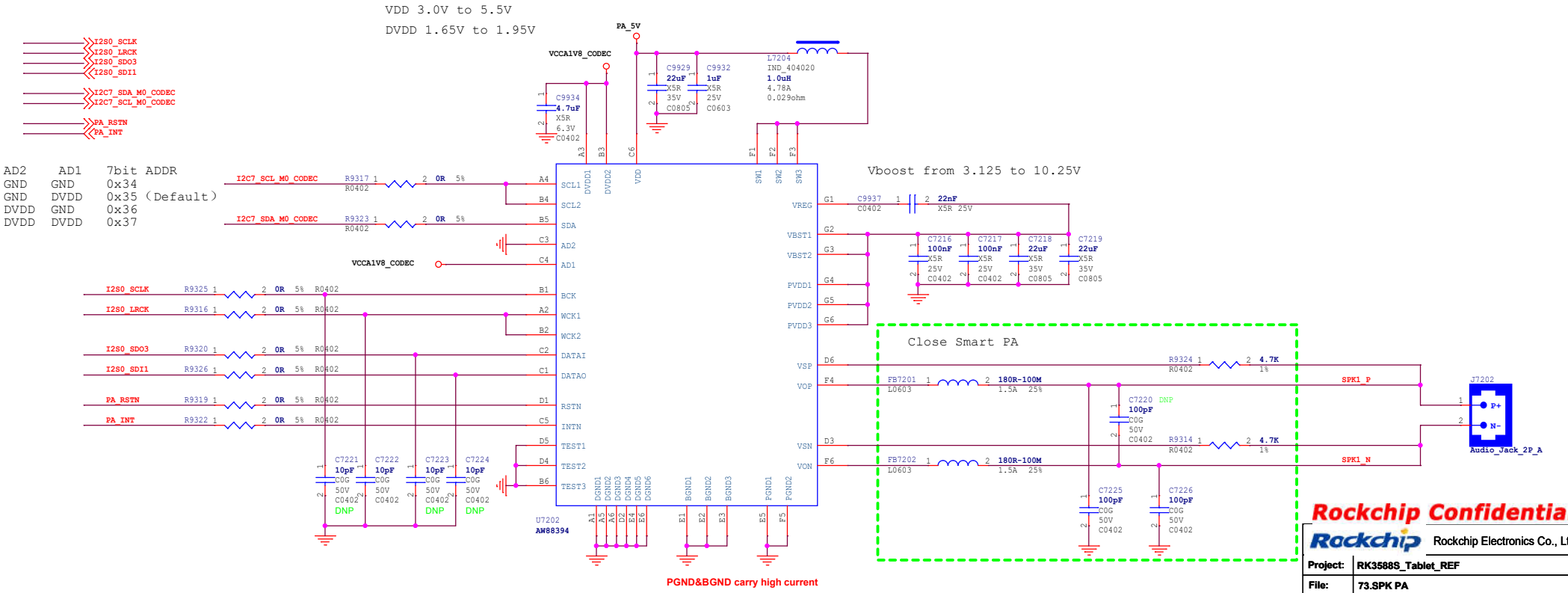
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	72.Audio-Loopback				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	48 of 54

SPK PA（Default）

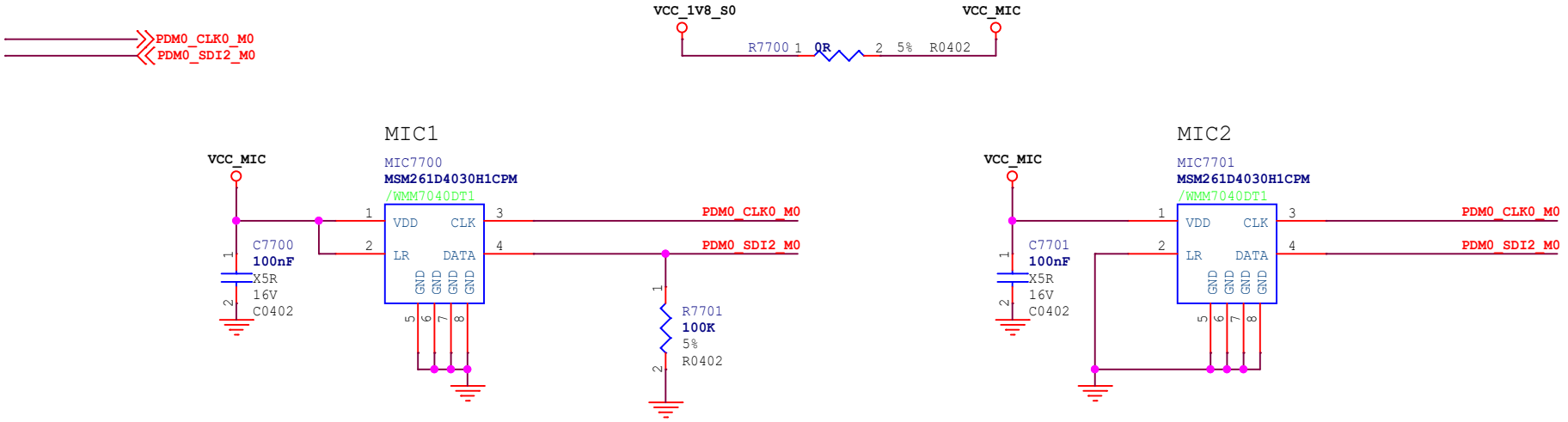


SPK PA（OPTION）



Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	73.SPK PA				
Date:	Friday, November 04, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	49 of 54

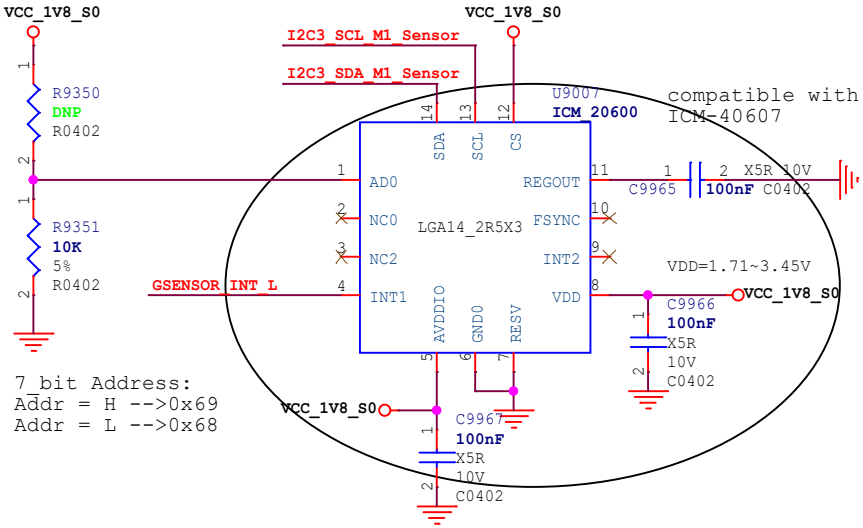
DMIC Array



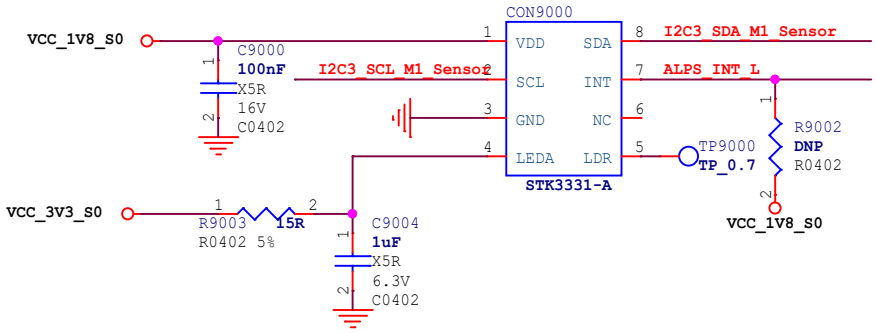
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	77.Audio-DMIC Array				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	50 of 54

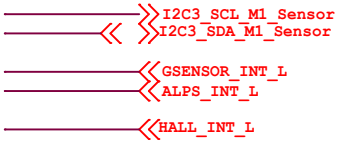
Gyroscope+G-sensor

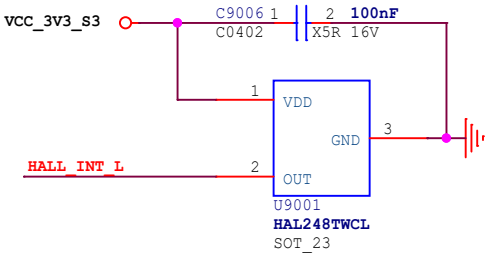


Ambient Light+Proximity Sensor



HALL SENSOR





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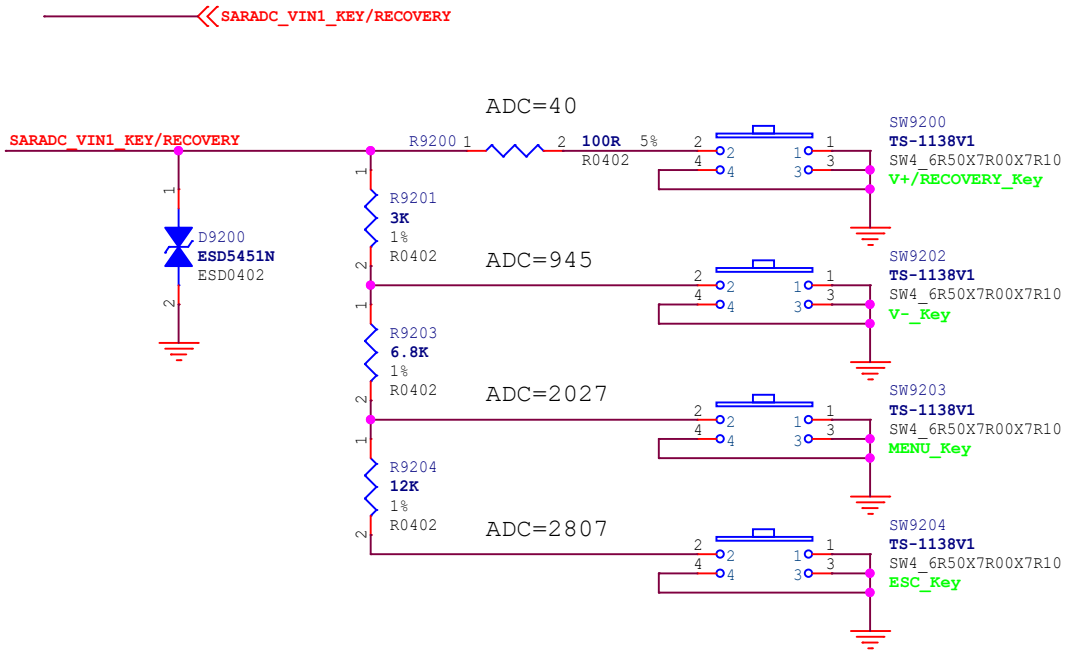
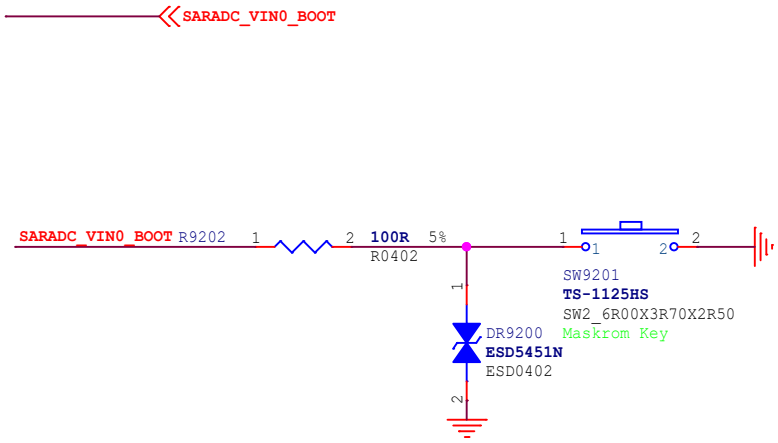
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	90.Sensor				
Date:	Monday, November 07, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	51 of 54

KEY Array

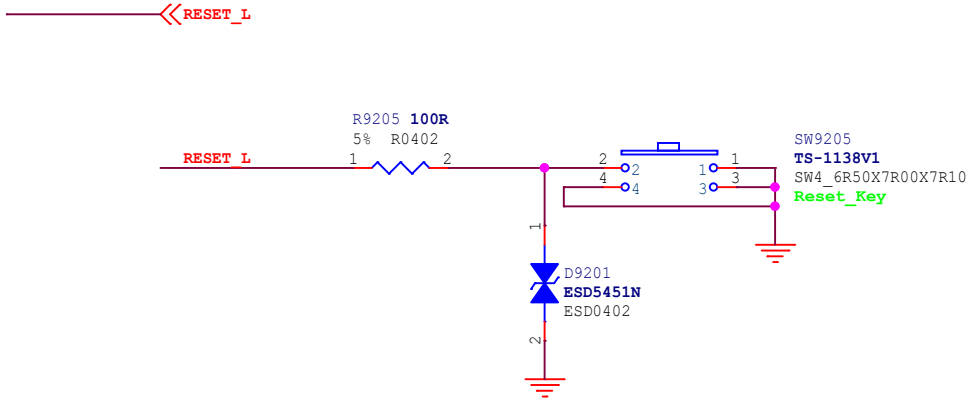


Maskrom Key

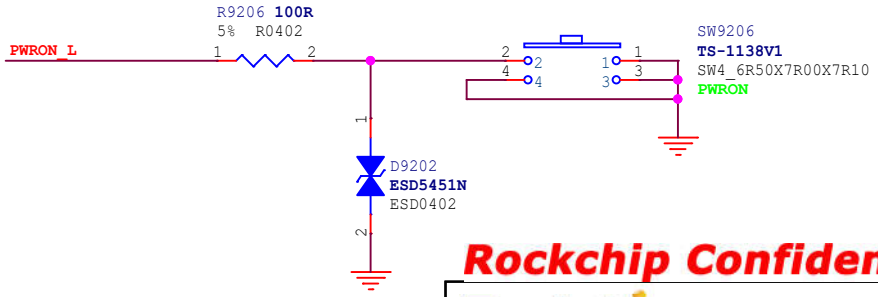


Note:
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

Reset_Key



PWR_Key



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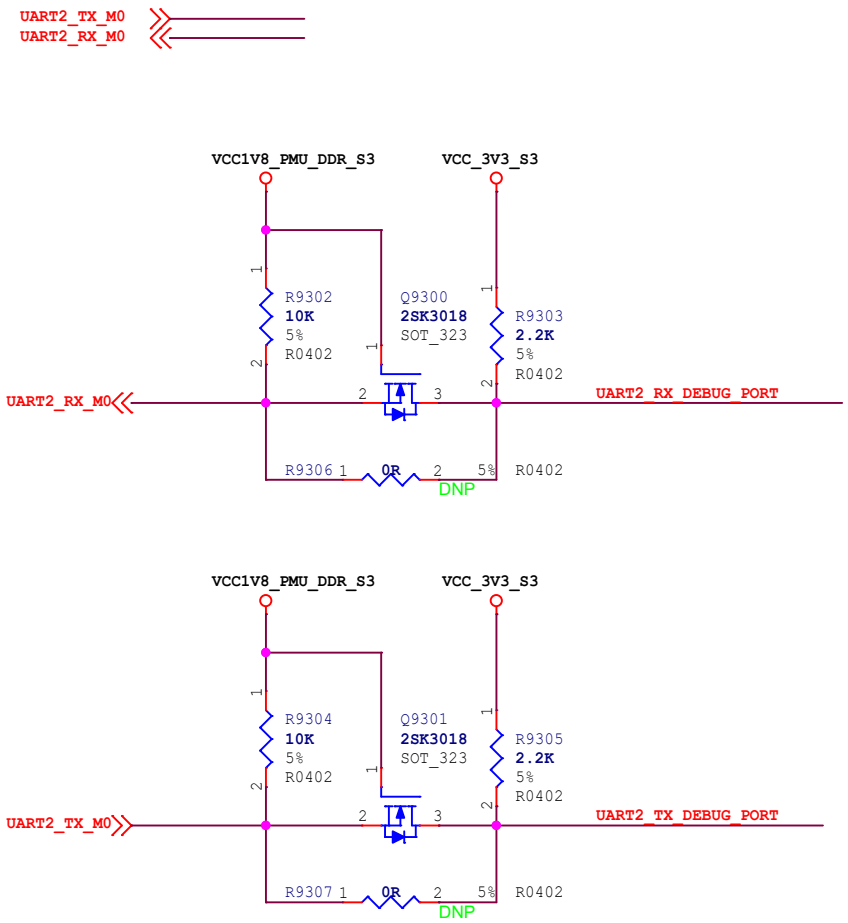
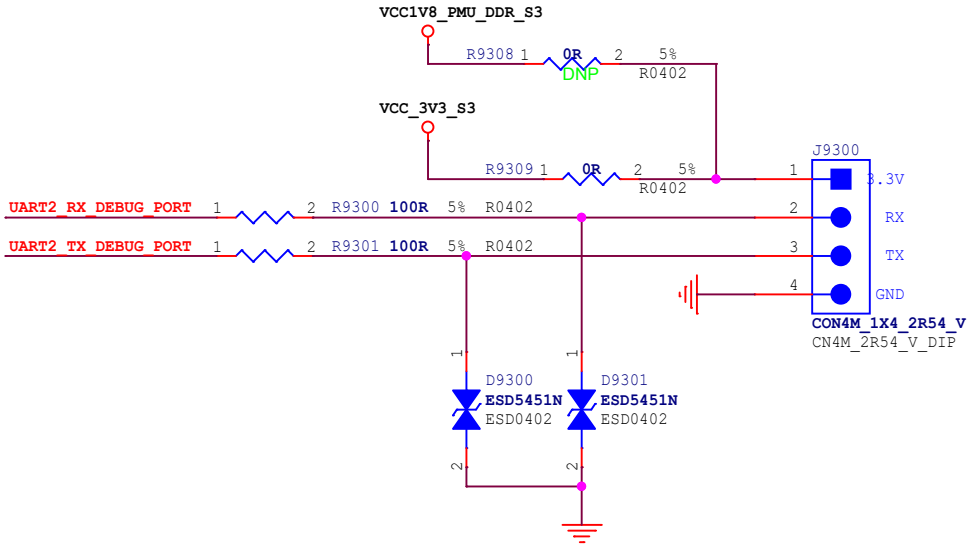
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	92.KEY Array				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	52 of 54

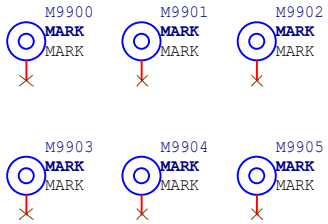
UART Debug



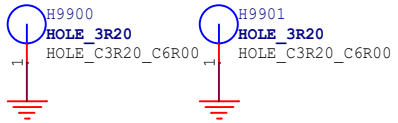


Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	93.UART Debug				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	53 of 54

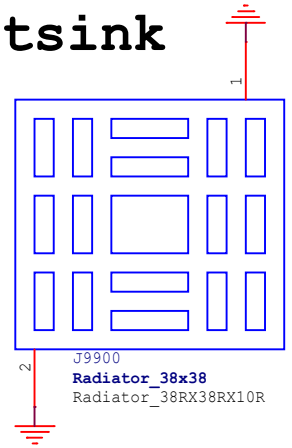
PCB Mark Point



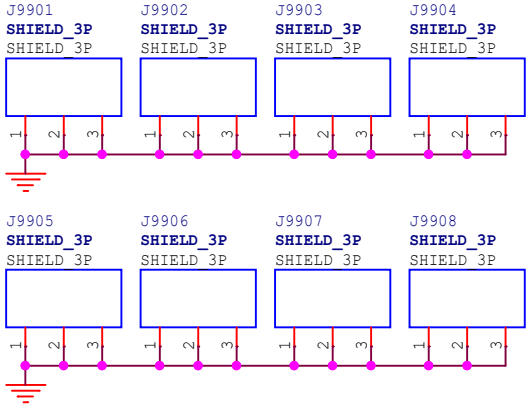
Mechanical Hole



Heatsink



Shield



Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	**RK3588S_Tablet_REF**				
File:	**99.Mark/Heatsink**				
Date:	Thursday, November 03, 2022			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	54 of 54