Reference Schematics For RK3588

RK3588_AIOT_REF_SCH_V14

Main Functions Introduction

1) PMIC: 1xRK806-1+DiscretePower
2) RAM: 2xLPDDR4/4X_32bit or 2xLPDDR5_32bit
3) ROM: eMMC5.1(Default) or SPI Flash
4) Support: 1xSDMMC3.0 Card
5) Support: 1 x TYPEC3.0(With DP TX)+1 x USB3.0 HOST+ 1 x USB20 HOST or USB3.0/2.0 HUB
6) Support: 3 x SATA3.0 Connector (7pin) or SATA PM
7) Support: 1 x 4Lane PCIe3.0 Connector (Dual Mode)
8) Support: 2 x 4Lanes MIPI DPHY RX Camera
9) Support: 2 x 4Lanes MIPI D/CPHY RX Camera
10) Support: 1 x HDMI2.0 RX or HDMI IN to mipi
11) Support: 2 x HDMI2.1 TX or 2 x eDP1.3 TX
12) Support: 2 x 4Lanes MIPI D/CHY-TX
13) Support: 1xVGA Connector(DP to VGA)
14) Support: 1x4Lanes DP Port
15) Support: a/b/g/n/ac/ax 2T2R WIFI 6/5(PCIE/SDIO) +BT5.0
16) Support: 1x 10/100/1000 RJ45 Port(RGMII)
17) Support: 1x 10/100/1000 RJ45 Port(PCIE)
18) Support: 4G Module
19) Support: PCIE M.2
20) Support: 1xHeadphone+2xSPK+1xAnalog MIC

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	00.Cover Page				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	0 of 99

Table of Content

Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

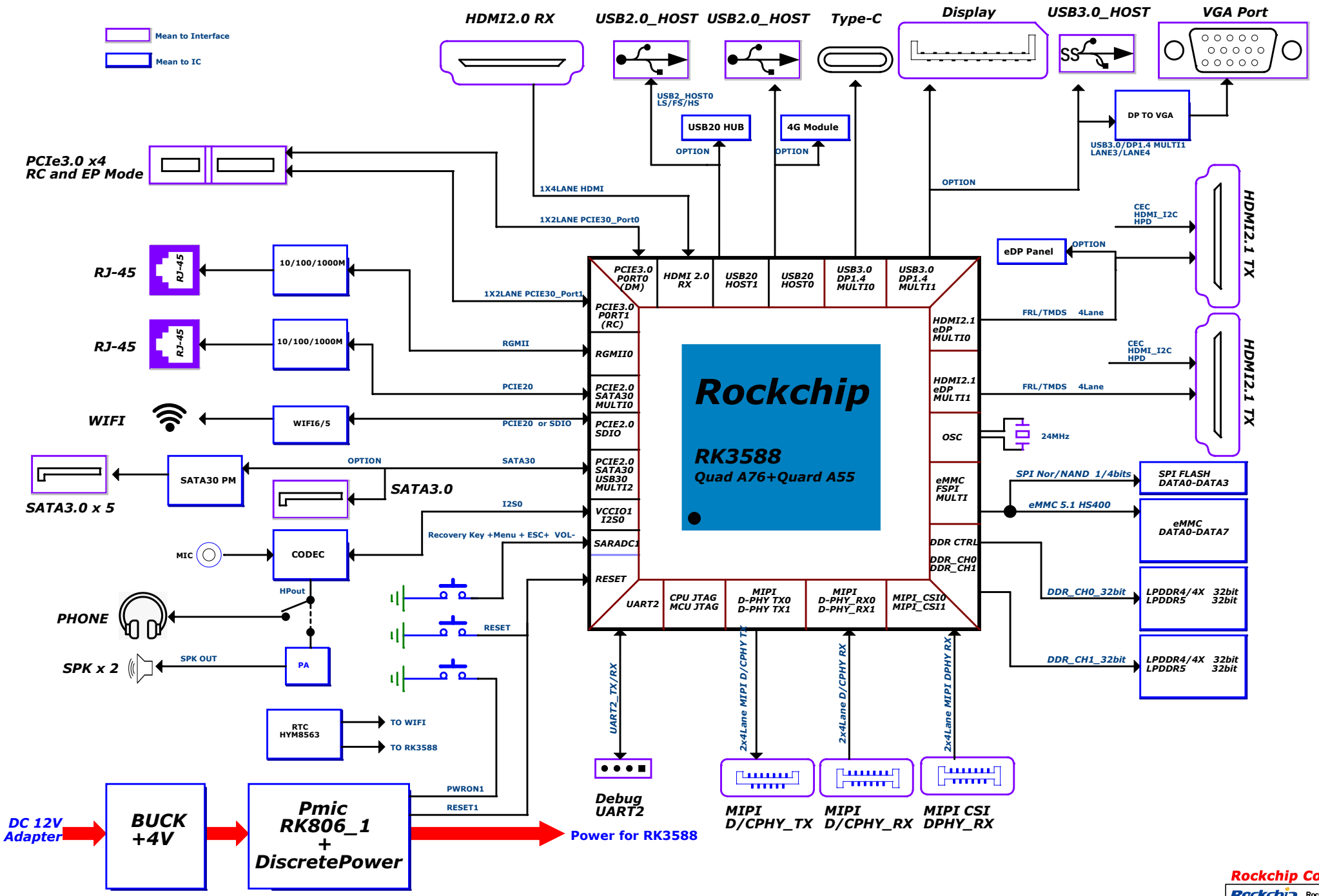
NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	01.Index and Notes				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	1 of 99

Revision History

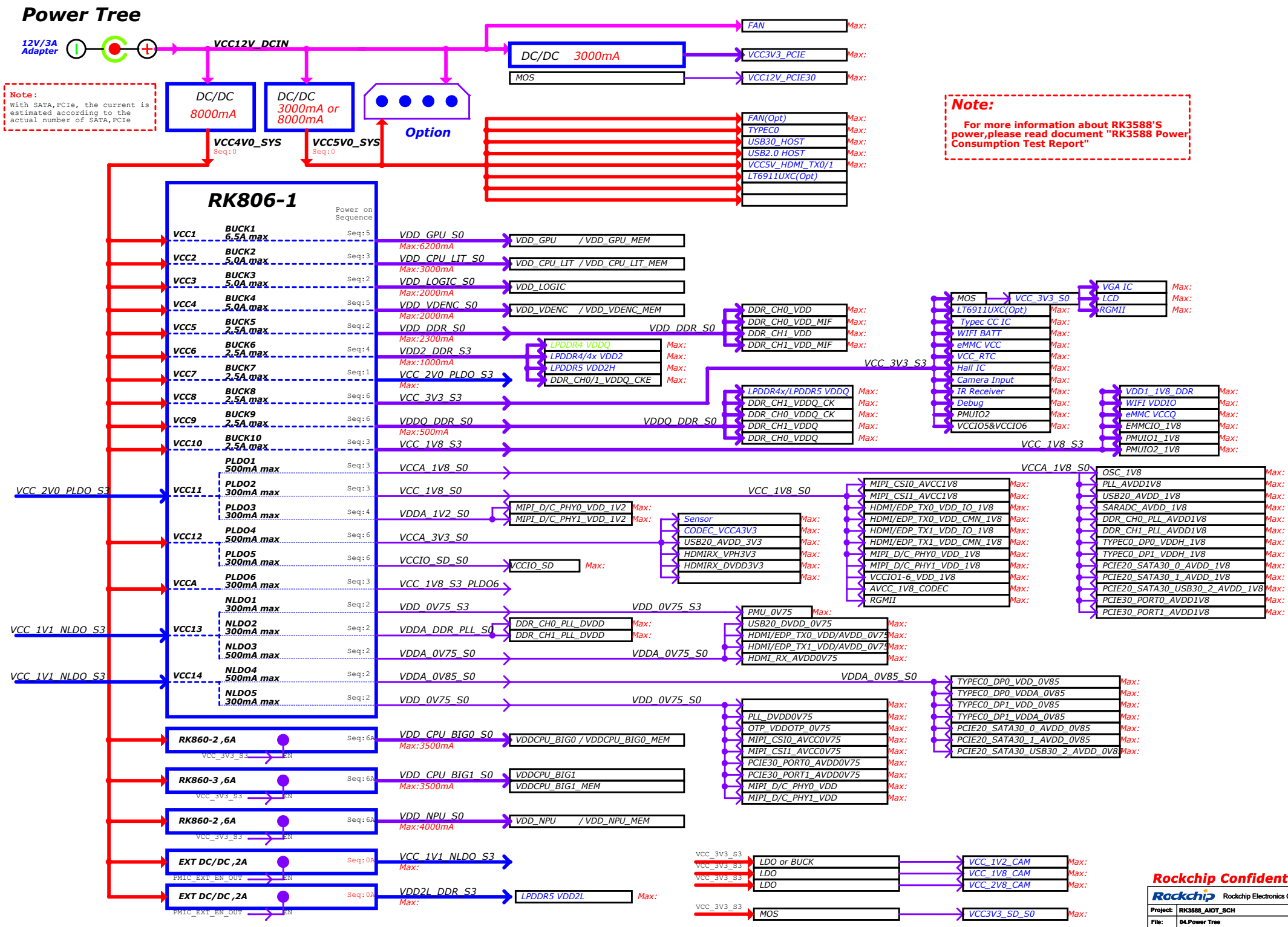
Version	Date	By	Change Dsecription	Approved
V1.0	2021-12-28	Felix.ruan	1.Revision preliminary version	Chenw
V1.1	2022-02-15	Felix.ruan	1.更改C5808-C5810,C5816的电容两边网络一致的问题。 2.C5205-C5208的耐压值改成25V；C5304－C5307的耐压值改成25V； C5614－C5617的耐压值改成25V。 3.C1600,C1608的电容改成1UF/4V。 4.PCIEx1_0_PERSTn_M1_L网络改成PCIEx1_0_PERSTn_M2_L；PCIEx1_0_CLKREQn _M1_L网络改成PCIEx1_0_CLKREQn_M2_L；PCIEx1_0_WAKEn_M1_L/GPIO1_B3网 络改成PCIEx1_0_WAKEn_M2_L/GPIO1_B3。 5.删除预留的电源。VCC_1V8_S3_PLDO6，"VCC1V8_PMU_DDR_S3"网络的电源直接 接VCC_1V8_S3。 6."VGA_HPDIN_L"(Pin AK27)与"SDMMC_PWREN"(Pin T28)的IO分配互换。 7.为了减少待机功耗，PMUIO2的供电电源改成1.8V。 8.L2300，L2301，L2203，L2205，L2207，L2303的电感0.22uH(TDK)改为0.24uH(Sunlord)； L2201的电感0.22uH(TDK)改为0.22uH (Sunlord)，封装IND_404020。 9.R2001电阻封装改0805。 10.C4900改为NC，R4911的47K改为2K，R4908的100K改为10K，R4909的100K改为10K。 11.eARC的功能不支持，相关eARC的网络改成"HDMI0/1_TX_SBDP/N"	Chenw
V1.2	2022-05-25	Felix.ruan	1.增加AU5426/SI52144的PCIE时钟方案；时钟发生器的OE脚，增加PCIE30X4_CLKREQn* 的控制，在待机时关掉，达到省电目的-----PAGE80 2.更改PAGE04，PAGE10页电流实测数据 3.更改RK3588的封装，增加MIPI D/C PHY的使用描述（此接口的MIPI_DPHY_RX不建义 使用） 4.SPKPA型号TT8642改成TCS7191A-----PAGE70&71 5.HDMI的eARC通道两个电容NC，暂不支持eARC功能----PAGE50 6.新增图纸中2A/3A BUCK的厂家型号 7.增加AW88394的SPK PA参考电路	Chenw
V1.3	2022-08-30	Felix.ruan	1.HDMI的下拉电阻从499ohm改成590ohm。-------PAGE50 2.删掉网络"PMIC_PWR_CTRL3"（Pin T32）。-------PAGE11& PAGE22 3.MP8759增加MODE SELECT控制。------PAGE11&PAGE20 4.增加每个SATA只能扩展5个PORT标注。----PAGE18 5.HDMI RX AVDD0V75和USB20_DVDD_0V75电压改成VDD_0V75_S0----PAGE14&PAGE17 6.R8024，R8026，R8039电阻改为10K；R8007电阻改为300R。----PAGE80 7.HDMI/EDP_TX_VDD_0V75电压网络改为"HDMI_VDDA0V85_S0"，实际软件设置0.8375V。 8.增加PCIE的标注。----PAGE18 9.增加PAGE51.VI－HDMI IN TO MIPI RX 10.RGMII的型号RTL82111改为RK631。----PAGE67 11.增加HDMI RX的使用注意事项标注。---PAGE49	Chenw
V1.4	2023-02-13	Felix.ruan	1.LT6911 UXC的I2S连接到ALC5651；CSCL(Pin 21)/CSDA(Pin 22)/HDMIIRX_DET_L网络 修改直接连到RK3588；增加LT6911UXE的兼容电路。-----PAGE51 PAGE71 2.增加eARC的注释。---PAGE50	Chenw

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	02.Revision History				
Date:	Wednesday, February 22, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	2 of 99



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	03.Block Diagram
Date:	Monday, February 20, 2023
Rev:	V1.4
Designed by:	RZF
Reviewed by:	
Sheet:	3 of 99

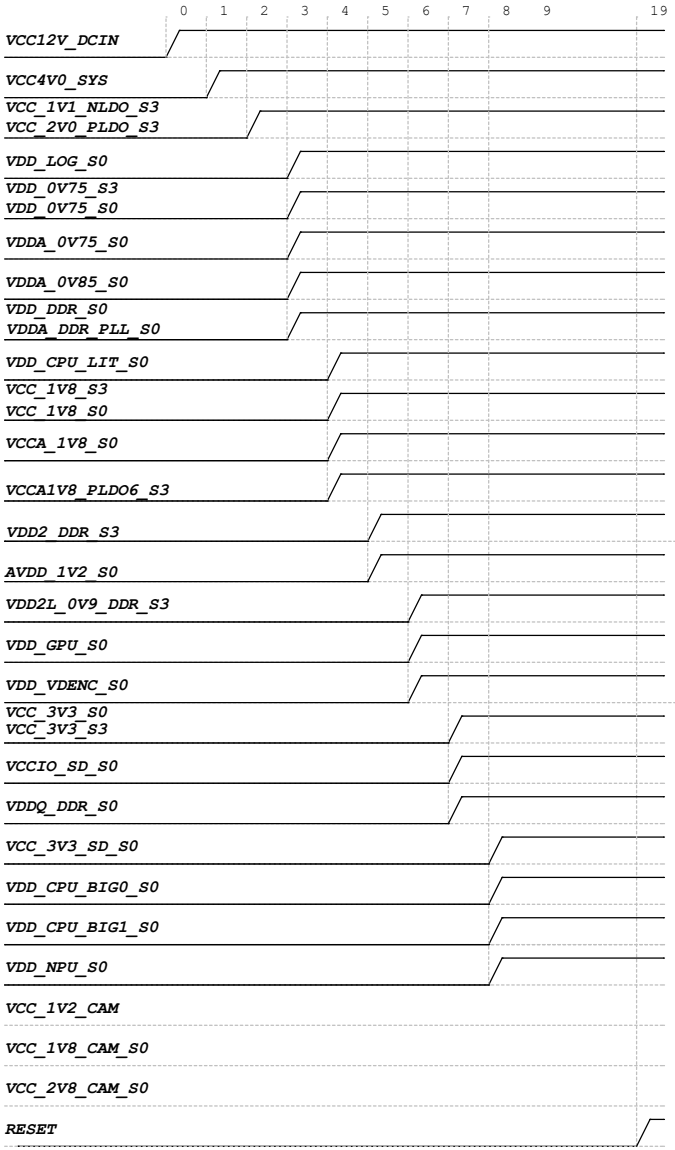
Power Tree



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	04.Power Tree
Date:	Monday, February 20, 2023
Rev:	V1.4
Designed by:	RZF
Reviewed by:	Default
Sheet:	4 of 99

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

IO Type	Operating Voltage
1.8V Only	VCCIO*_1V8=1.8V
1.8V or 3.3V	VCCIO*_1V8=1.8V VCCIO*=1.8V or 3.3V

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	05.System Power Sequence				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	5 of 99

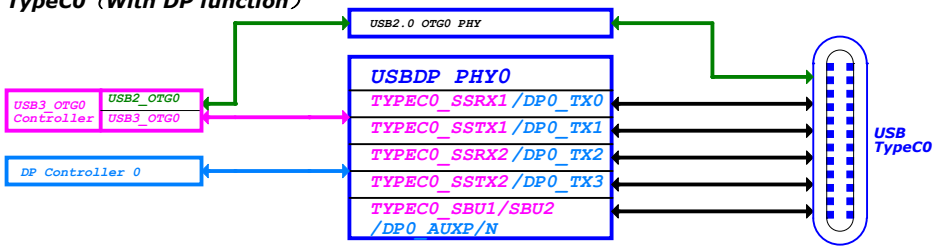
USB Controller Configure Table

Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1M/DP0_TX1M	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1M/DP1_TX1M	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

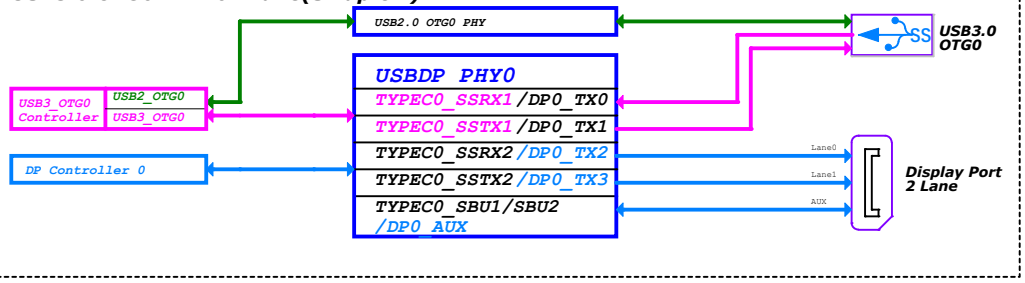
			OPTION1 USB30 HOST	OPTION2 USB30 HOST	OPTION3 USB30 HOST
USB30 HOST2	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM		
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM			USB20_HOST1_DP USB20_HOST1_DM	
					TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

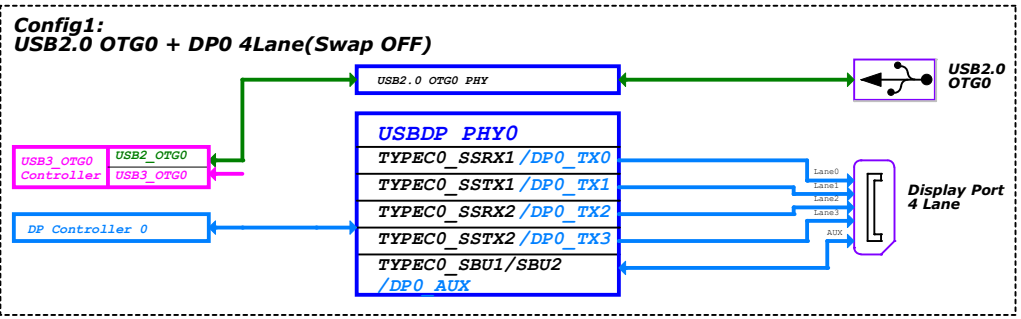
Config0:
TypeC0（With DP function）



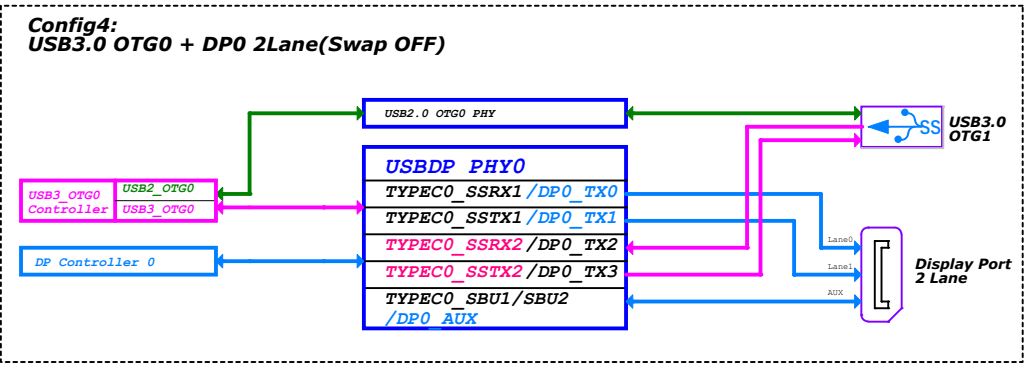
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



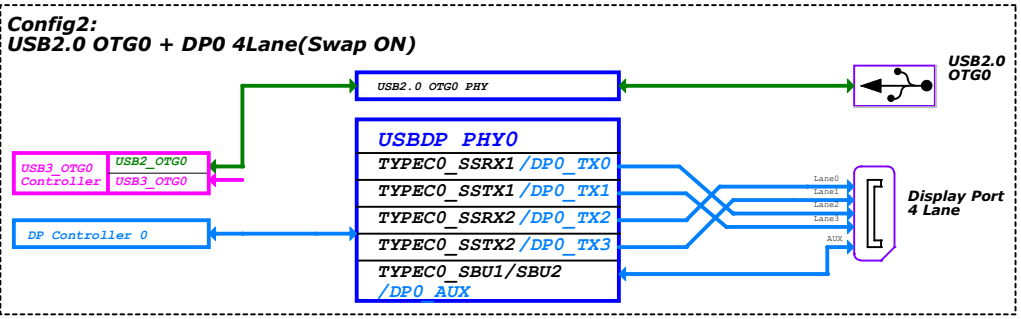
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)

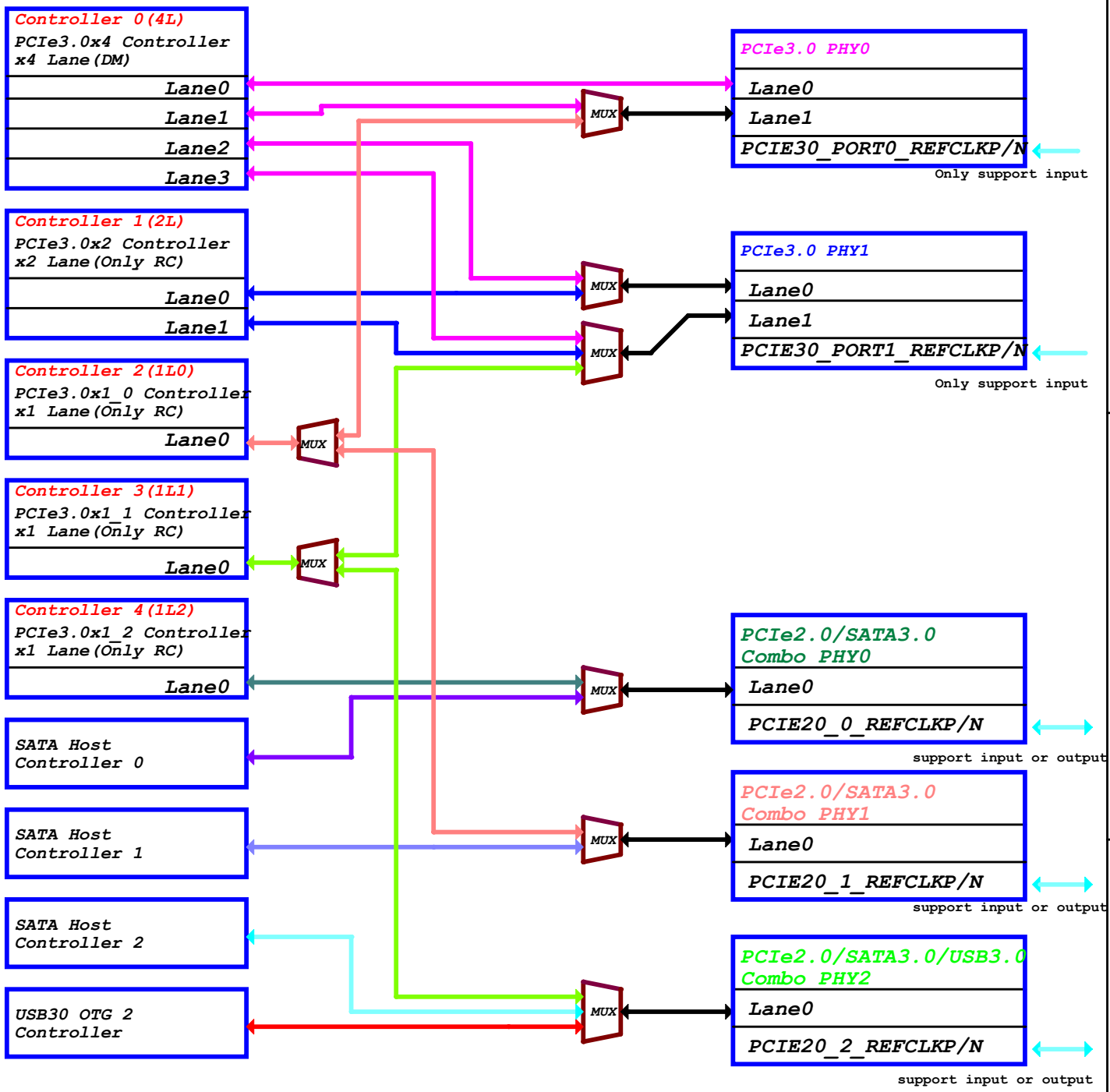


Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	07.USB Controller Configure Tab
Date:	Monday, February 20, 2023
Rev:	V1.4
Designed by:	RDF
Reviewed by:	
Sheet:	7 of 99

PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M*
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M*
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

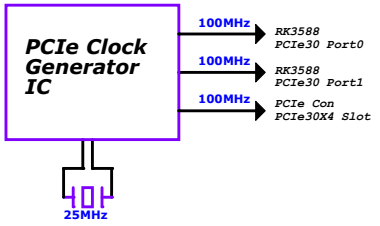
Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

PCIe/SATA Function Combination

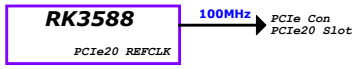
Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK



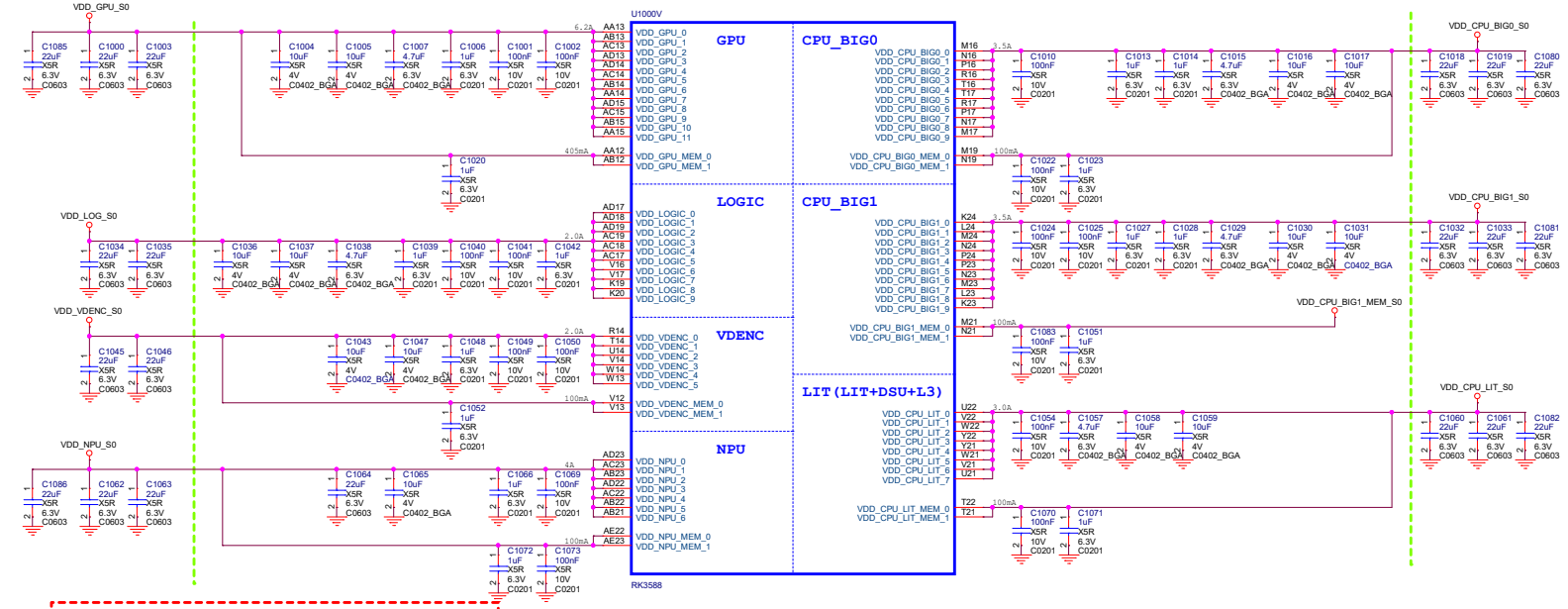
PCIe2.0 REFCLK



Rockchip Confidential

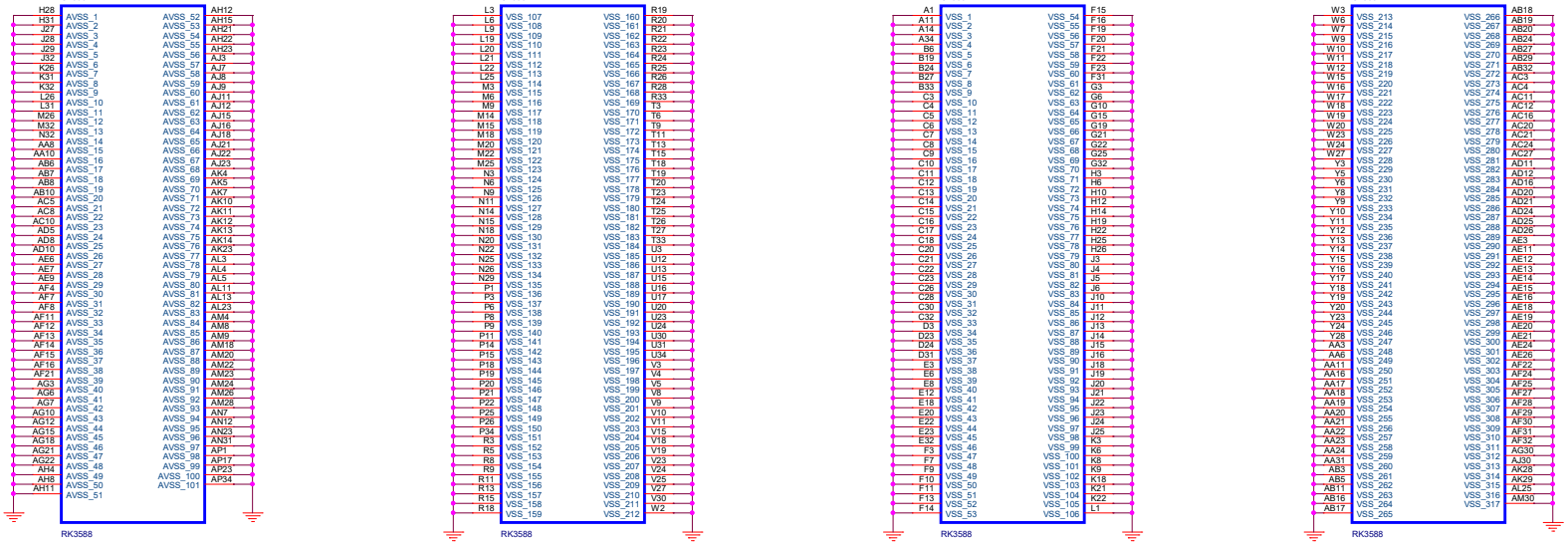
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	08.PCIE Fun Map
Date:	Monday, February 20, 2023
Rev:	V1.4
Designed by:	RZF
Reviewed by:	
Sheet:	8 of 99

RK3588_V(POWER)



Note:

The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



Rockchip Confidential

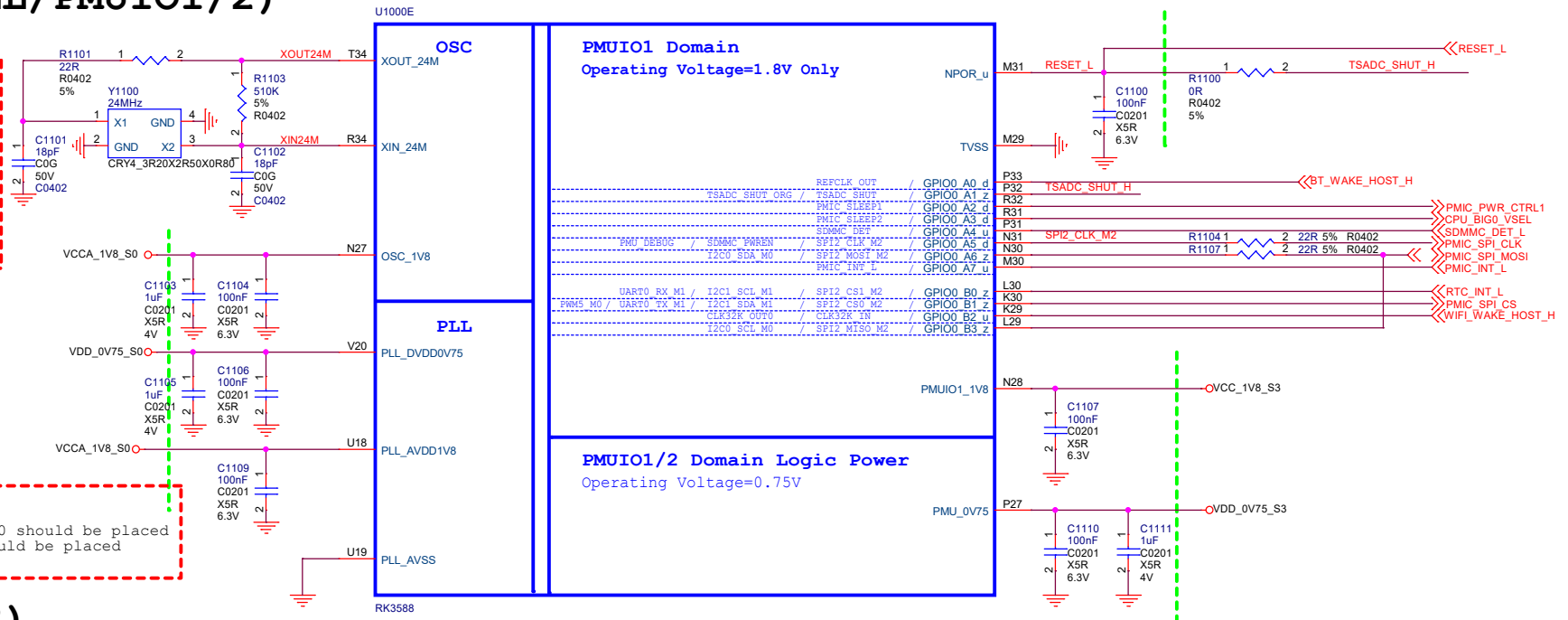
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	10.RK3588_Power/GND		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by:	RZF	Reviewed by:	Sheet: 10 of 99

RK3588_E(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification

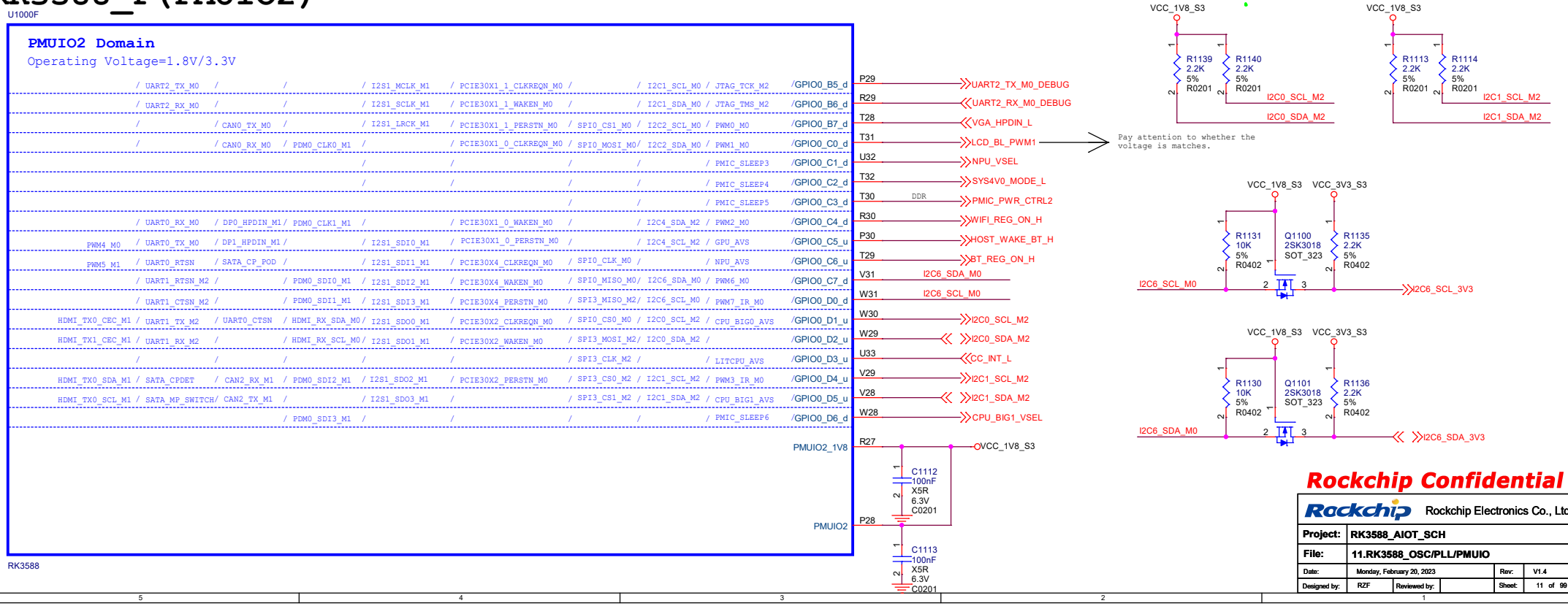
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



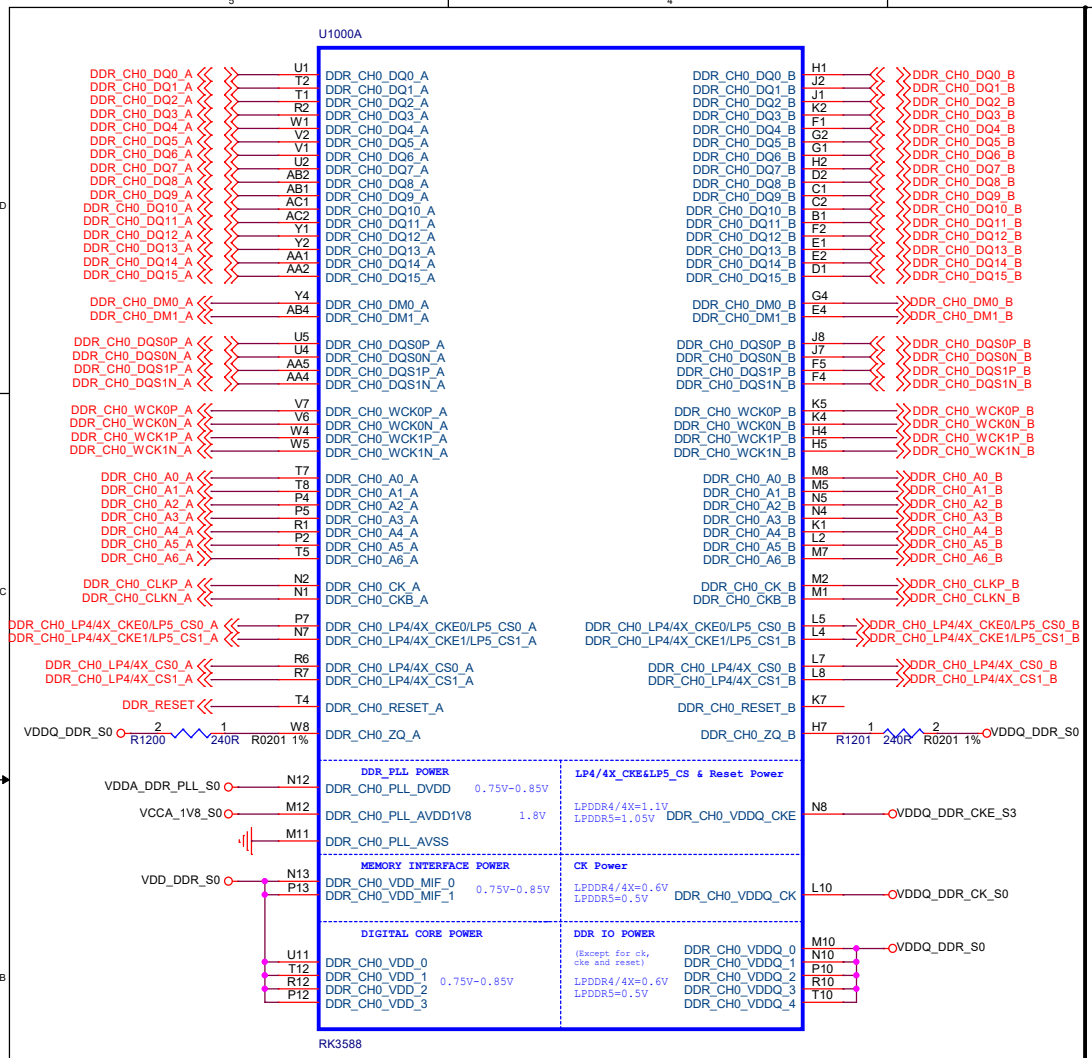
Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

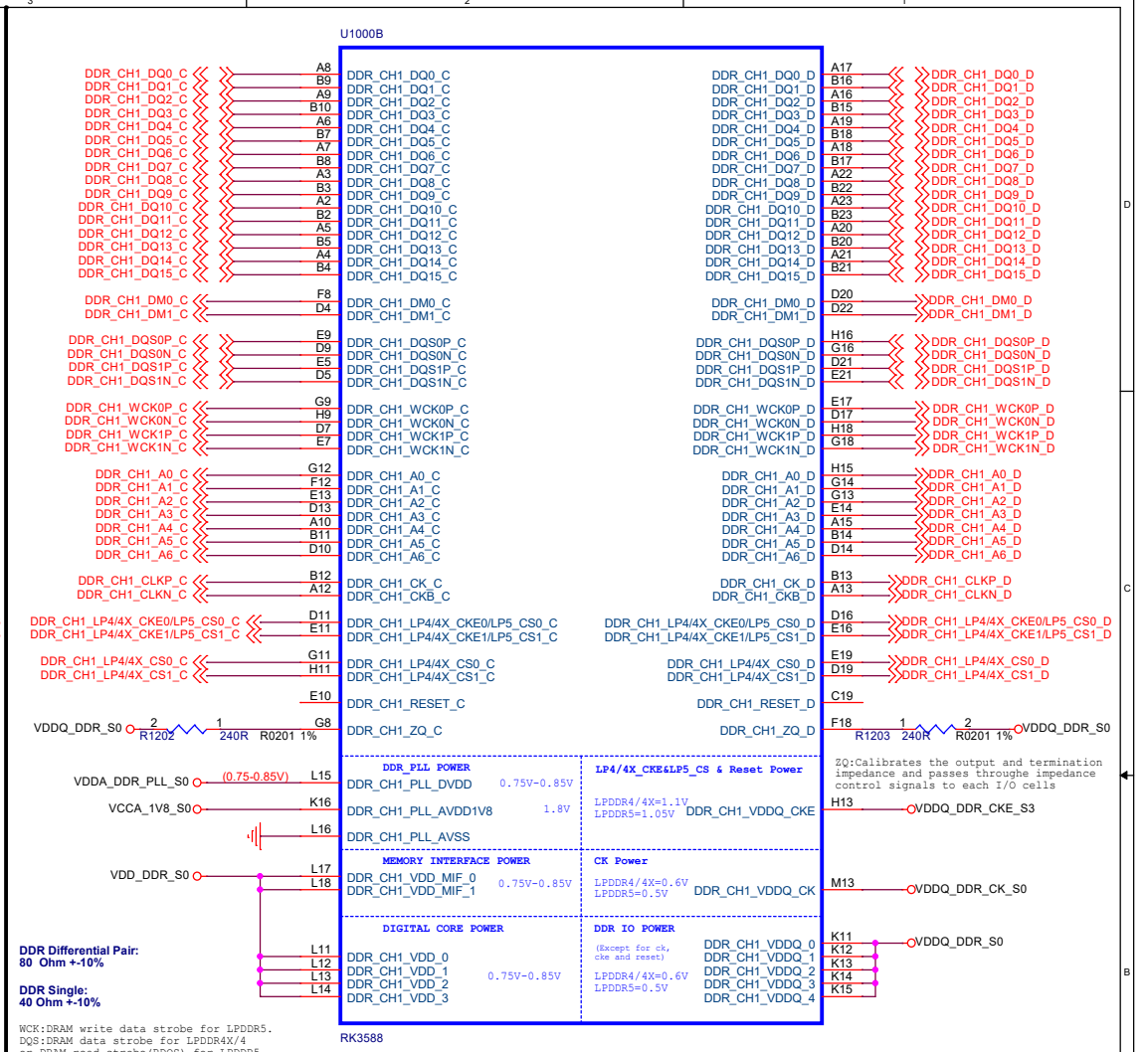
RK3588_F(PMUIO2)



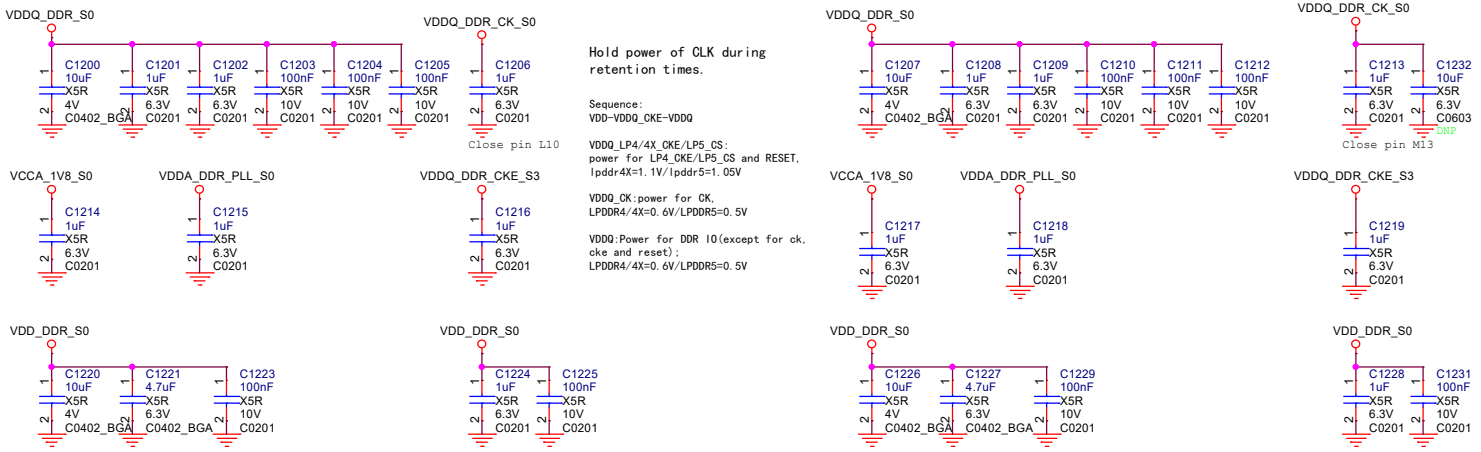
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	11.RK3588_OSC/PLL/PMUIO		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	11 of 99



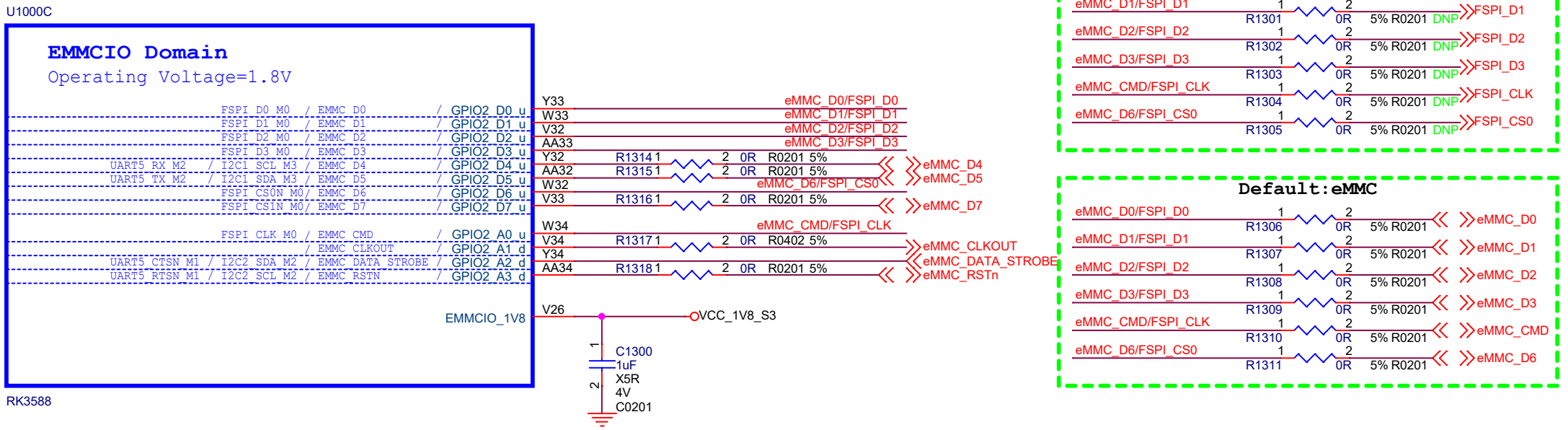


DDR FILTER

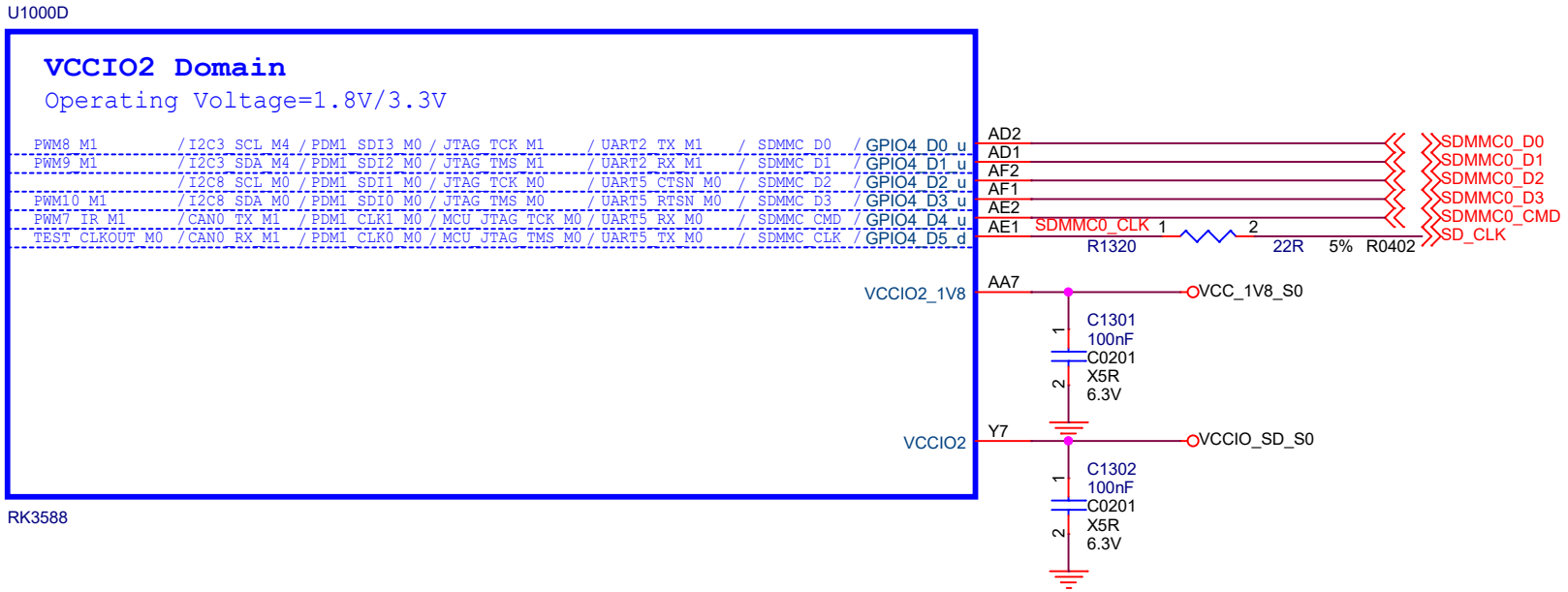


Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	12.RK3588 DDR Controler		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	12 of 99

RK3588_C(EMMCIO Domain)



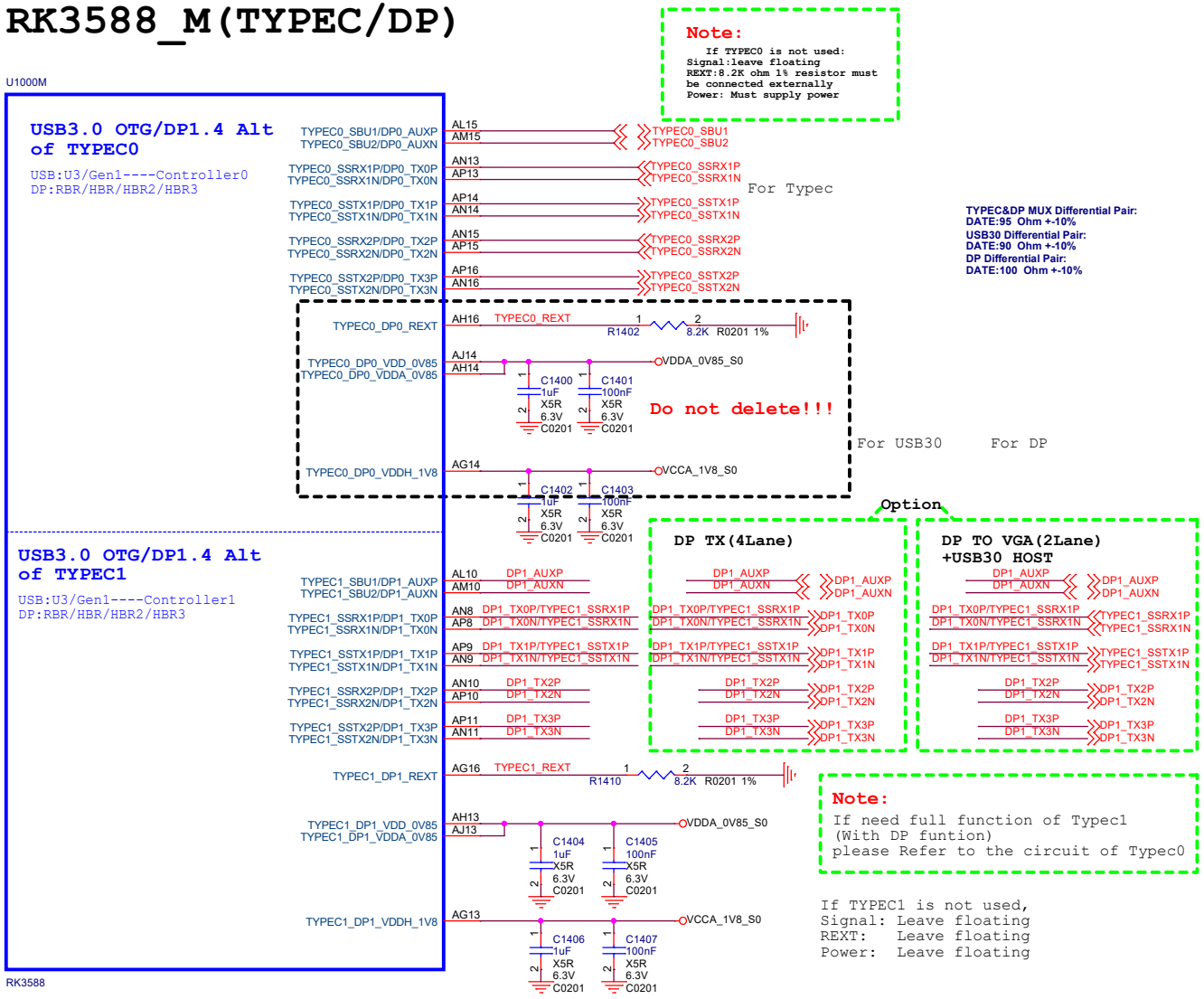
RK3588_D(VCCIO2 Domain)



Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	13.RK3588_Flash/SD Controller		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	13 of 99

RK3588_M(TYPEC/DP)



Note:
If TYPEC0 is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

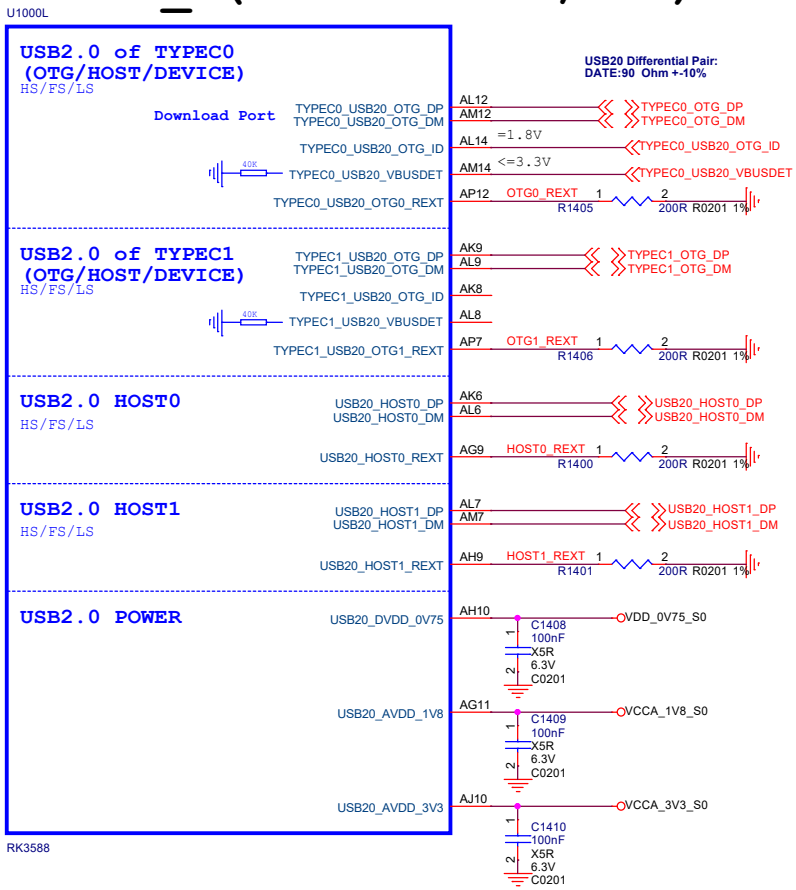
Note:
If need full function of Typec1 (With DP funtion) please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*TYPEC_SSTX1P/1N&TYPEC_SSRX1P/1N or TYPEC_SSTX2P/2N&TYPEC_SSRX2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1 DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3 DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)



Note:
TYPEC0_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

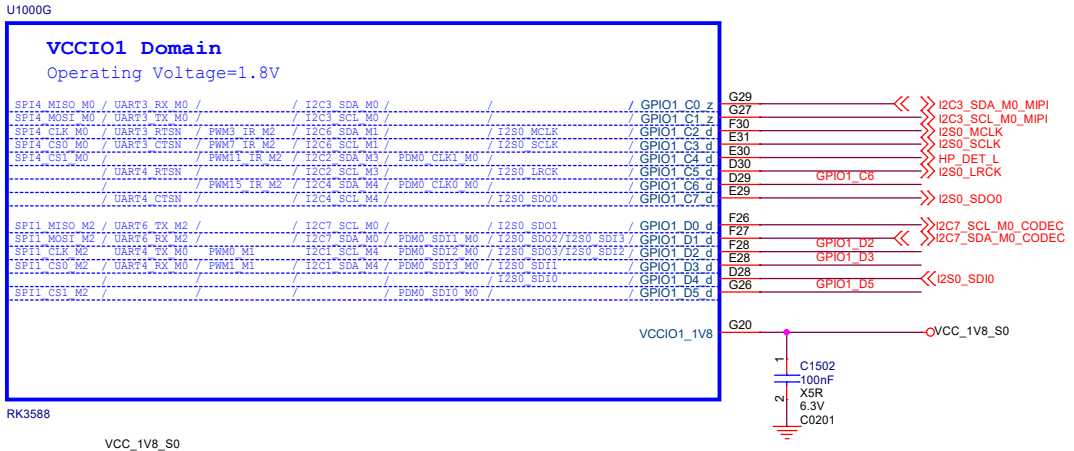
TYPEC1_USB20_OTG:
If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating
Power:Leave floating

USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating
Power:Leave floating

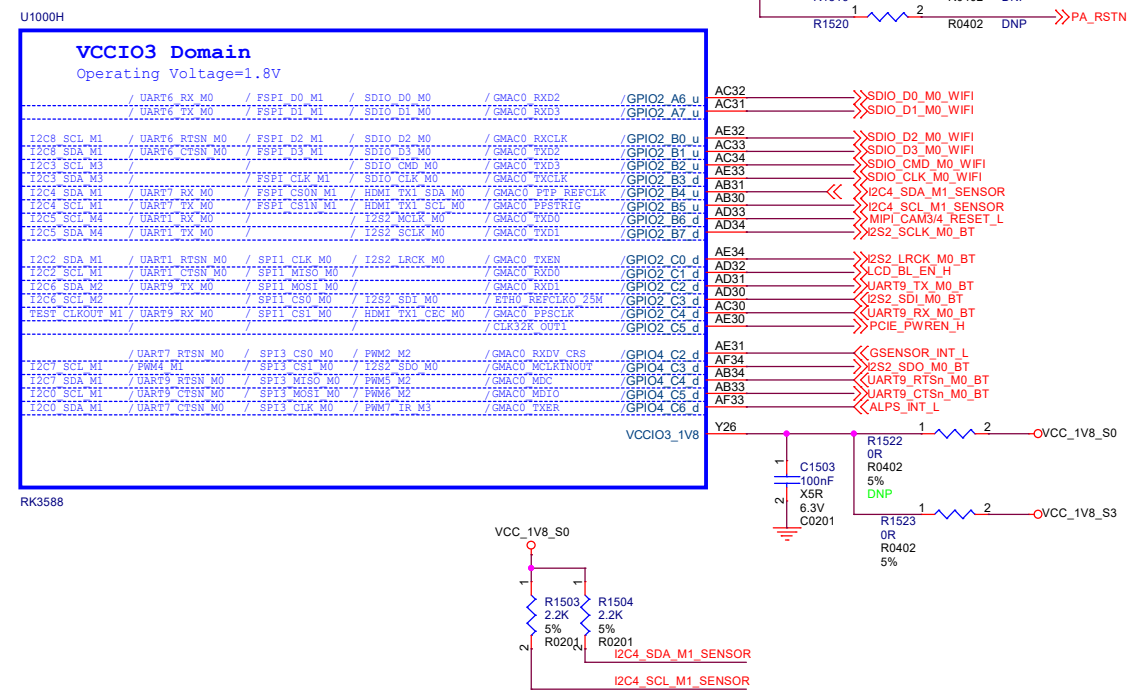
Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	14.RK3588_USB30/USB20_Ctrl		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	14 of 99

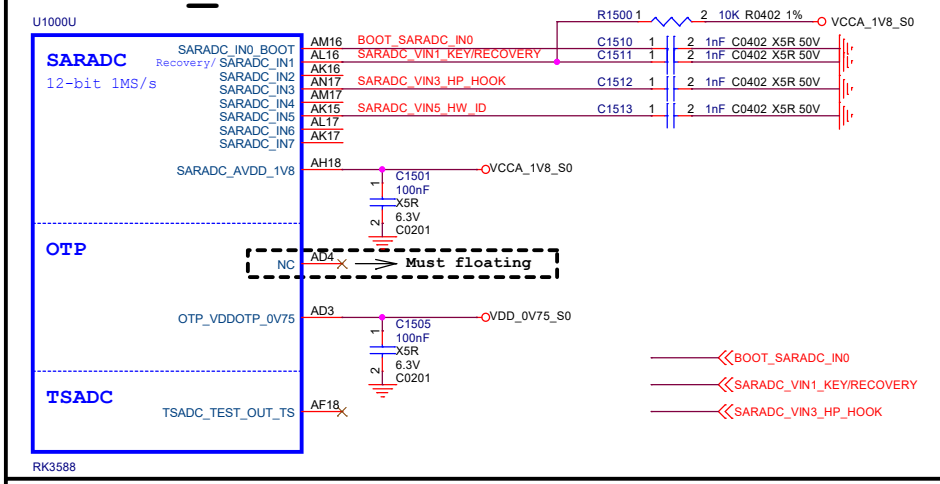
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

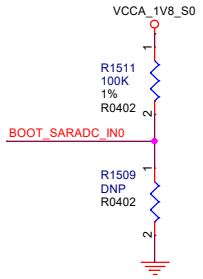


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

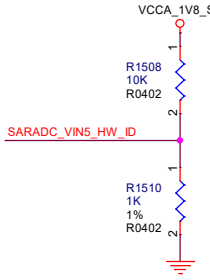


TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	100K	51K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	100K	200K	2730	1.2V	V5.0
LEVEL6	100K	499K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	15.RK3588_SARADC/1.8V Only GPIO		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	15 of 99

RK3588_Q/R(MIPI_D/C_PHY0/1)

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C — AN26 — MIPI_DPHY0_TX_CLKP
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B — AP26 — MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B — AN24 — MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A — AP24 — MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A — AN25 — MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C — AP25 — MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B — AN27 — MIPI_DPHY0_TX_D2P
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A — AP27 — MIPI_DPHY0_TX_D2N
MIPI_DPHY0_TX_D3P /NO_USE_AN28 — AN28 — MIPI_DPHY0_TX_D3P
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C — AP28 — MIPI_DPHY0_TX_D3N

MIPI DPHY Differential Pair: 100 Ohm +-10%

MIPI CPHY Single: 50 Ohm +-10%

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
此D-PHY使用受限!!!
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C — AN32 — MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B — AP31 — MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B — AN29 — MIPI_DPHY0_RX_D0P
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A — AP29 — MIPI_DPHY0_RX_D0N
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A — AN30 — MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C — AP30 — MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B — AN33 — MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A — AP32 — MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_D3P /NO_USE_AN34 — AN34 — MIPI_DPHY0_RX_D3P
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C — AP33 — MIPI_DPHY0_RX_D3N

Note:
Suggest Using 1/2 lane mode, Using 4Lane is limited, Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG — AF20 — C1600 1uF — C0201 X5R 4V
MIPI_D/C_PHY0_VDD — AG20 — VDD_0V75_S0
C1602 100nF X5R 6.3V C0201
C1601 1uF X5R 6.3V C0201 C-PHY 5.7Gbps 0.85V D-PHY 2.5Gbps & C-PHY 5.7Gbps 0.75V
MIPI_D/C_PHY0_VDD_1V2 — AH20 — VDDA_1V2_S0
C1603 1uF X5R 6.3V C0201
MIPI_D/C_PHY0_VDD_1V8 — AJ20 — VCC_1V8_S0
C1605 1uF X5R 6.3V C0201

RK3588

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C — AN20 — MIPI_DPHY1_TX_CLKP
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B — AP20 — MIPI_DPHY1_TX_CLKN
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B — AN18 — MIPI_DPHY1_TX_D0P
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A — AP18 — MIPI_DPHY1_TX_D0N
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A — AN19 — MIPI_DPHY1_TX_D1P
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C — AP19 — MIPI_DPHY1_TX_D1N
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B — AN21 — MIPI_DPHY1_TX_D2P
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A — AP21 — MIPI_DPHY1_TX_D2N
MIPI_DPHY1_TX_D3P /NO_USE_AN22 — AN22 — MIPI_DPHY1_TX_D3P
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C — AP22 — MIPI_DPHY1_TX_D3N

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
此D-PHY使用受限!!!
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C — AK20 — MIPI_DPHY1_RX_CLKP
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B — AL20 — MIPI_DPHY1_RX_CLKN
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B — AK18 — MIPI_DPHY1_RX_D0P
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A — AL18 — MIPI_DPHY1_RX_D0N
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A — AK19 — MIPI_DPHY1_RX_D1P
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C — AL19 — MIPI_DPHY1_RX_D1N
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B — AK21 — MIPI_DPHY1_RX_D2P
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A — AL21 — MIPI_DPHY1_RX_D2N
MIPI_DPHY1_RX_D3P /NO_USE_AK22 — AK22 — MIPI_DPHY1_RX_D3P
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C — AL22 — MIPI_DPHY1_RX_D3N

Note:
Suggest Using 1/2 lane mode, Using 4Lane is limited, Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG — AF19 — C1608 1uF — C0201 X5R 4V
MIPI_D/C_PHY1_VDD — AG19 — VDD_0V75_S0
C1609 1uF X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V2 — AH19 — VDDA_1V2_S0
C1611 100nF X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V8 — AJ19 — VCC_1V8_S0
C1613 1uF X5R 6.3V C0201

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588

RK3588_P(MIPI_DPHY_CSI_RX_PHY)

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N — AJ33/AJ34 — MIPI_CSI0_RX_CLK0P/MIPI_CSI0_RX_CLK0N
MIPI_CSI0_D0P/MIPI_CSI0_D0N — AG33/AG34 — MIPI_CSI0_RX_D0P/MIPI_CSI0_RX_D0N
MIPI_CSI0_D1P/MIPI_CSI0_D1N — AH33/AH34 — MIPI_CSI0_RX_D1P/MIPI_CSI0_RX_D1N
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N — AM33/AM34
MIPI_CSI0_D2P/MIPI_CSI0_D2N — AK33/AK34 — MIPI_CSI0_RX_D2P/MIPI_CSI0_RX_D2N
MIPI_CSI0_D3P/MIPI_CSI0_D3N — AL33/AL34 — MIPI_CSI0_RX_D3P/MIPI_CSI0_RX_D3N
MIPI_CSI0_AVCC0V75 — AB25 — VDD_0V75_S0
C1616 100nF X5R 6.3V C0201
C1615 1uF X5R 6.3V C0201
MIPI_CSI0_AVCC1V8 — AB26 — VCC_1V8_S0
C1617 1uF X5R 6.3V C0201

MIPI CSI Differential Pair: 100 Ohm +-10%

Note:
建义优先使用U1000P这个模块的DPHY CSI_RX。

First use the DPHY_CSI_RX controller of U1000P.

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N — AJ31/AJ32 — MIPI_CSI1_RX_CLK0P/MIPI_CSI1_RX_CLK0N
MIPI_CSI1_D0P/MIPI_CSI1_D0N — AG31/AG32 — MIPI_CSI1_RX_D0P/MIPI_CSI1_RX_D0N
MIPI_CSI1_D1P/MIPI_CSI1_D1N — AH31/AH32 — MIPI_CSI1_RX_D1P/MIPI_CSI1_RX_D1N
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N — AM31/AM32
MIPI_CSI1_D2P/MIPI_CSI1_D2N — AK31/AK32 — MIPI_CSI1_RX_D2P/MIPI_CSI1_RX_D2N
MIPI_CSI1_D3P/MIPI_CSI1_D3N — AL31/AL32 — MIPI_CSI1_RX_D3P/MIPI_CSI1_RX_D3N
MIPI_CSI1_AVCC0V75 — AA25 — VDD_0V75_S0
C1619 1uF X5R 6.3V C0201
MIPI_CSI1_AVCC1V8 — AA26 — VCC_1V8_S0
C1621 100nF X5R 6.3V C0201

RK3588

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

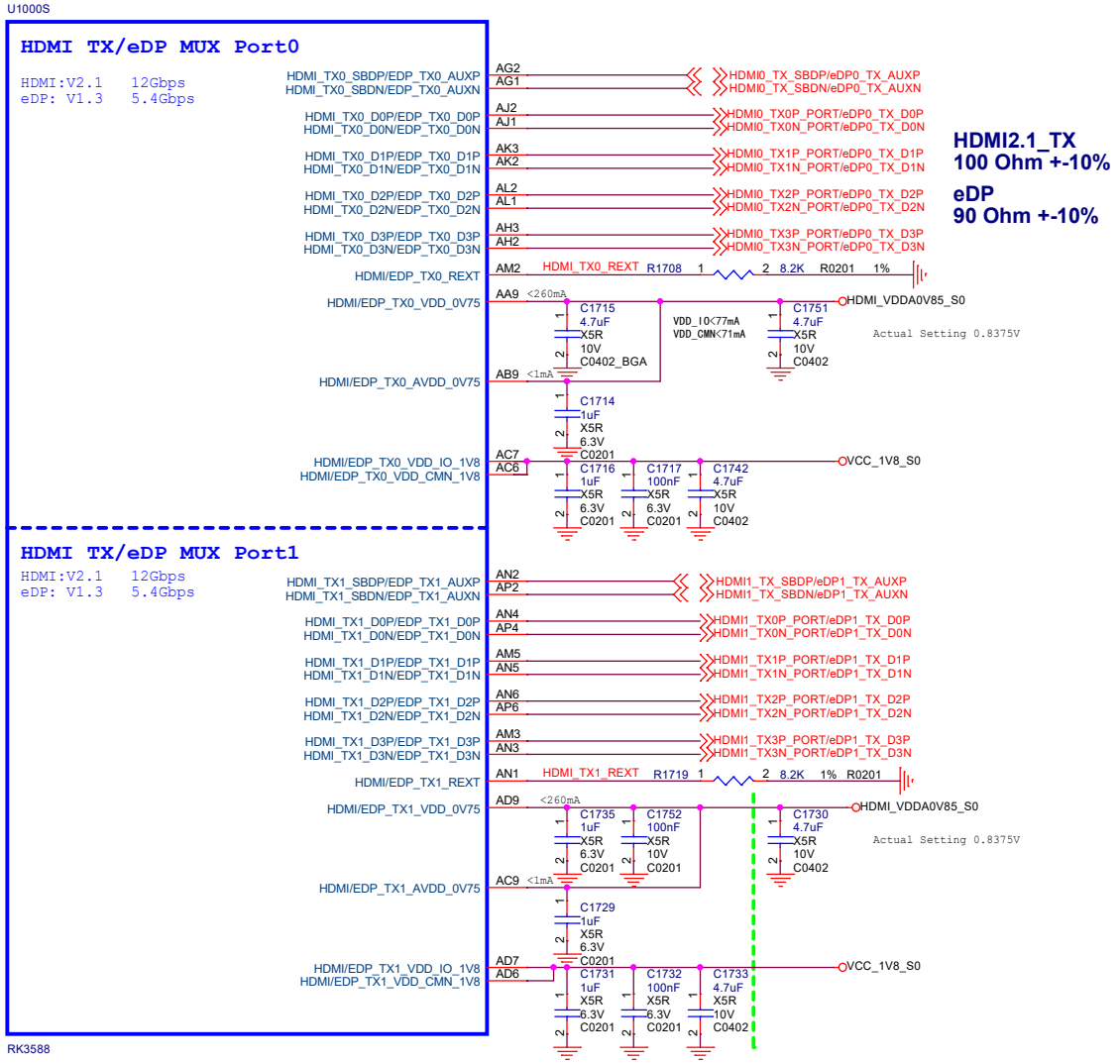
Note:
If not used:
Signal:leave floating
Power: Floating

Rockchip Confidential

Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH			
File:	16.RK3588_MIPI Interface			
Date:	Monday, February 20, 2023		Rev:	V1.4
Designed by:	RZF	Reviewed by:	Sheet:	16 of 99

RK3588_S(HDMI2.1 TX)

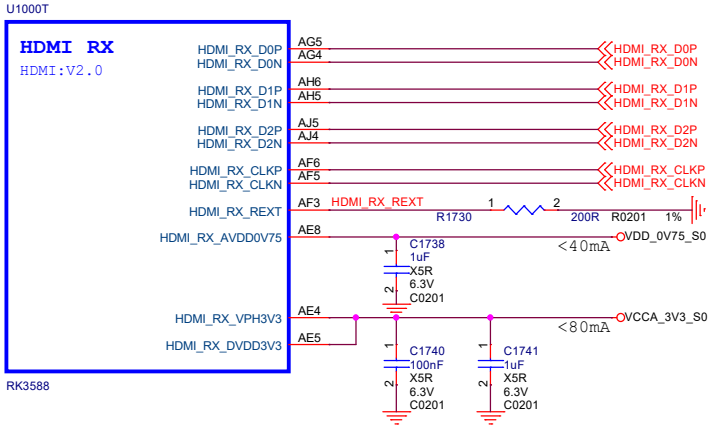
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



Note:
If not used:
Signal:leave floating
Power: Floating

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	17.RK3588_HDMI/eDP Interface				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	17 of 99

RK3588_N(PCIE20)

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2 1Lane(RC)--4(1L2)

SATA30 HOST Controller0

MUX

input or output

PCIE20_0_REFCLKP / PCIE20_0_REFCLKN — L32 / L33

PCIE20_0_TXP/SATA30_0_TXP — M34 → PCIE20_0_TXP/SATA30_0_TXP

PCIE20_0_TXN/SATA30_0_TXN — M33 → PCIE20_0_TXN/SATA30_0_TXN

PCIE20_0_RXP/SATA30_0_RXP — N33 → PCIE20_0_RXP/SATA30_0_RXP

PCIE20_0_RXN/SATA30_0_RXN — N34 → PCIE20_0_RXN/SATA30_0_RXN

PCIE20_SATA30_0_AVDD_0V85 — M28 → VDDA_0V85_S0

C1810 10uF X5R 4V C0402

PCIe20x1_2 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin AH24/AJ24/AG23
Option1 :Pin AJ25/AJ28/AK24

PCIE20_SATA30_0_AVDD_1V8 — M27 → VCCA_1V8_S0

C1808 1uF X5R 4V C0201

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0 1Lane(RC)--2(1L0)

SATA30 HOST Controller1

MUX

input or output

PCIE20_1_REFCLKP / PCIE20_1_REFCLKN — H32 / H33 → PCIE20_1_REFCLKP / PCIE20_1_REFCLKN

PCIE20_1_TXP/SATA30_1_TXP — K33 → PCIE20_1_TXP/SATA30_1_TXP

PCIE20_1_TXN/SATA30_1_TXN — K34 → PCIE20_1_TXN/SATA30_1_TXN

PCIE20_1_RXP/SATA30_1_RXP — J33 → PCIE20_1_RXP/SATA30_1_RXP

PCIE20_1_RXN/SATA30_1_RXN — J34 → PCIE20_1_RXN/SATA30_1_RXN

PCIE20_SATA30_1_AVDD_0V85 — L28 → VDDA_0V85_S0

C1818 100nF X5R 6.3V C0201

PCIe30x1_0 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin R30/T31/P30
Option1 :Pin AL28/AL29/AK27
Option2: Pin D27/E25/E24

PCIE20_SATA30_1_AVDD_1V8 — L27 → VCCA_1V8_S0

C1816 100nF X5R 6.3V C0201

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1 1Lane(RC)--3(1L1)

SATA30 HOST Controller2

USB30 HOST Controller2

MUX

input or output

PCIE20_2_REFCLKP / PCIE20_2_REFCLKN — G31 / G30 → PCIE20_2_REFCLKP / PCIE20_2_REFCLKN

PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP — H30 → PCIE20_2_TXP/SATA30_2_TXP

PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN — H29 → PCIE20_2_TXN/SATA30_2_TXN

PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP — J31 → PCIE20_2_RXP/SATA30_2_RXP

PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN — J30 → PCIE20_2_RXN/SATA30_2_RXN

PCIE20_SATA30_USB30_2_AVDD_0V85 — K28 → VDDA_0V85_S0

C1806 1uF X5R 4V C0201

PCIe30x1_1 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin R29/P29/T28
Option1 :Pin AL30/AK30/AM29
Option2: Pin A25/A24/C25

PCIE20_SATA30_USB30_2_AVDD_1V8 — K27 → VCCA_1V8_S0

C1804 1uF X5R 4V C0201

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588

Note:
If not used:
Signal:leave floating
Power: Floating

CLK Differential Pair:
100 Ohm±10%

DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

Note:
每个SATA PORT最多只能扩展5个SATA，
不支持二级扩展。
Each sata port can only expand 5 sata port at most,No support level-2 expand.

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4 4Lane(DM)--0(4L)

PCIe30x1_0 1Lane(RC)--2(1L0) — PCIE20/SATA30 MUX1

PCIe30x2 2Lane(RC)--1(2L)

PCIe30x1_1 1Lane(RC)--3(1L1) — PCIE20/SATA30/USB30 MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input PCIE30_PORT0_REF_CLKP / PCIE30_PORT0_REF_CLKN — E33 / E34 → PCIE30_PORT0_REFCLKP_IN / PCIE30_PORT0_REFCLKN_IN

Lane0

PCIE30_PORT0_TX0P / PCIE30_PORT0_TX0N — D32 / D33 → PCIE30_PORT0_TX0P / PCIE30_PORT0_TX0N

PCIE30_PORT0_RX0P / PCIE30_PORT0_RX0N — G33 / G34 → PCIE30_PORT0_RX0P / PCIE30_PORT0_RX0N

Lane1

PCIE30_PORT0_TX1P / PCIE30_PORT0_TX1N — C33 / C34 → PCIE30_PORT0_TX1P / PCIE30_PORT0_TX1N

PCIE30_PORT0_RX1P / PCIE30_PORT0_RX1N — F32 / F33 → PCIE30_PORT0_RX1P / PCIE30_PORT0_RX1N

PCIE30_PORT0_RESREF — B34 PCIE30_0_REF — R1801 R0201 1 2 200R 1%

PCIE30_PORT0_AVDD0V75 — G24 → VDD_0V75_S0

C1802 1uF X5R 6.3V C0201

C1803 4.7uF X5R 10V C0402

PCIE30_PORT0_AVDD1V8 — G23 → VCCA_1V8_S0

C1800 1uF X5R 6.3V C0201

C1801 4.7uF X5R 10V C0402

PCIE30 PORT1

input PCIE30_PORT1_REF_CLKP / PCIE30_PORT1_REF_CLKN — A28 / B28 → PCIE30_PORT1_REFCLKP_IN / PCIE30_PORT1_REFCLKN_IN

Lane0

PCIE30_PORT1_TX0P / PCIE30_PORT1_TX0N — B30 / A30 → PCIE30_PORT1_TX2P / PCIE30_PORT1_TX2N

PCIE30_PORT1_RX0P / PCIE30_PORT1_RX0N — B32 / A32 → PCIE30_PORT1_RX2P / PCIE30_PORT1_RX2N

Lane1

PCIE30_PORT1_TX1P / PCIE30_PORT1_TX1N — C29 / B29 → PCIE30_PORT1_TX3P / PCIE30_PORT1_TX3N

PCIE30_PORT1_RX1P / PCIE30_PORT1_RX1N — C31 / B31 → PCIE30_PORT1_RX3P / PCIE30_PORT1_RX3N

PCIE30_PORT1_RESREF — A33 PCIE30_1_REF — R1807 R0201 1 2 200R 1%

PCIE30_PORT1_AVDD0V75 — H24 → VDD_0V75_S0

C1814 1uF X5R 6.3V C0201

C1815 4.7uF X5R C0402 10V

PCIE30_PORT1_AVDD1V8 — H23 → VCCA_1V8_S0

C1812 100nF X5R 6.3V C0201

C1813 4.7uF X5R 10V C0402

RK3588

CLK Differential Pair:
100 Ohm ±10%

DATA Differential Pair:
PCIE30: 85 Ohm ±10%

PCIe30x4 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin V31/T29/W31
Option1 :Pin AJ26/AL26/AJ27
Option2: Pin AH25/AH26/AG26
Option3: Pin D25/C27/D26

Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	18.RK3588_PCIE30/PCIE20/SATA30				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	18 of 99

RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0 / SPI4_MISO_M1 / I2C6_SDA_M4 / FSPI_D0_M2 / I2S3_MCLK / SDIO_D0_M1 / GMAC1_TXD2 / GPIO3_A0_u

AUDDSM_LN / SPI4_MOSI_M1 / PWM11_IR_M0 / I2C6_SCL_M4 / FSPI_D1_M2 / I2S3_SCLK / SDIO_D1_M1 / GMAC1_TXD3 / GPIO3_A1_u

AUDDSM_LP / SPI4_CLK_M1 / UART8_TX_M1 / FSPI_D2_M2 / I2S3_LRCK / SDIO_D2_M1 / GMAC1_RXD2 / GPIO3_A2_u

AUDDSM_RN / SPI4_CS0_M1 / UART8_RX_M1 / FSPI_D3_M2 / I2S3_SDO / SDIO_D3_M1 / GMAC1_RXD3 / GPIO3_A3_u

AUDDSM_RP / SPI4_CS1_M1 / UART8_RTSN_M1 / I2S3_SDI / SDIO_CMD_M1 / GMAC1_TXCLK / GPIO3_A4_d

/ MIPI_CAMERA0_CLK_M1 / UART8_CTSN_M1 / I2C4_SDA_M0 / FSPI_CLK_M2 / SDIO_CLK_M1 / GMAC1_RXCLK / GPIO3_A5_d

/ MIPI_CAMERA1_CLK_M1 / I2C4_SCL_M0 / ETH1_REFCLKO_25M / GPIO3_A6_d

PWM8_M0 / MIPI_CAMERA2_CLK_M1 / GMAC1_RXD0 / GPIO3_A7_u

PWM9_M0 / MIPI_CAMERA3_CLK_M1 / GMAC1_RXD1 / GPIO3_B0_u

PWM2_M1 / MIPI_CAMERA4_CLK_M1 / UART2_TX_M2 / GMAC1_RXDV_CRS / GPIO3_B1_d

PWM3_IR_M1 / UART2_RX_M2 / I2S2_SDI_M1 / GMAC1_TXER / GPIO3_B2_d

/ UART2_RTSN / I2S2_SDO_M1 / GMAC1_TXD0 / GPIO3_B3_u

/ UART2_CTSN / I2S2_MCLK_M1 / GMAC1_TXD1 / GPIO3_B4_u

PWM12_M0 / CAN1_RX_M0 / UART3_TX_M1 / I2S2_SCLK_M1 / GMAC1_TXEN / GPIO3_B5_u

PWM13_M0 / CAN1_TX_M0 / UART3_RX_M1 / I2S2_LRCK_M1 / GMAC1_MCLKINOUT / GPIO3_B6_d

/ I2C3_SCL_M1 / SPI1_MOSI_M1 / HDMI_TX1_HPD_M1 / GMAC1_PTP_REF_CLK / GPIO3_B7_d

/ UART7_TX_M1 / I2C3_SDA_M1 / SPI1_MISO_M1 / GMAC1_PPSTRIG / GPIO3_C0_d

/ PCIE30X2_BUTTON_RSTN / UART7_RX_M1 / SPI1_CLK_M1 / GMAC1_PPSCLK / GPIO3_C1_d

PWM14_M0 / UART7_RTSN_M1 / I2C8_SCL_M4 / SPI1_CS0_M1 / MIPI_TE0 / GMAC1_MDC / GPIO3_C2_d

PWM15_IR_M0 / UART7_CTSN_M1 / I2C8_SDA_M4 / SPI1_CS1_M1 / MIPI_TE1 / GMAC1_MDIO / GPIO3_C3_d

CAN2_RX_M0 / PCIE30X4_CLKREQN_M2 / UART5_TX_M1 / FSPI_CS0N_M2 / SPI3_CS0_M3 / HDMI_TX1_CEC_M2 / CIF_D8 / GPIO3_C4_u

CAN2_TX_M0 / PCIE30X4_WAKEN_M2 / UART5_RX_M1 / FSPI_CS1N_M2 / SPI3_CS1_M3 / HDMI_TX1_SDA_M1 / CIF_D9 / GPIO3_C5_u

/ PCIE30X4_PERSTN_M2 / SPI3_MISO_M3 / HDMI_TX1_SCL_M1 / CIF_D10 / GPIO3_C6_u

/ PCIE20X1_2_CLKREQN_M0 / I2C5_SCL_M0 / SPI3_MOSI_M3 / HDMI_TX0_SCL_M2 / CIF_D11 / GPIO3_C7_u

PWM8_M2 / PCIE20X1_2_WAKEN_M0 / UART4_RX_M1 / I2C5_SDA_M0 / SPI3_CLK_M3 / HDMI_TX0_SDA_M2 / CIF_D12 / GPIO3_D0_u

PWM9_M2 / PCIE20X1_2_PERSTN_M0 / UART4_TX_M1 / SPI0_MISO_M3 / HDMI_RX_CEC_M1 / CIF_D13 / GPIO3_D1_d

/ PCIE30X2_CLKREQN_M2 / UART9_RTSN_M2 / I2C7_SCL_M2 / SPI0_MOSI_M3 / HDMI_RX_SCL_M1 / CIF_D14 / GPIO3_D2_d

PWM10_M2 / PCIE30X2_WAKEN_M2 / UART9_CTSN_M2 / I2C7_SDA_M2 / SPI0_CLK_M3 / HDMI_RX_SDA_M1 / CIF_D15 / GPIO3_D3_d

/ PCIE30X2_PERSTN_M2 / UART9_RX_M2 / SPI0_CS0_M3 / HDMI_RX_HPDOUT_M1 / HDMI_TX0_HPD_M1 / MCU_JTAG_TCK_M1 / GPIO3_D4_d

PWM11_IR_M3 / PCIE30X4_BUTTON_RSTN / UART9_TX_M2 / SPI0_CS1_M3 / DP1_HPDIN_M0 / MCU_JTAG_TMS_M1 / GPIO3_D5_d

AA29 MAC1_TXD2 R1900 1 2 0R 5% R0402 GMAC1_TXD2

AA30 MAC1_TXD3 R1901 1 2 0R 5% R0402 GMAC1_TXD3

AD27 GMAC1_RXD2

AE27 GMAC1_RXD3

AD28 MAC1_TXCLK R1902 1 2 0R 5% R0402 GMAC1_TXCLK

AH30 GMAC1_RXCLK

AH27 ETH1_REFCLKO_25M

AG29 GMAC1_RXD0

AG28 GMAC1_RXD1

AH29 GMAC1_RXDV_CRS

AE28 USB_HUB_RESET

AC28 MAC1_TXD0 R1903 1 2 0R 5% R0402 GMAC1_TXD0

AC29 MAC1_TXD1 R1904 1 2 0R 5% R0402 GMAC1_TXD1

AD29 MAC1_TXEN R1905 1 2 0R 5% R0402 GMAC1_TXEN

AE29 MAC1_MCLKINOUT R1906 1 2 0R 5% R0402 GMAC1_MCLKINOUT

AA28 GMAC1_RSTn_L

Y29 TP_INT_L

Y27 TP_RST_L

Y31 GMAC1_MDC

Y30 R1907 1 2 0R 5% R0402 GMAC1_MDIO

AH26 HDMITX1_CEC_M2

AH25 HDMITX1_SDA_M1

AG26 HDMITX1_SCL_M1

AJ24 I2C5_SCL_M0_TP

AH24 I2C5_SDA_M0_TP

AG23 GPIO3_D1_d/HDMI_RX_CEC

AG25 HDMI_RX_SCL_M1

AG24 HDMI_RX_SDA_M1

AA27 GPIO3_D4_d/HDMIIRX_HPDOUT_H

AB28 DP1_HPDIN_M0

VCCIO5_1V8

W25 C1903 100nF X5R 6.3V C0201 VCC_1V8_S0

VCCIO5

W26 C1902 100nF X5R 6.3V C0201 VCC_3V3_S0

RK3588

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

/ SPI0_MISO_M1 / UART9_RTSN_M1 / / I2S1_MCLK_M0 / PCIE30X1_1_CLKREQN_M1 / BT1120_D0 / CIF_D0 / GPIO4_A0_d

/ SPI0_MOSI_M1 / UART9_CTSN_M1 / / I2S1_SCLK_M0 / PCIE30X1_1_WAKEN_M1 / BT1120_D1 / CIF_D1 / GPIO4_A1_d

/ SPI0_CLK_M1 / / / I2S1_LRCK_M0 / PCIE30X1_1_PERSTN_M1 / BT1120_D2 / CIF_D2 / GPIO4_A2_d

/ / UART0_TX_M2 / / / PCIE30X1_0_CLKREQN_M1 / BT1120_D3 / CIF_D3 / GPIO4_A3_d

/ SPI2_MISO_M1 / UART0_RX_M2 / I2C3_SCL_M2 / / / PCIE30X1_0_WAKEN_M1 / BT1120_D4 / CIF_D4 / GPIO4_A4_d

/ SPI2_MOSI_M1 / UART3_TX_M2 / I2C3_SDA_M2 / I2S1_SDI0_M0 / PCIE30X1_0_PERSTN_M1 / BT1120_D5 / CIF_D5 / GPIO4_A5_d

/ SPI2_CLK_M1 / UART3_RX_M2 / I2C5_SCL_M2 / I2S1_SDI1_M0 / PCIE30X2_CLKREQN_M1 / BT1120_D6 / CIF_D6 / GPIO4_A6_d

/ SPI2_CS0_M1 / / I2C5_SDA_M2 / I2S1_SDI2_M0 / PCIE30X2_WAKEN_M1 / BT1120_D7 / CIF_D7 / GPIO4_A7_d

/ SPI2_CS1_M1 / UART8_TX_M0 / I2C6_SDA_M3 / I2S1_SDI3_M0 / PCIE30X2_PERSTN_M1 / BT1120_CLKOUT / CIF_CLKIN / GPIO4_B0_d

SATA2_ACT_LED_M0 / SPDIF1_TX_M1 / SPI0_CS1_M1 / UART8_RX_M0 / I2C6_SCL_M3 / I2S1_SDO0_M0 / PCIE30X1_0_BUTTON_RSTN / / MIPI_CAMERA5_CLK_M0 / GPIO4_B1_u

CAN1_RX_M1 / PWM14_M1 / SPI0_CS0_M1 / UART8_RTSN_M0 / I2C7_SCL_M3 / I2S1_SDO1_M0 / PCIE30X1_1_BUTTON_RSTN / BT1120_D8 / CIF_HREF / GPIO4_B2_u

CAN1_TX_M1 / PWM15_IR_M1 / UART8_CTSN_M0 / I2C7_SDA_M3 / I2S1_SDO2_M0 / PCIE20X1_2_BUTTON_RSTN / BT1120_D9 / CIF_VSYNC / GPIO4_B3_u

SPDIFP0_TX_M1 / PWM11_IR_M1 / DP0_HPDIN_M0 / UART9_TX_M1 / / I2S1_SDO3_M0 / PCIE30X4_CLKREQN_M1 / BT1120_D10 / CIF_CLKOUT / GPIO4_B4_u

SATA1_ACT_LED_M0 / PWM12_M1 / SPI3_MISO_M1 / UART9_RX_M1 / / HDMI_RX_CEC_M0 / PCIE30X4_WAKEN_M1 / BT1120_D11 / / GPIO4_B5_d

SATA0_ACT_LED_M0 / PWM13_M1 / SPI3_MOSI_M1 / / I2C5_SCL_M1 / HDMI_RX_HPDOUT_M0 / PCIE30X4_PERSTN_M1 / BT1120_D12 / / GPIO4_B6_d

/ / SPI3_CLK_M1 / / I2C5_SDA_M1 / HDMI_TX0_SCL_M0 / PCIE20X1_2_CLKREQN_M1 / BT1120_D13 / / GPIO4_B7_u

/ / SPI3_CS0_M1 / / I2C8_SCL_M3 / HDMI_TX0_SDA_M0 / PCIE20X1_2_WAKEN_M1 / BT1120_D14 / / GPIO4_C0_u

SPDIF1_TX_M2 / PWM6_M1 / SPI3_CS1_M1 / / I2C8_SDA_M3 / HDMI_TX0_CEC_M0 / PCIE20X1_2_PERSTN_M1 / BT1120_D15 / / GPIO4_C1_d

AK30 PCIEX1_1_CLKREQn_M1_L

AL30 PCIEX1_1_WAKEn_M1_L/GPIO4_A1

AM29 PCIEX1_1_PERSTn_M1_L

AL29 SPK_CTL_H

AL28 PHONE_CTL

AK27 SDMMC_PWREN

AL27 TYPEC0_SBU1_DC

AM27 TYPEC0_SBU2_DC

AK26 USB_HOST_PWREN_H

AL24 HDMI0_TX_ON_H

AK25 HDMI1_TX_ON_H

AM25 PCIE30X4_PRSNT_L/GPIO4_B3

AL26 PCIE30X4_CLKREQn_M1_L

AJ26 PCIE30X4_WAKEn_M1_L/GPIO4_B5

AJ27 PCIE30X4_PERSTn_M1_L

AJ28 HDMITX0_SCL_M0

AJ25 HDMITX0_SDA_M0

AK24 HDMITX0_CEC_M0

VCCIO6_1V8

AC25 C1909 100nF X5R 6.3V C0201 VCC_1V8_S0

VCCIO6

AC26 C1908 100nF X5R 6.3V C0201 VCC_3V3_S0

RK3588

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

/ / /SPI4_MISO_M2 /PCIE30X1_1_CLKREQN_M2/ DP0_HPDIN_M2 / I2C2_SDA_M4 / UART6_RX_M1 /GPIO1_A0_d

SATA1_ACT_LED_M1 / / /SPI4_MOSI_M2 /PCIE30X1_1_WAKEN_M2 / DP1_HPDIN_M2 / I2C2_SCL_M4 / UART6_TX_M1 /GPIO1_A1_d

/ PWM0_M2 /SPI4_CLK_M2 / / VOP_POST_EMPTY / I2C4_SDA_M3 / UART6_RTSN_M1 /GPIO1_A2_d

/ PWM1_M2 /SPI4_CS0_M2 / / HDMI_TX1_SDA_M2 / I2C4_SCL_M3 / UART6_CTSN_M1 /GPIO1_A3_d

/ / /SPI2_MISO_M0 / / HDMI_TX1_SCL_M2 / / / /GPIO1_A4_d

/ / /SPI2_MOSI_M0 / / HDMI_TX0_HPD_M0 / / / /GPIO1_A5_d

/ / /SPI2_CLK_M0 / / HDMI_TX1_HPD_M0 / / / /GPIO1_A6_d

/ PWM3_IR_M3 /SPI2_CS0_M0 /PCIE30X1_1_PERSTN_M2 / / PDM1_SDI0_M1 / /GPIO1_A7_u

/ / /SPI2_CS1_M0 /PCIE30X4_CLKREQN_M3 / / PDM1_SDI1_M1 / /GPIO1_B0_u

/ / /SPI0_MISO_M2 /PCIE30X4_WAKEN_M3 / / PDM1_SDI2_M1 / /GPIO1_B1_d

/ / /SPI0_MOSI_M2 /PCIE30X4_PERSTN_M3 / / PDM1_SDI3_M1 / UART4_RX_M2 /GPIO1_B2_d

SATA0_ACT_LED_M1 / / /SPI0_CLK_M2 /PCIE30X1_0_WAKEN_M2 / / PDM1_CLK1_M1 / UART4_TX_M2 /GPIO1_B3_d

/ / /SPI0_CS0_M2 /PCIE30X1_0_PERSTN_M2 / / PDM1_CLK0_M1 / UART7_RX_M2 /GPIO1_B4_u

/ / /SPI0_CS1_M2 /PCIE30X1_0_CLKREQN_M2/ / / / UART7_TX_M2 /GPIO1_B5_u

HDMI_RX_HPDOUT_M2/ /SPDIF0_TX_M0 /PCIE30X2_WAKEN_M3 / MIPI_CAMERA1_CLK_M0 / I2C5_SCL_M3 / UART1_TX_M1 /GPIO1_B6_u

SATA2_ACT_LED_M1/ HDMI_RX_CEC_M2 / PWM13_M2 /SPDIF1_TX_M0 /PCIE30X2_PERSTN_M3 / MIPI_CAMERA2_CLK_M0 / I2C5_SDA_M3 / UART1_RX_M1 /GPIO1_B7_u

HDMI_RX_SCL_M2 / PWM14_M2 / / / MIPI_CAMERA3_CLK_M0 / I2C8_SCL_M2 / UART1_RTSN_M1 /GPIO1_D6_u

HDMI_RX_SDA_M2 / PWM15_IR_M3 / /PCIE30X2_CLKREQN_M3 / MIPI_CAMERA4_CLK_M0 / I2C8_SDA_M2 / UART1_CTSN_M1 /GPIO1_D7_u

A24 I2C2_SDA_M4_MIPI

A25 I2C2_SCL_M4_MIPI

A26 MIPI_CAM1_PDN_L

A27 MIPI_CAM1/2_RESET_L

B25 MIPI_CAM2_PDN_L

B26 HDMITX0_HPDIN_M0

C24 HDMITX1_HPDIN_M0

C25 MIPI_CAM3_PDN_L

C27 MIPI_CAM4_PDN_L

D25 MIPI_CAM4_PWREN_H

D26 MIPI_CAM3_PWREN_H

D27 PCIEx1_0_WAKEn_M2_L/GPIO1_B3

E24 PCIEx1_0_PERSTn_M2_L

E25 PCIEx1_0_CLKREQn_M2_L

E26 MIPI_CAM1_CLKOUT

E27 MIPI_CAM2_CLKOUT

F24 MIPI_CAM3_CLKOUT

F25 MIPI_CAM4_CLKOUT

VCCIO4_1V8

H20 C1907 100nF X5R 6.3V C0201 VCC_1V8_S0

VCCIO4

H21

RK3588

PCIE30X4_WAKEn_M1_L/GPIO4_B5 R1908 1 2 0R R0402 5% DNP PCIE30X4_WAKEn_M1_L

R1909 1 2 0R R0402 5% PWM12_M1_FAN

PCIEX1_1_WAKEn_M1_L/GPIO4_A1 R1910 1 2 0R R0402 5% TYPEC5V_PWREN_H

R1911 1 2 0R R0402 5% DNP PCIEX1_1_WAKEn_M1_L

R1912 1 2 0R R0402 5% DNP PCIE30X4_PRSNT_L

PCIE30X4_PRSNT_L/GPIO4_B3 R1913 1 2 0R R0402 5% HG_DISABLE_L

R1914 1 2 0R R0402 5% DNP PCIEx1_0_WAKEn_M2_L

PCIEx1_0_WAKEn_M2_L/GPIO1_B3 R1915 1 2 0R R0402 5% LCD_PWREN_H

R1920 1 2 0R R0402 5% DNP LT6911UXC_INT

GPIO3_D1_d/HDMI_RX_CEC R1921 1 2 0R R0402 5% HDMI_RX_CEC

R1922 1 2 0R R0402 5% DNP LT6911_RST

GPIO3_D4_d/HDMIIRX_HPDOUT_H R1923 1 2 0R R0402 5% HDMIIRX_HPDOUT_H

VCC_3V3_S0

R1916 2.2K 5% R0201 R1917 2.2K 5% R0201

I2C5_SDA_M0_TP

I2C5_SCL_M0_TP

VCC_1V8_S0

R1918 2.2K 5% R0201 R1919 2.2K 5% R0201

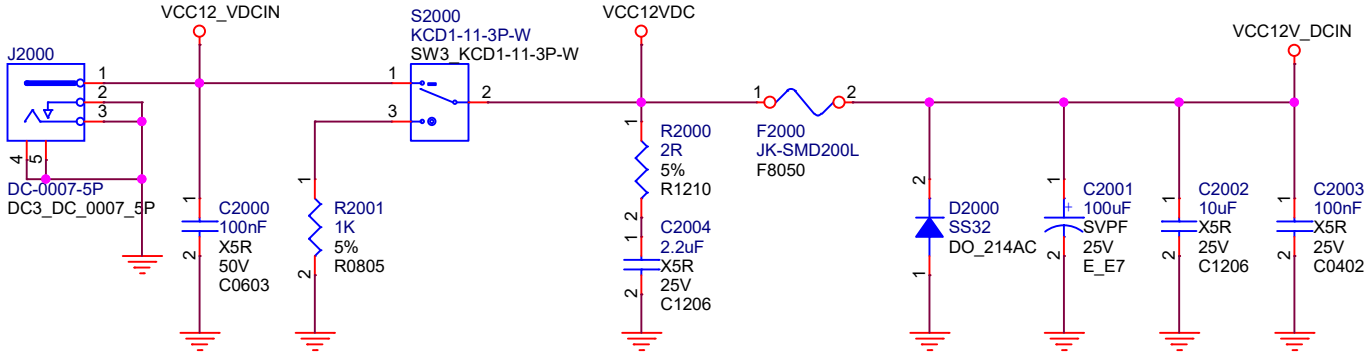
I2C2_SDA_M4_MIPI

I2C2_SCL_M4_MIPI

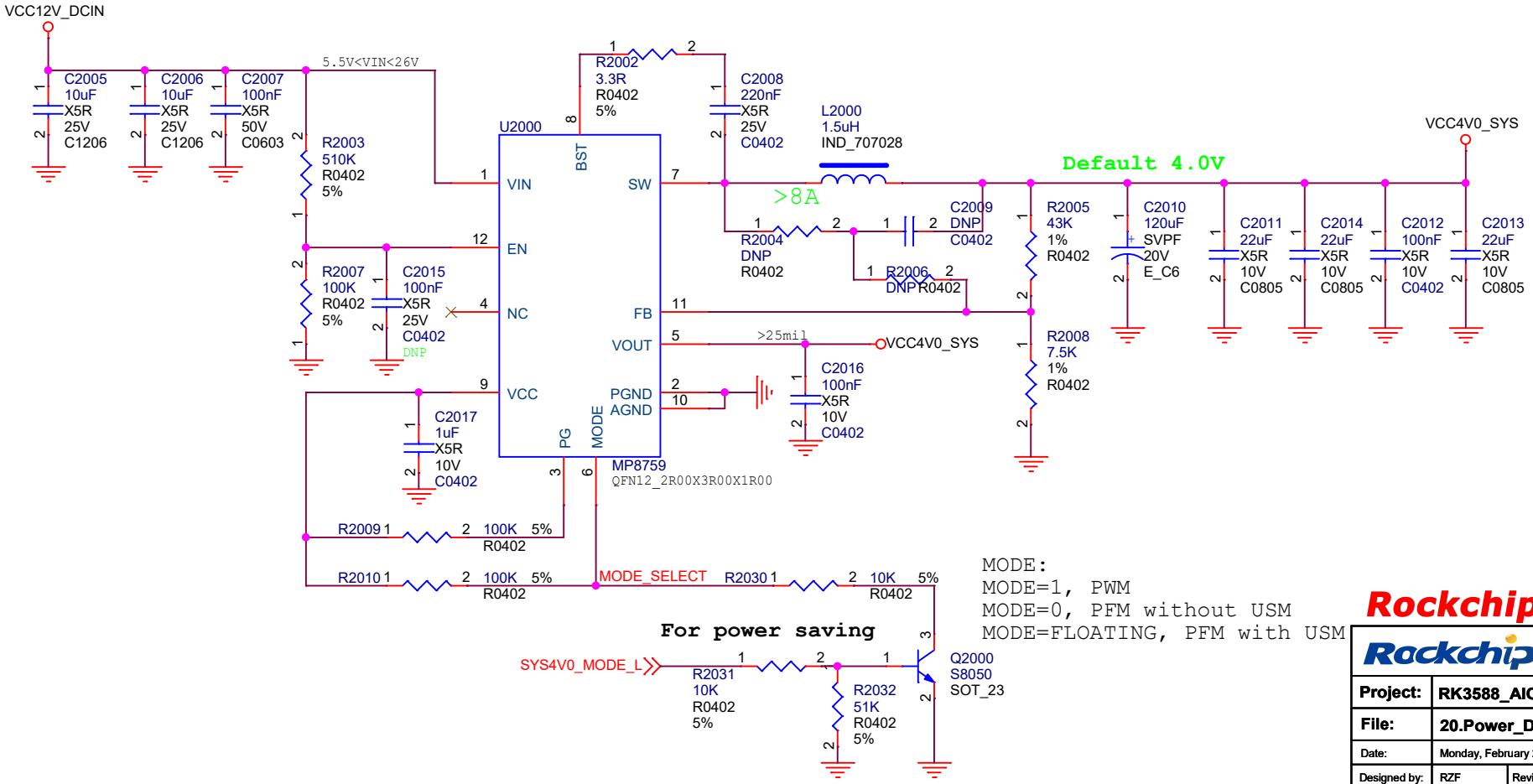
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	19.RK3588_1.8V 3.3V GPIO		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by:	RZF	Reviewed by:	Sheet: 19 of 99

12V DCIN



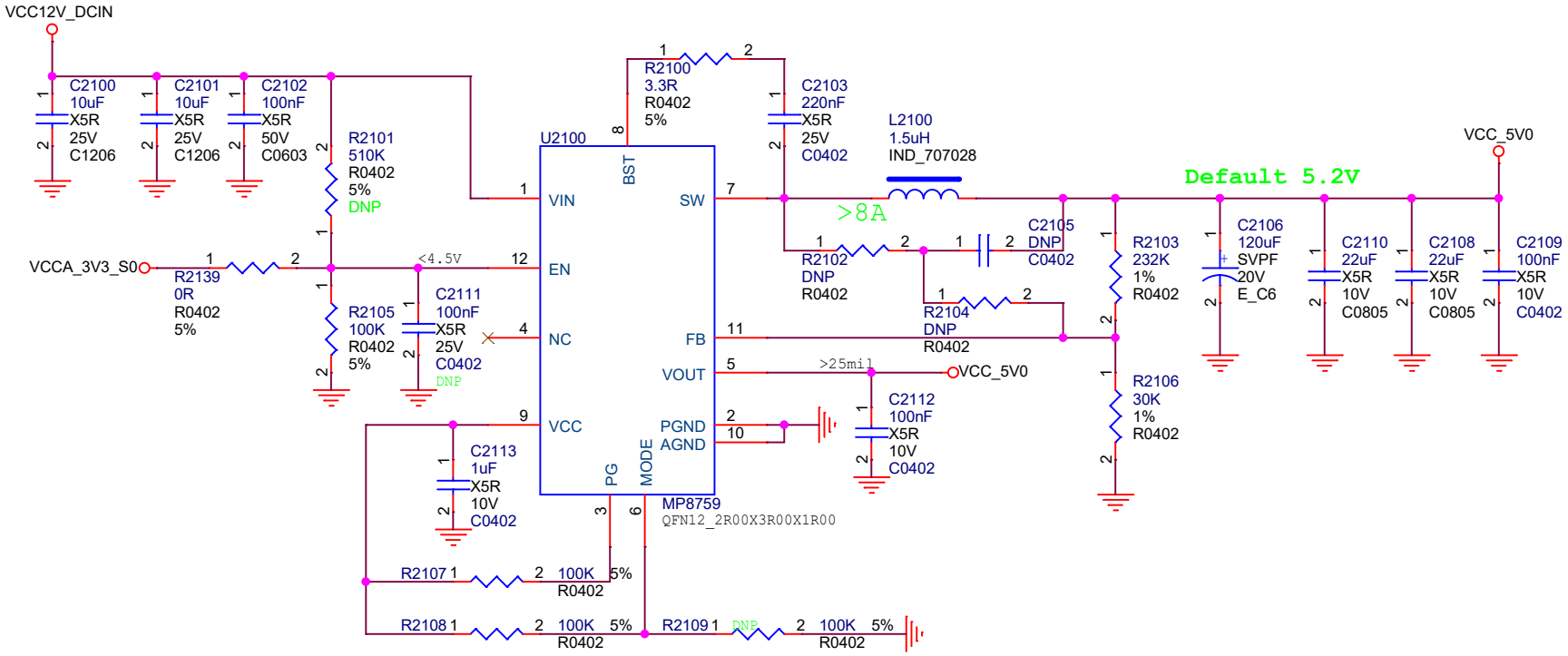
VCC4V0_SYS



Rockchip Confidential

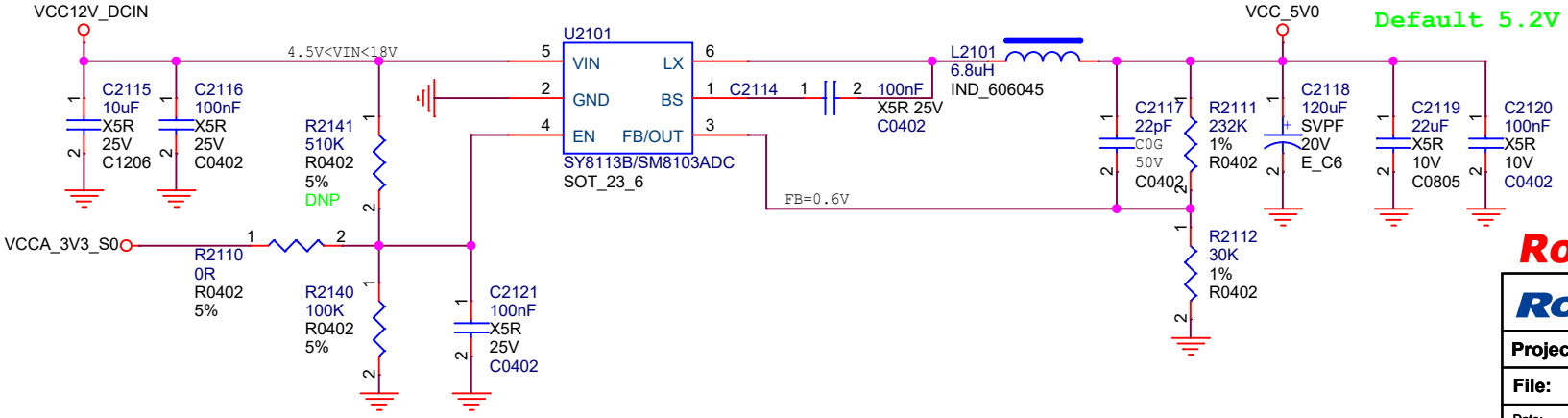
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	20.Power_DC IN/VCC4V0_SYS				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	20 of 99

VCC5V0_SYS
OPTION1:Output Support 5V/8A



Note:
DCDC power supply is recommended if the current exceeds 3A

VCC5V0_SYS
OPTION2:Output Support 5V/3A

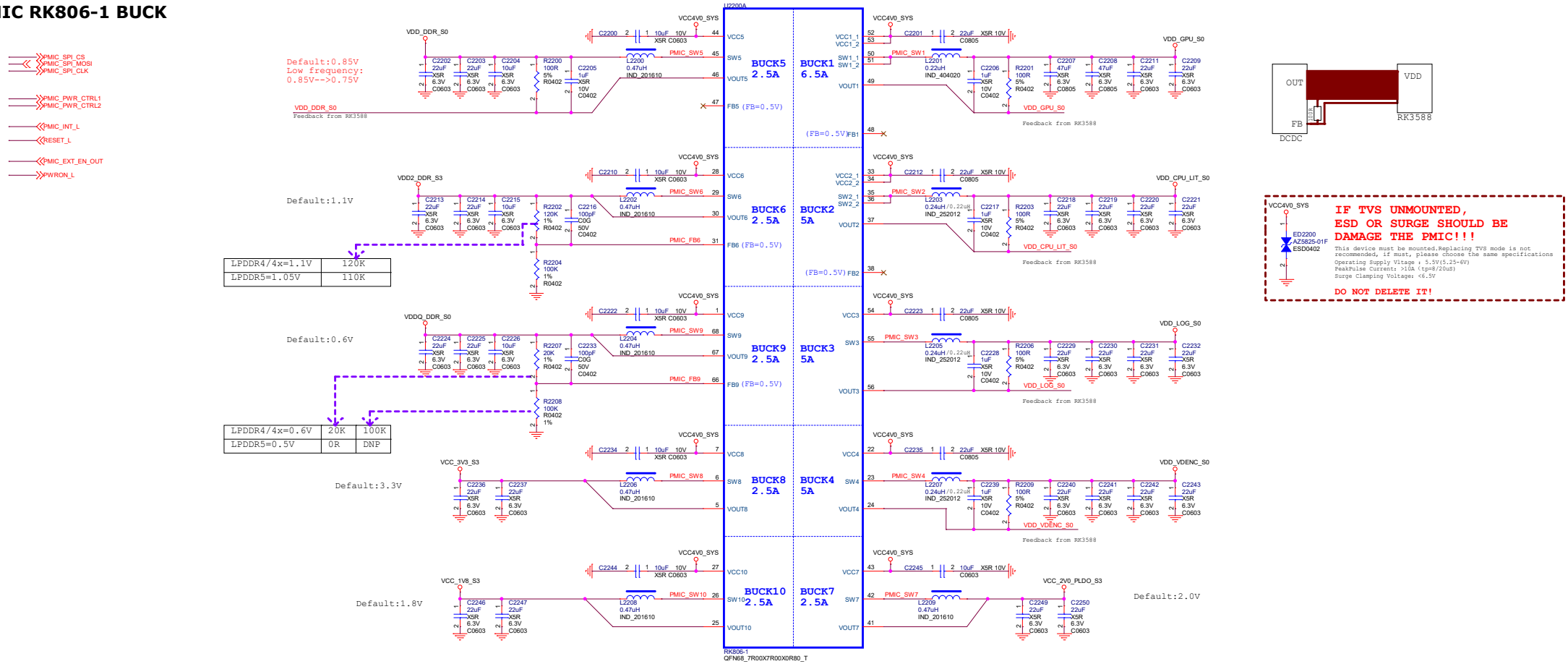


Note:
DCDC power supply is recommended if the current below 3A

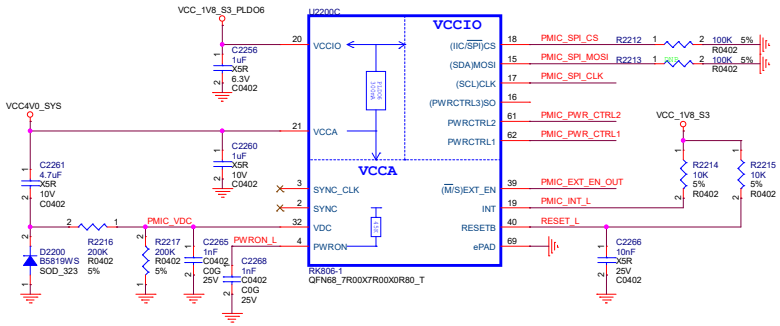
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	21.Power_Ext VCC_5V0				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	21 of 99

PMIC RK806-1 BUCK



PMIC RK806-1 Managerment

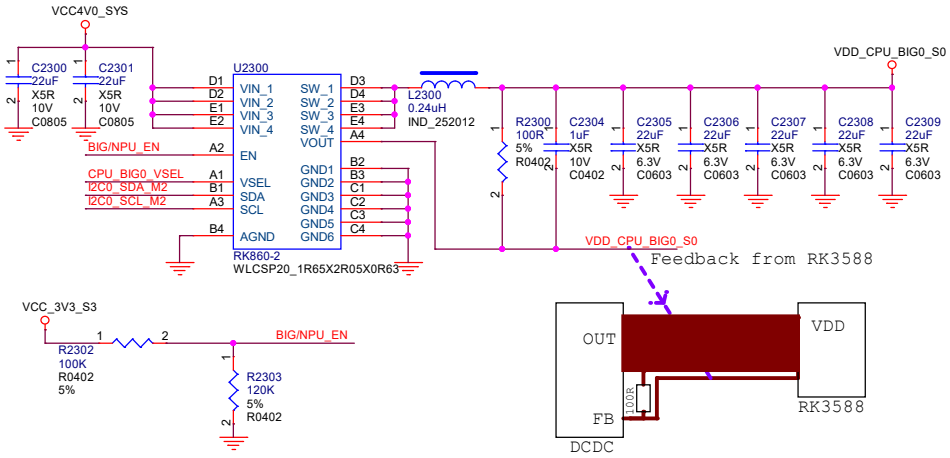


PMIC RK806-1 LDO

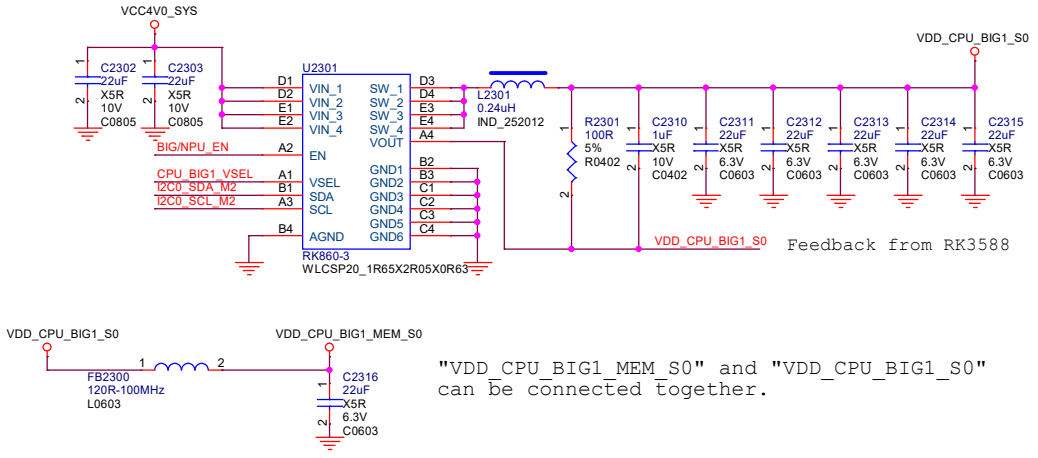
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	22.Power-PMIC_RK806-1		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by: Default	Sheet:	22 of 99

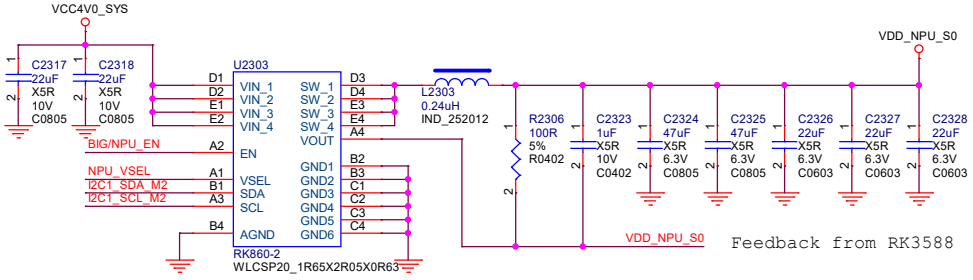
VDD_CPU_BIG0



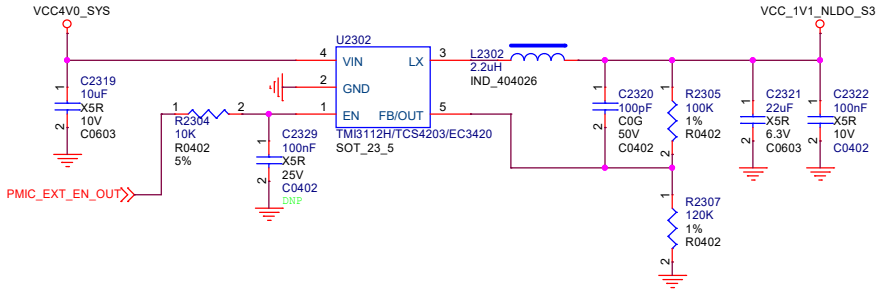
VDD_CPU_BIG1

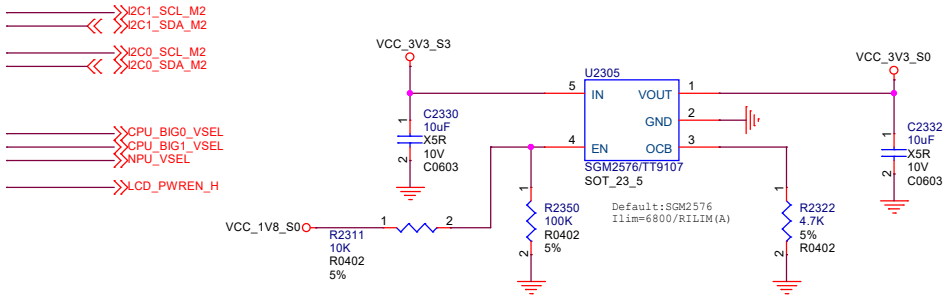


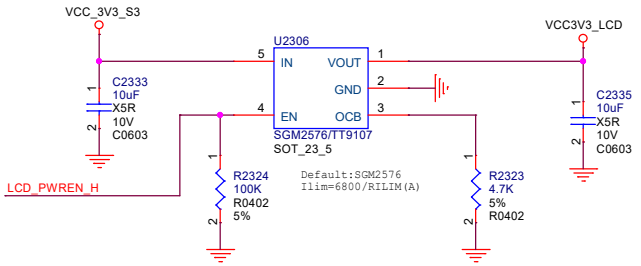
VDD_NPU



VCC_1V1_NLDO_S3



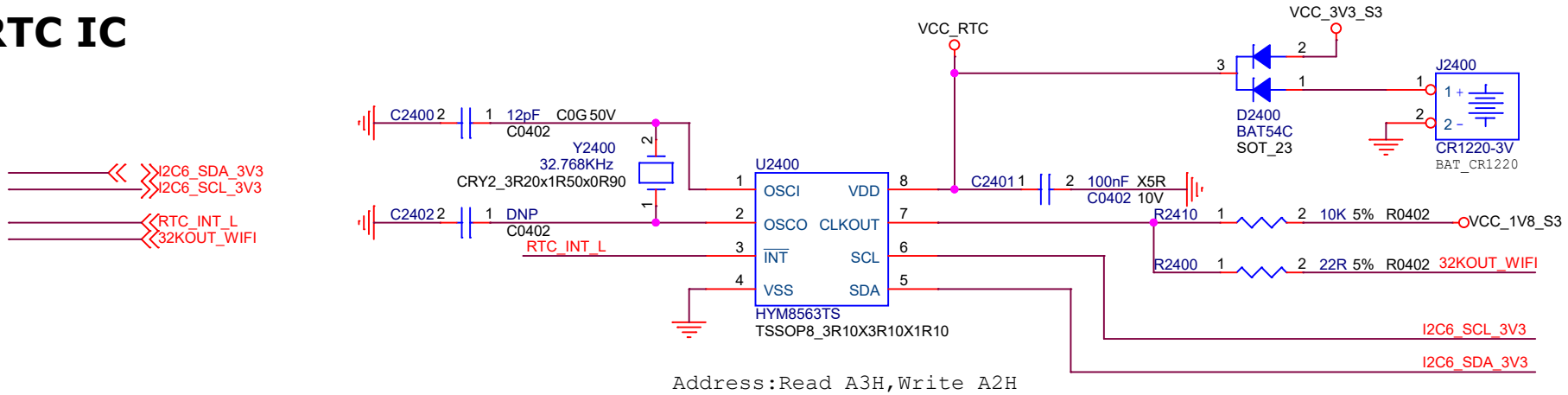




Rockchip Confidential

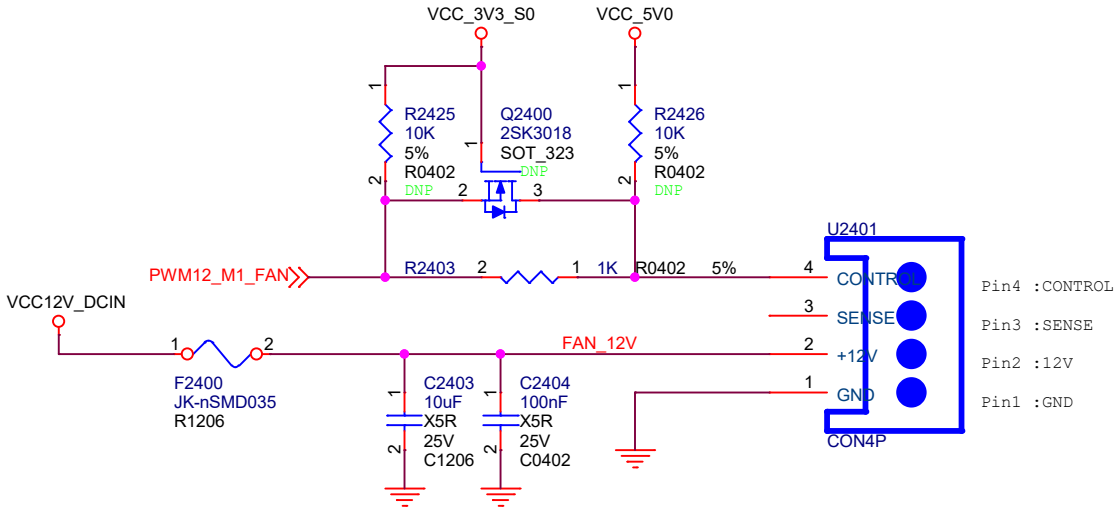
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	23.Power_Ext Discrete				
Date:	Thursday, March 02, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	23 of 99

RTC IC

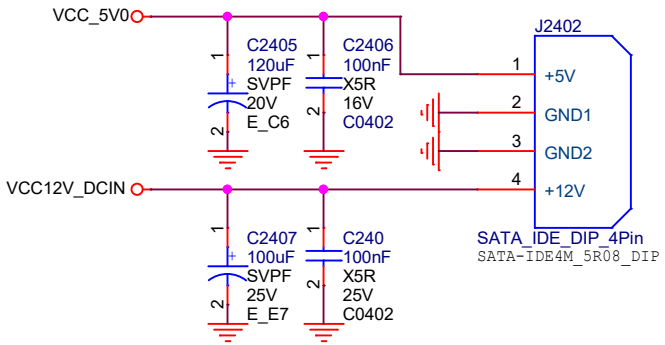


Address:Read A3H,Write A2H

FAN_POWER



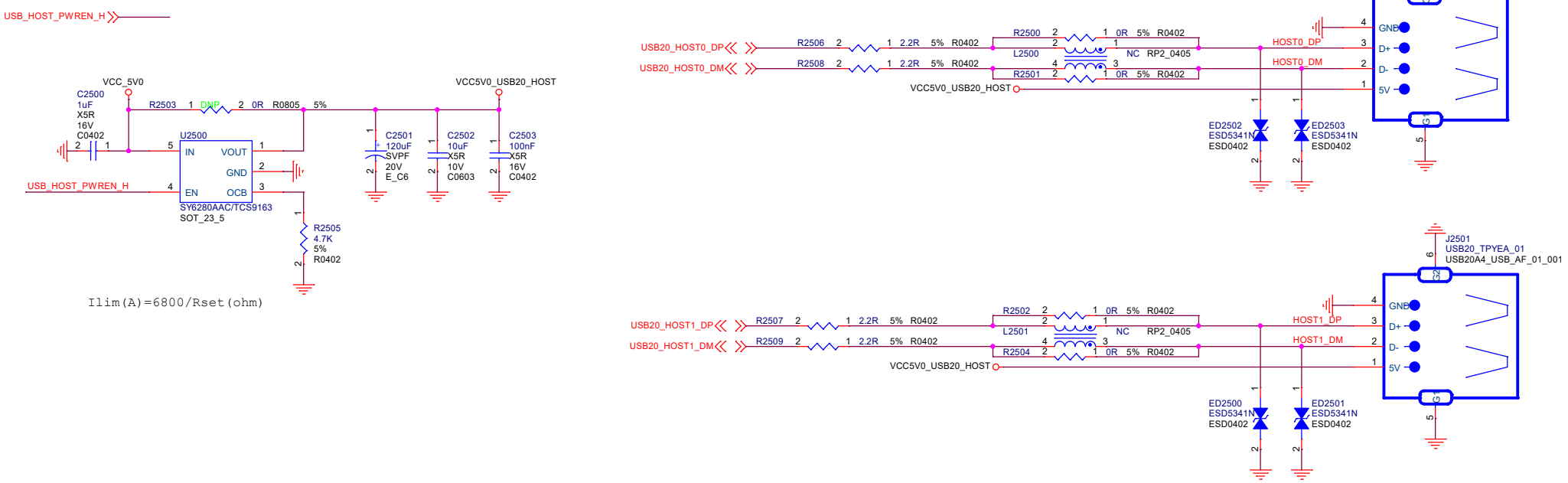
SATA_POWER



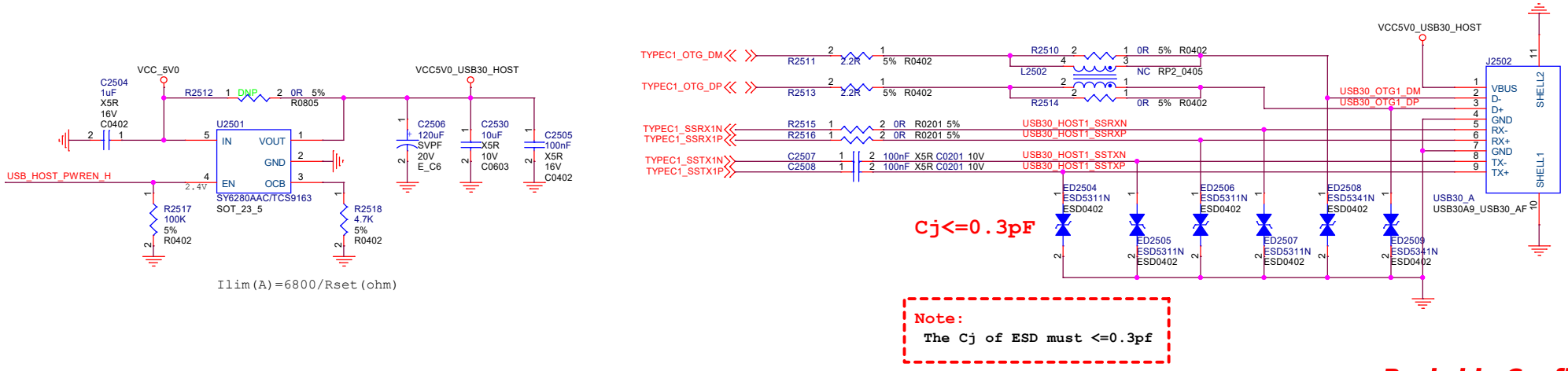
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	24.RTC/FAN/SATA POWER				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	24 of 99

USB2.0 HOST PORT



USB3.0 HOST PORT

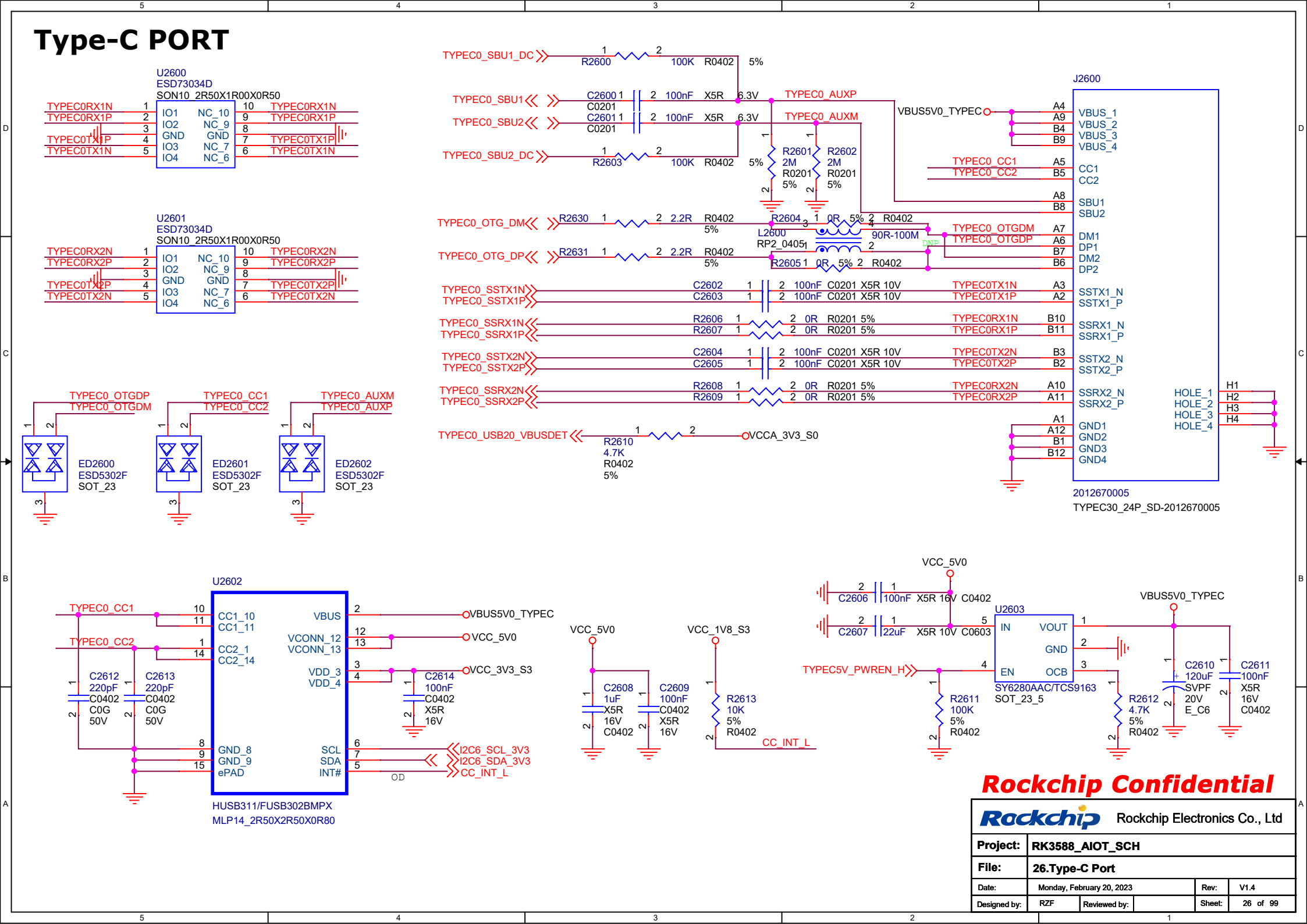


Note:
The Cj of ESD must <=0.3pf

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	25.USB20/USB30 Port				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	25 of 99

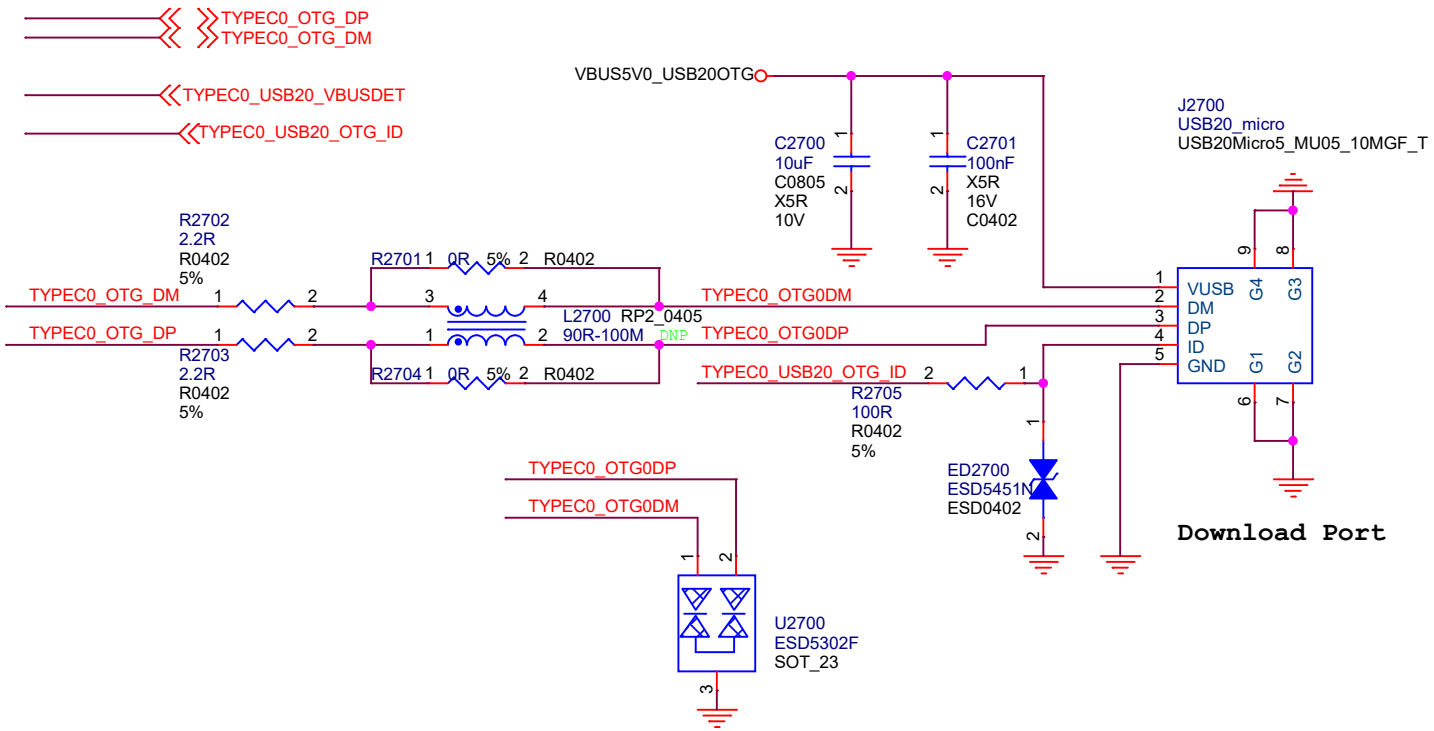
Type-C PORT



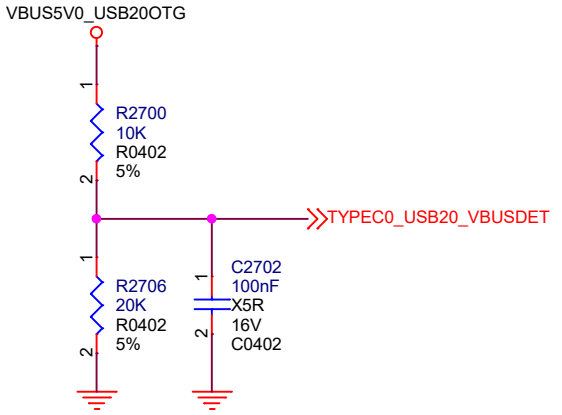
Rockchip Confidential

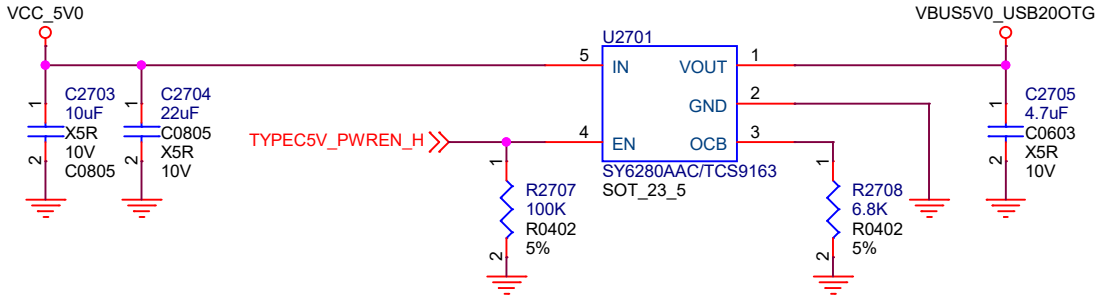
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	26.Type-C Port		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by:	RZF	Reviewed by:	Sheet: 26 of 99

USB2.0 Micro Port



USB Detection

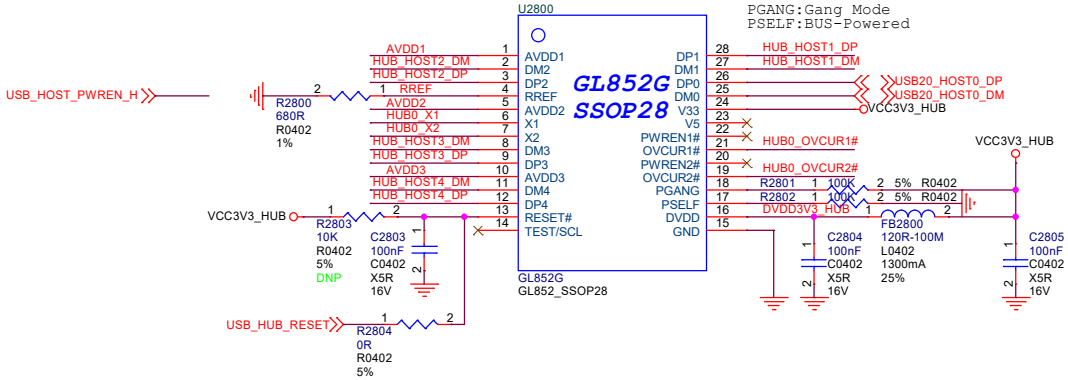




Rockchip Confidential

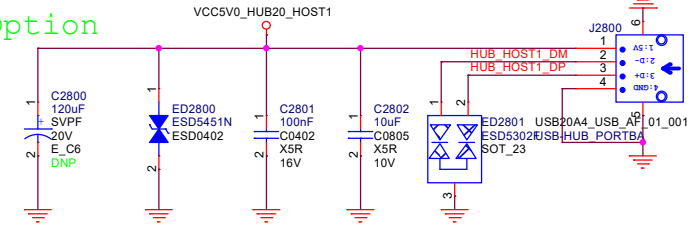
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	27.USB2.0 Micro Port(option)				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	27 of 99

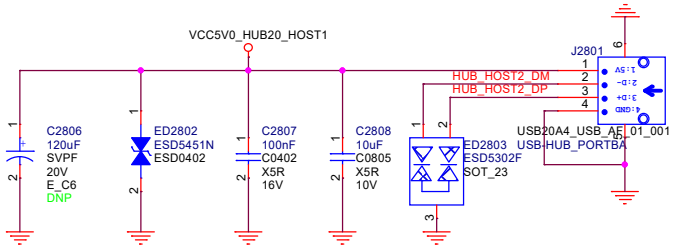
USB2.0 HUB

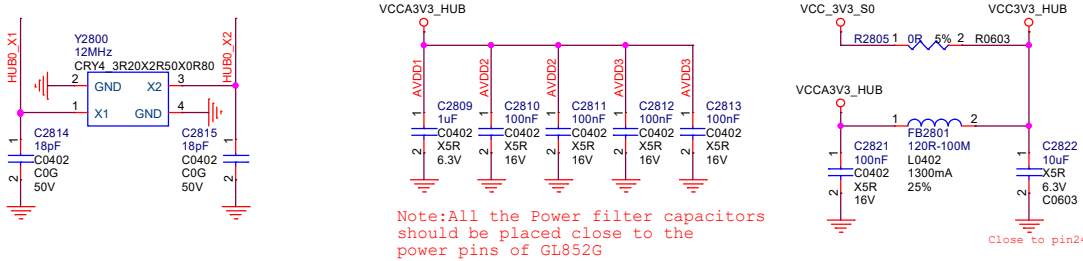


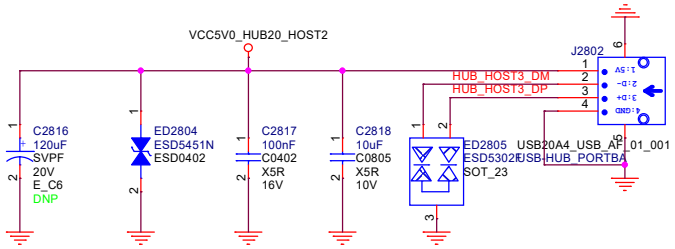
Note:
Used ECAP if want to drive mobile hard-disk and enough structure space for place.

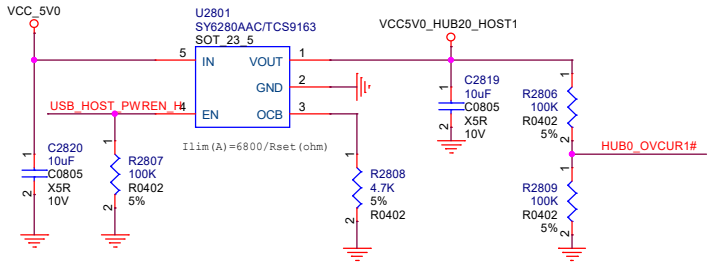
Option

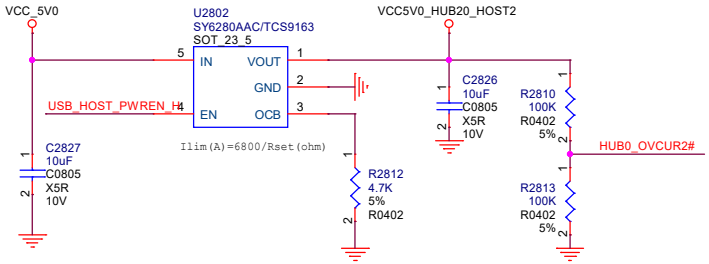


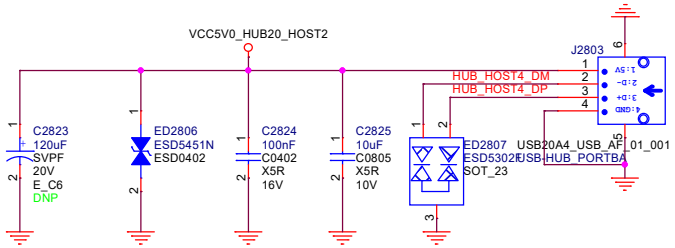








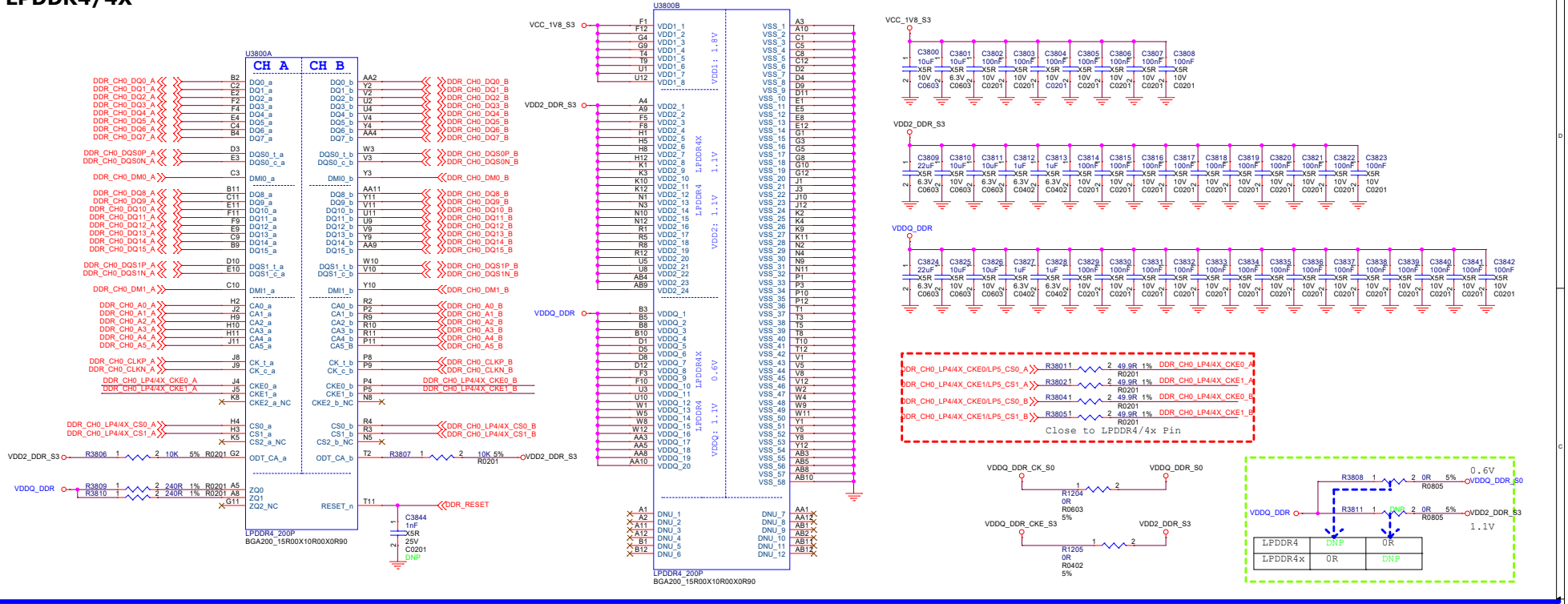


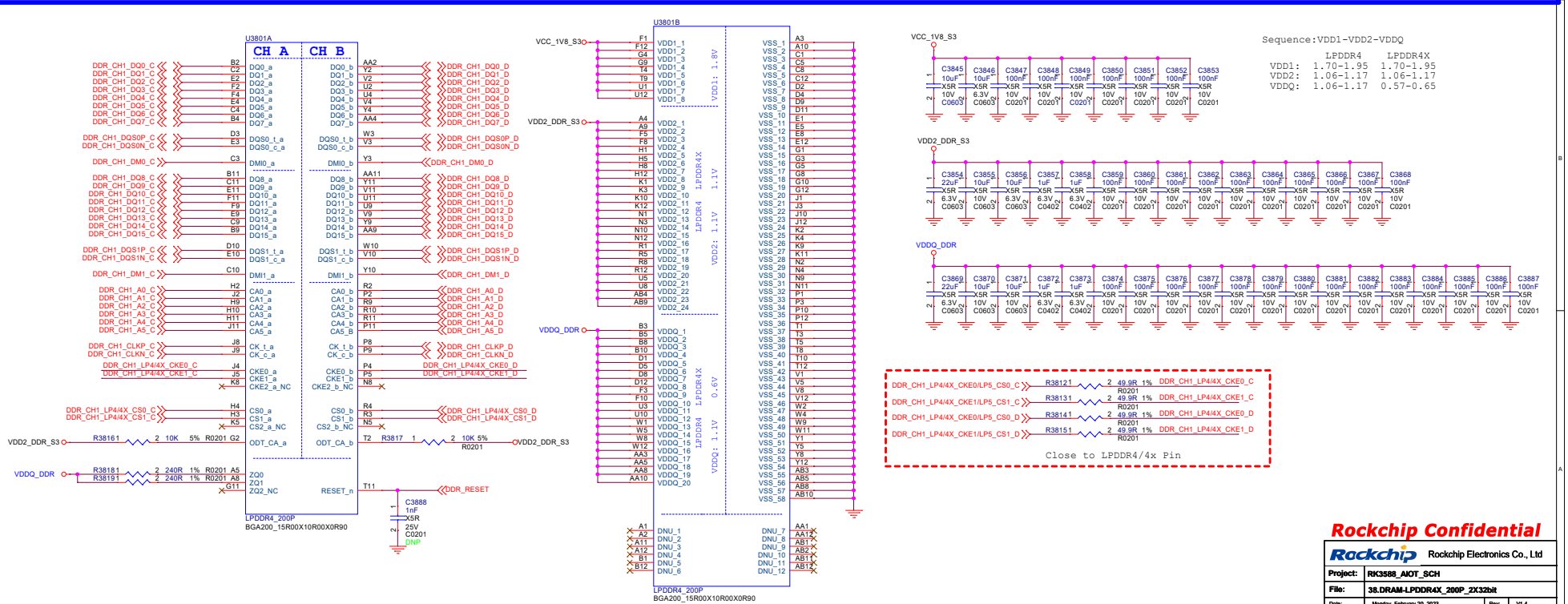


Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	28.USB HUB GL85x (option)				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	28 of 99

LPDDR4/4X

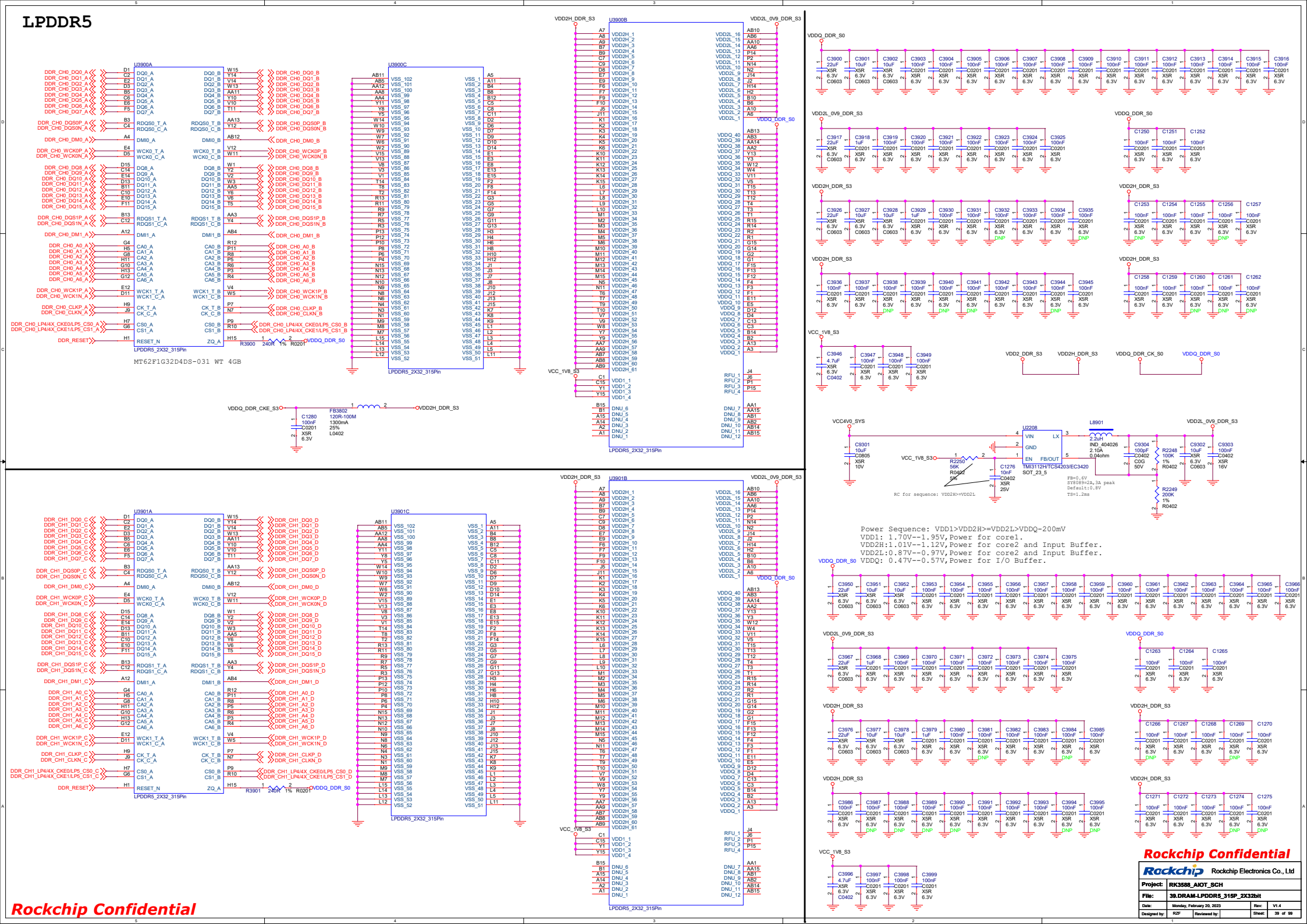




Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	38.DRAM-LPDDR4X_200P_2X32bit
Date:	Monday, February 20, 2023
Rev:	V1.4
Designed by:	RZF
Reviewed by:	
Sheet:	38 of 99

LPDDR5

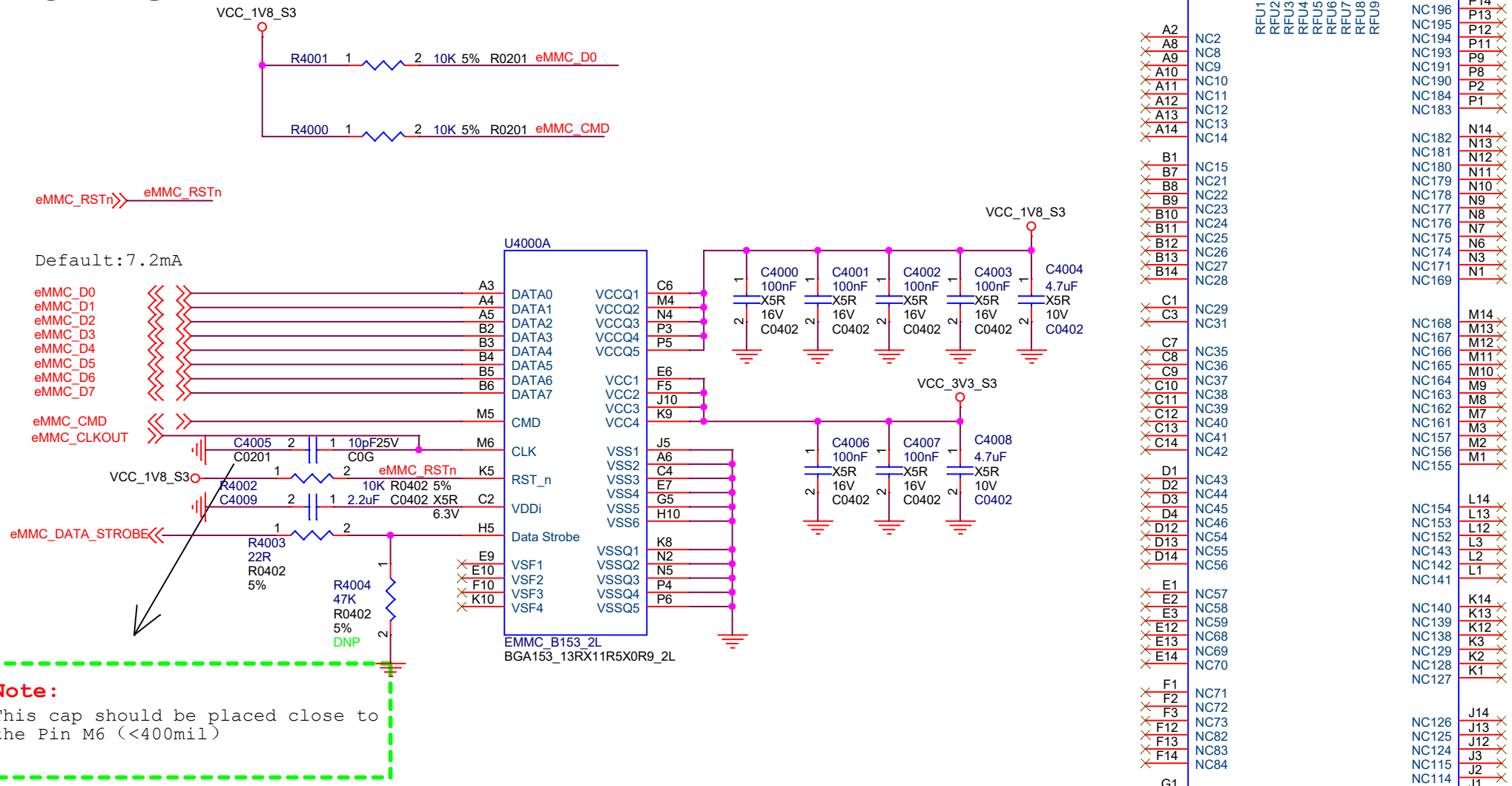


Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for core1.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer.
VDDQ: 0.47V--0.57V,Power for I/O Buffer.

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	39.DRAM-LPDDR5_315P_2X32bit
Date:	Monday, February 20, 2023
Rev:	V1.4
Designed by:	RZF
Reviewed by:	
Sheet:	39 of 99

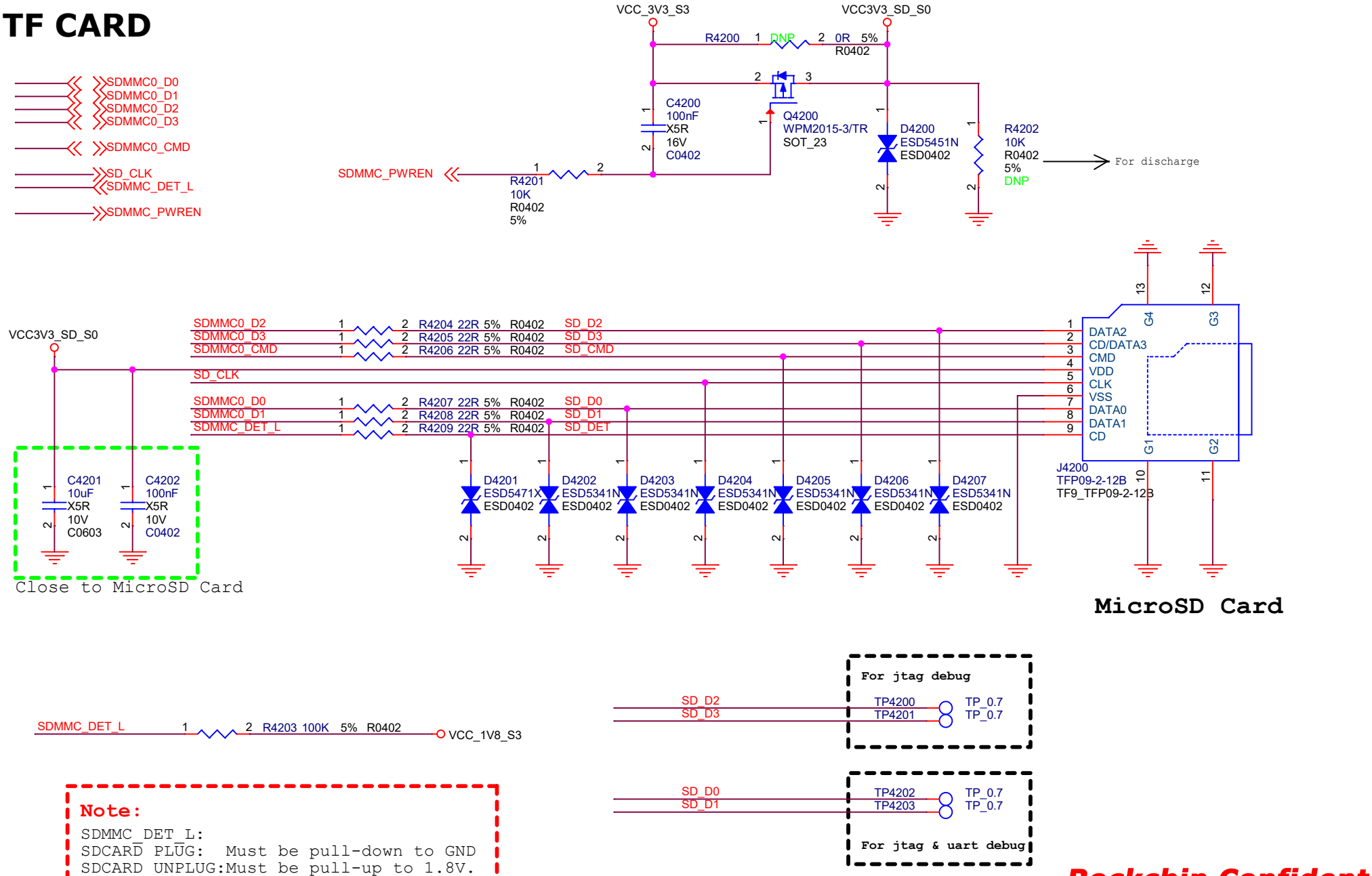
Rockchip Confidential

eMMC FLASH



Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	40.Flash-eMMC Flash		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	40 of 99

TF CARD



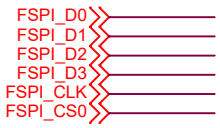
Note:

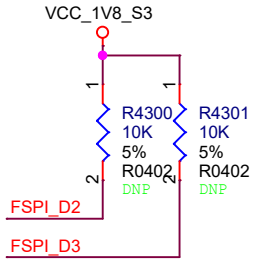
SDMMC_DET_L:
SDCARD PLUG: Must be pull-down to GND
SDCARD UNPLUG:Must be pull-up to 1.8V.

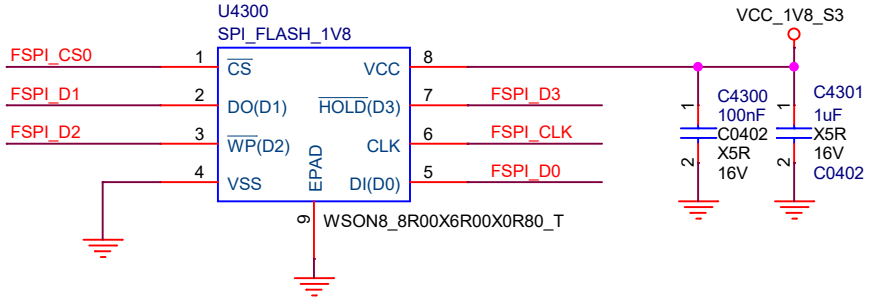
Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	42.Flash-TF Card		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	42 of 99

Rockchip Confidential

SPI NOR OR NAND Flash







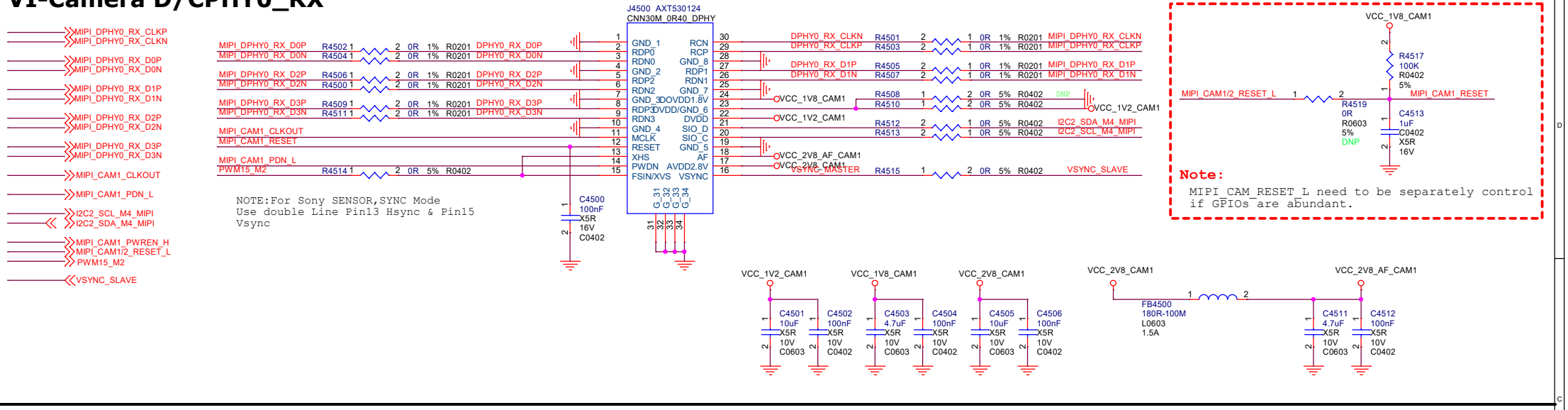
SPI FLASH:1.8V

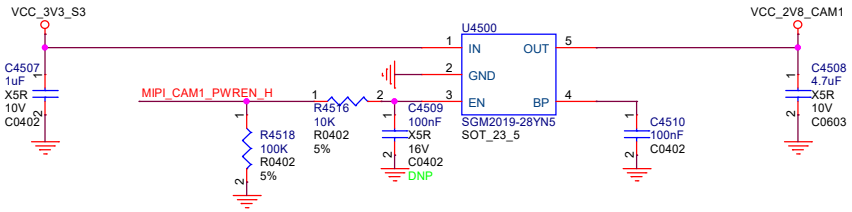
Note:
When using SPI FLASH with only 1 bit, it needs to be stuffed.

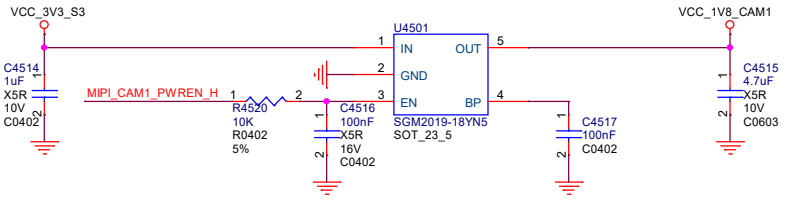
Rockchip Confidential

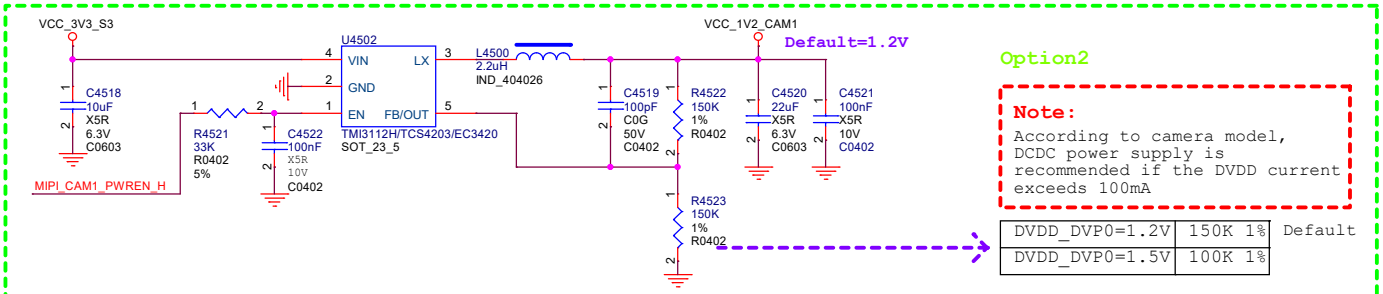
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	43.Flash-SPI FLASH(option)				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	43 of 99

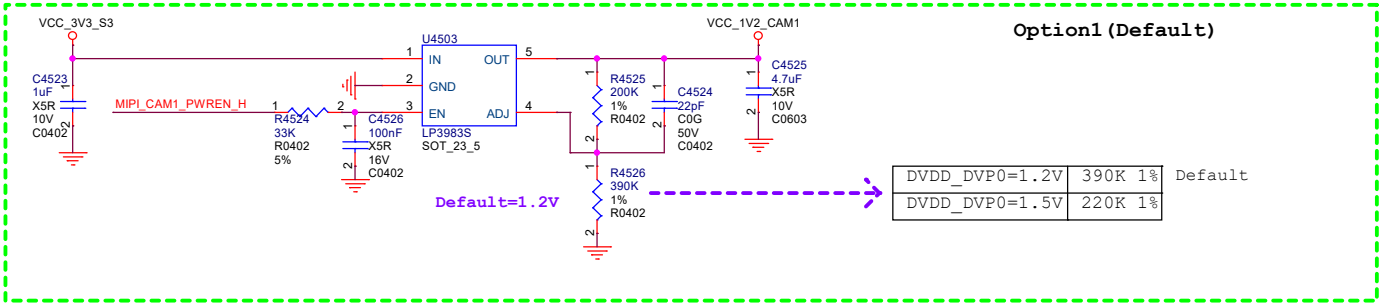
VI-Camera D/CPHY0_RX











Note:

Adjust the power on sequence according to the camera model

eg:OV50C40

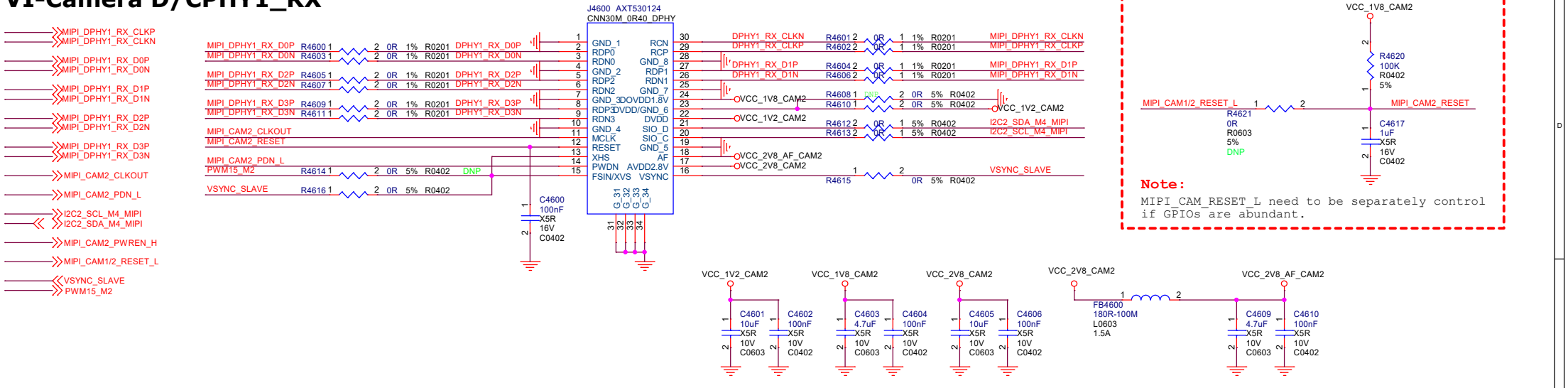
Power on Sequence

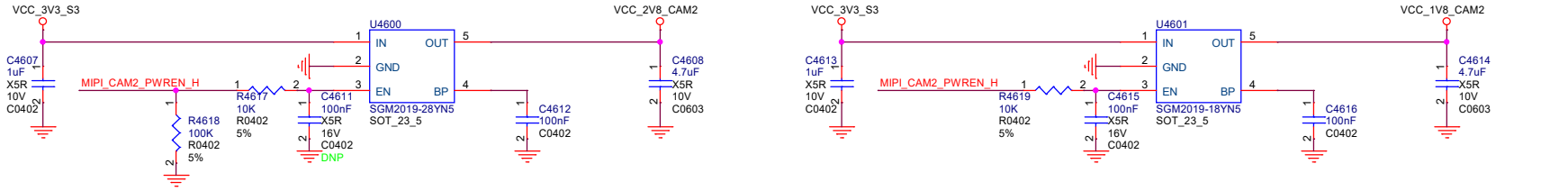
2.8V-->1.8V-->1.2V--->MCLK-->PWDN--->RST

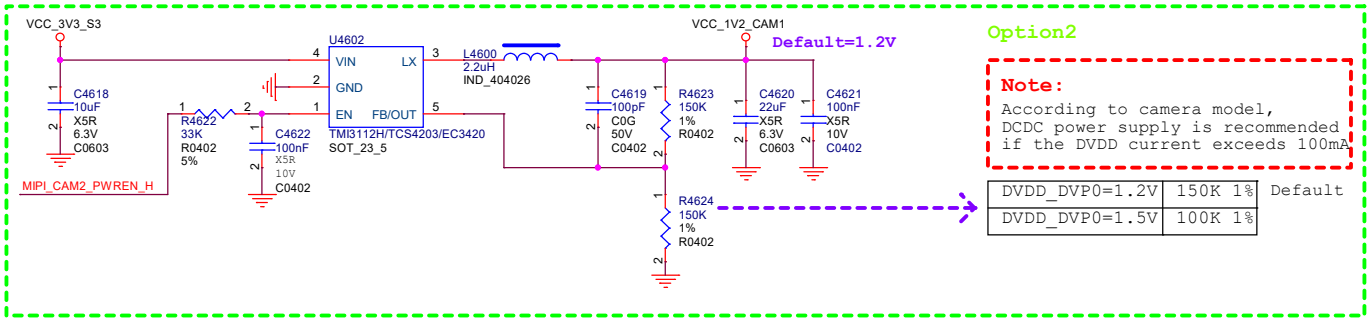
Rockchip Confidential

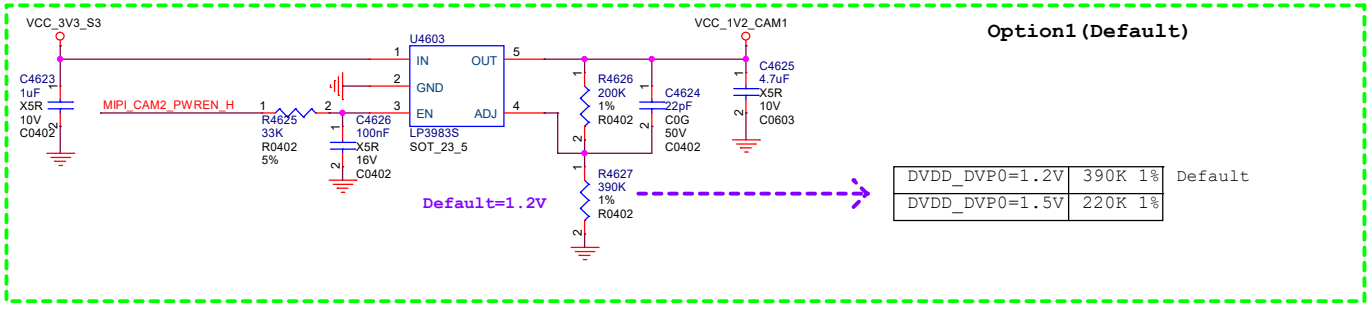
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	45.VI-Camera MIPI_D/CPHY0-RX				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	45 of 99

VI-Camera D/CPHY1_RX









Note:

Adjust the power on sequence according to the camera model

eg:OV50C40

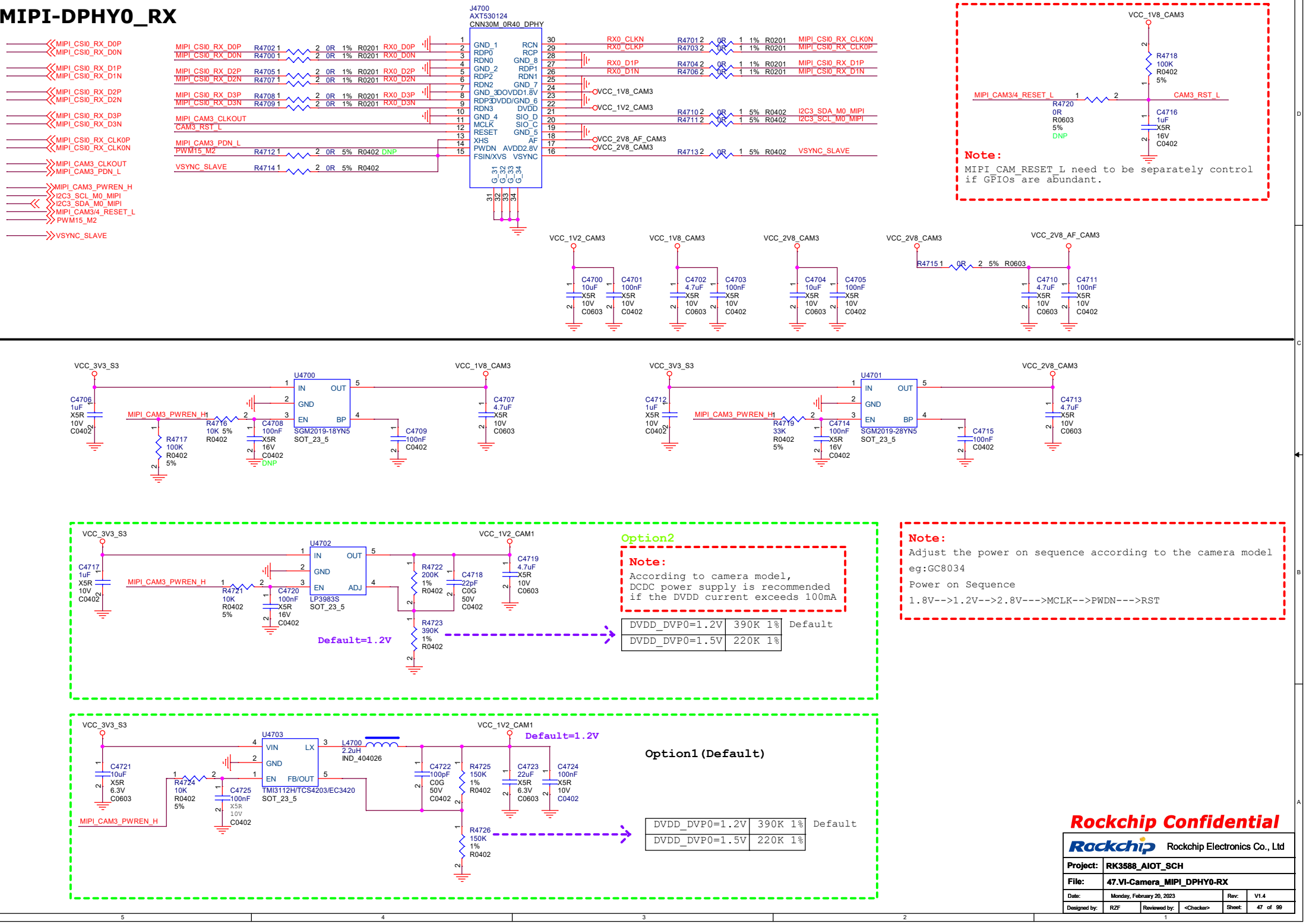
Power on Sequence

2.8V-->1.8V-->1.2V--->MCLK-->PWDN--->RST

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	46.VI-Camera MIPI_D/CPHY1-RX				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	46 of 99

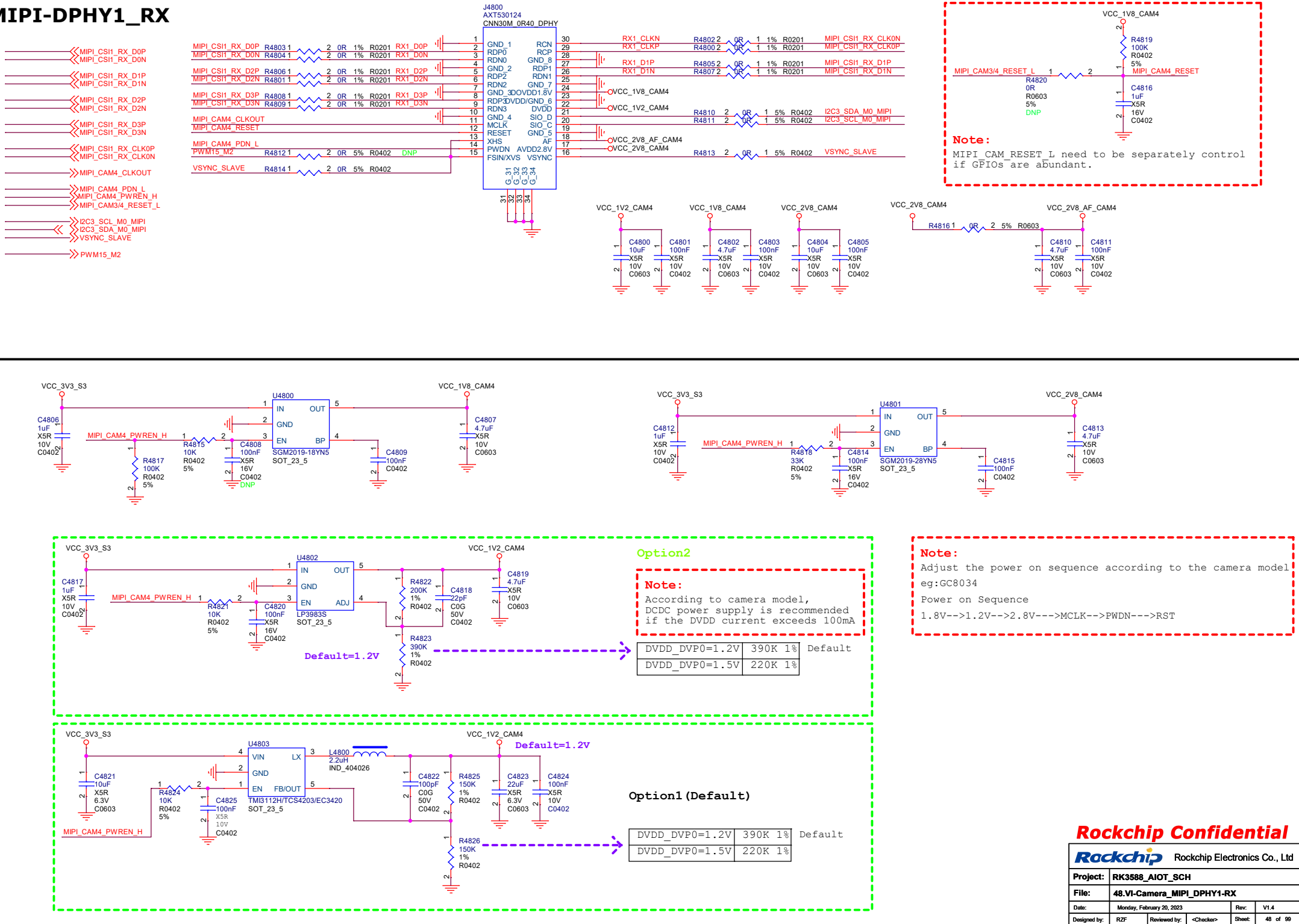
MIPI-DPHY0_RX



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	47.VI-Camera_MIPI_DPHY0-RX				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	47 of 99

MIPI-DPHY1_RX



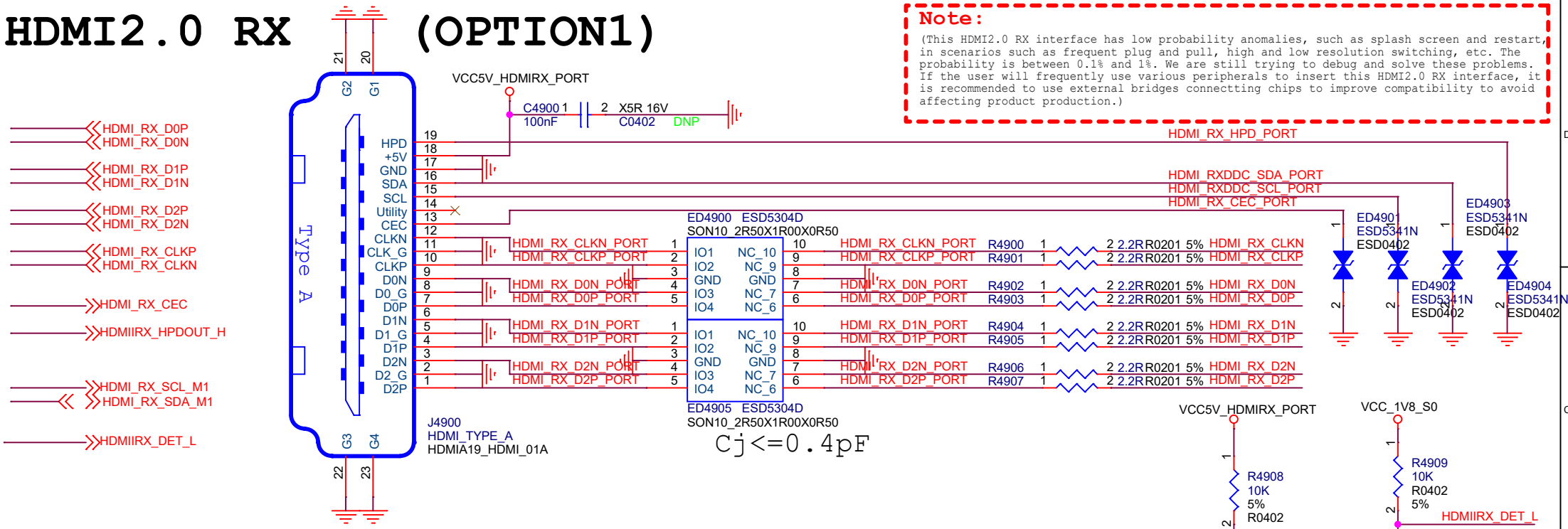
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	48.VI-Camera_MIPI_DPHY1-RX				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	48 of 99

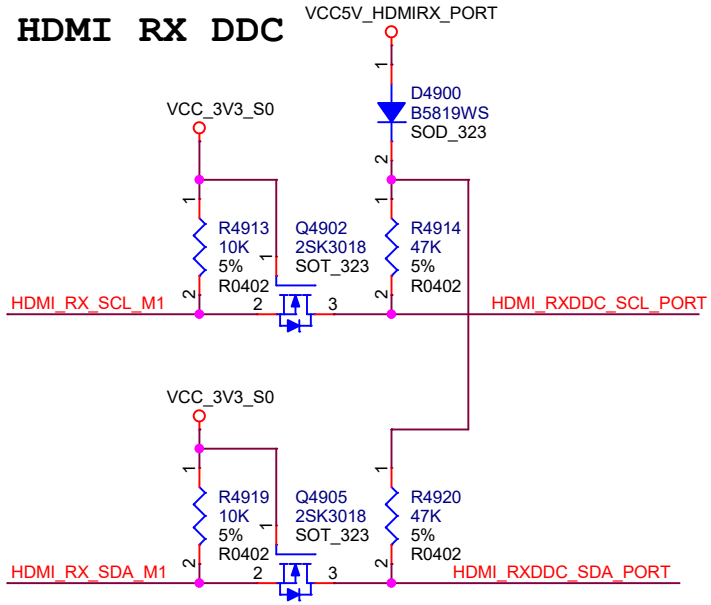
HDMI2.0 RX (OPTION1)

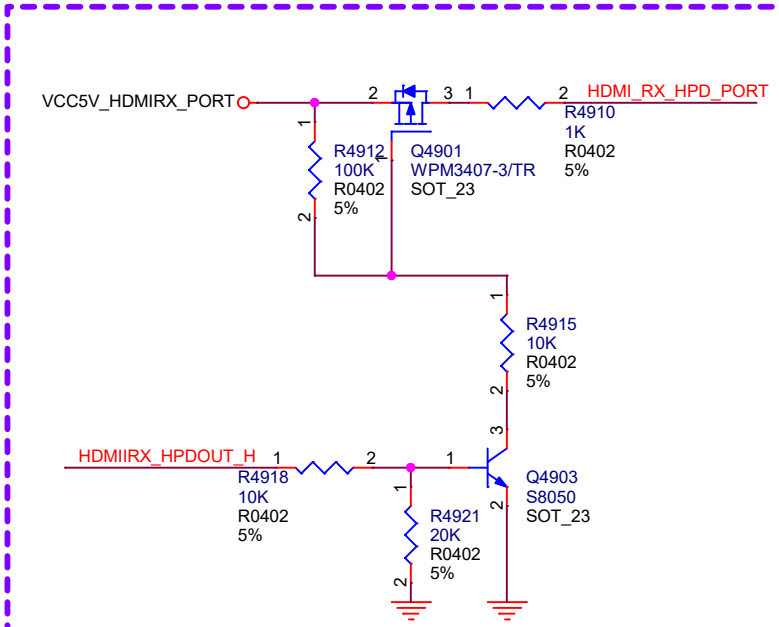
Note:

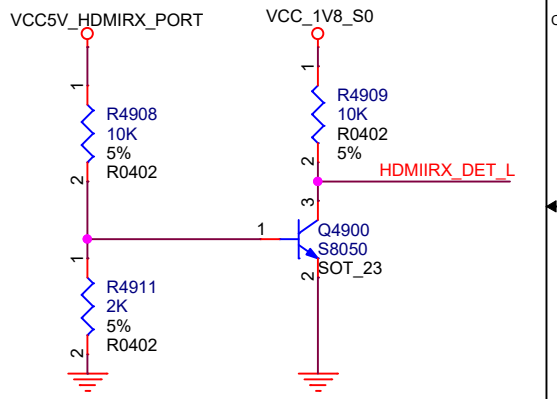
(This HDMI2.0 RX interface has low probability anomalies, such as splash screen and restart, in scenarios such as frequent plug and pull, high and low resolution switching, etc. The probability is between 0.1% and 1%. We are still trying to debug and solve these problems. If the user will frequently use various peripherals to insert this HDMI2.0 RX interface, it is recommended to use external bridges connectting chips to improve compatibility to avoid affecting product production.)

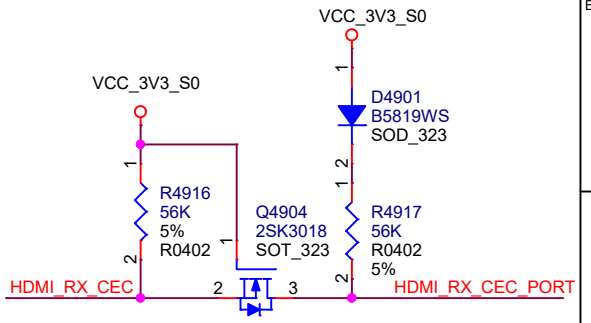


HDMI RX DDC







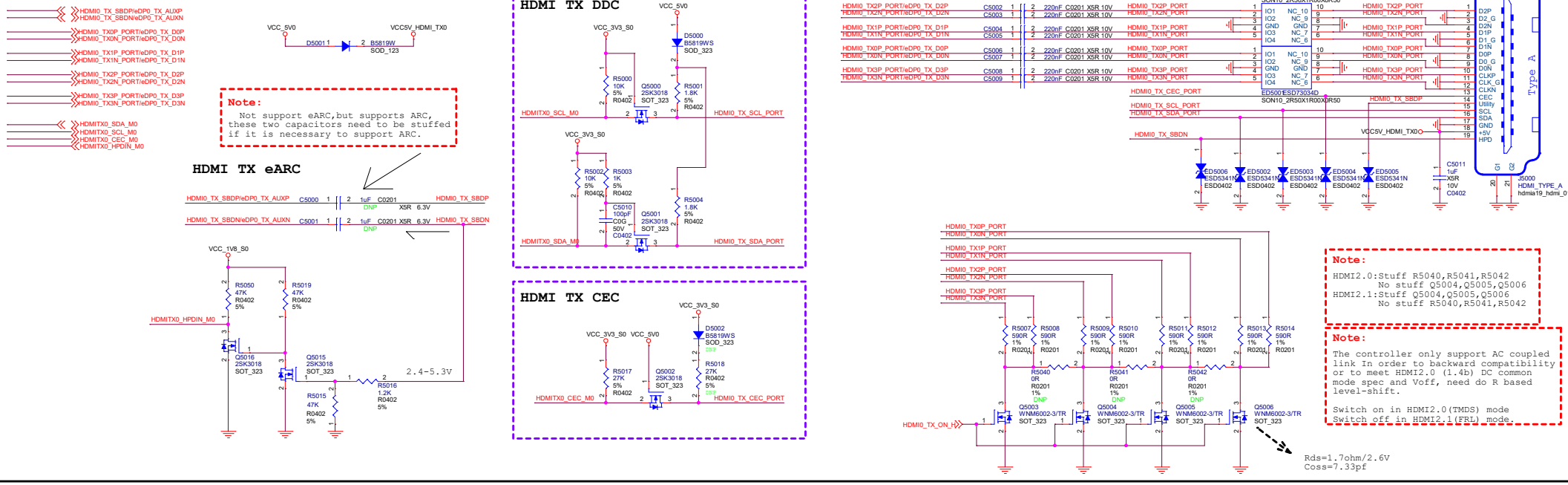


HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V

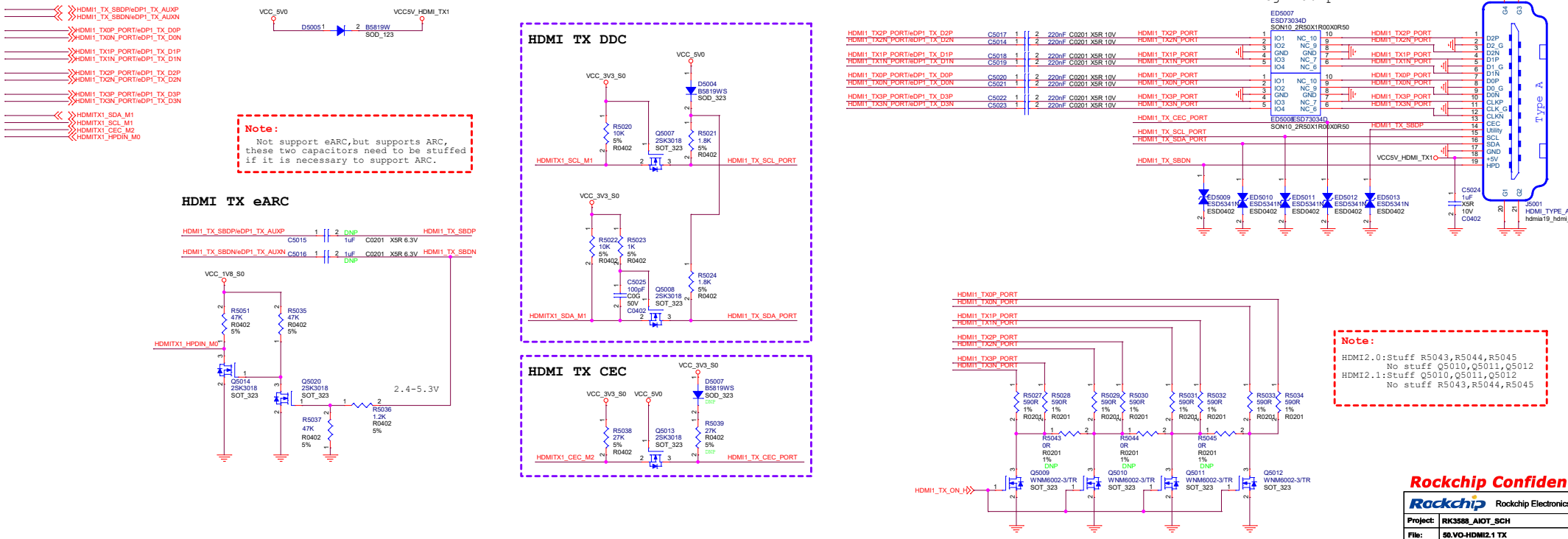
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	49.VI-HDMI2.0 RX(option1)				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	49 of 99

HDMI TX0

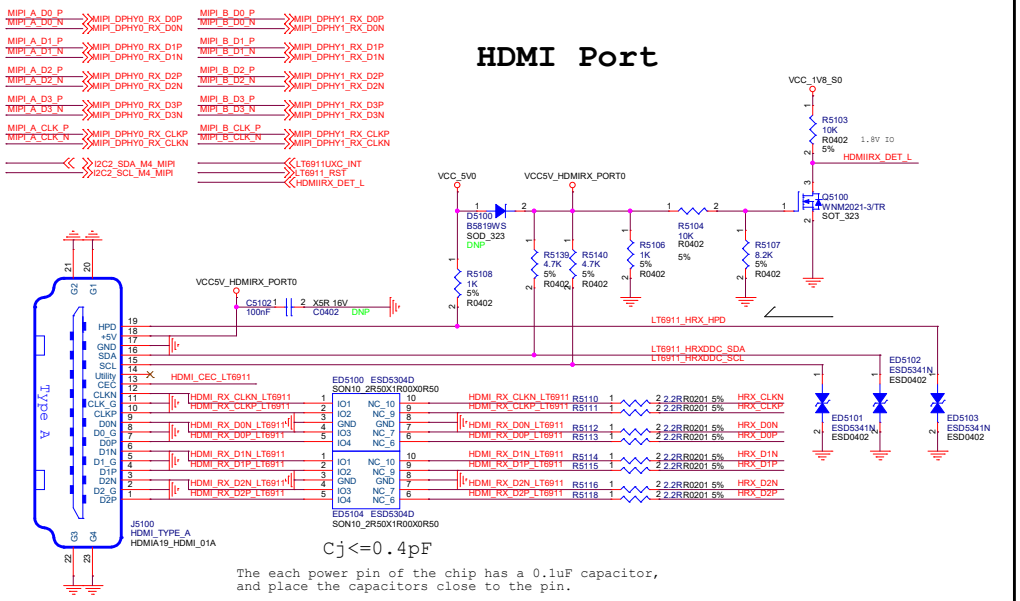


HDMI TX1



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	50.VO-HDMI2.1 TX
Date:	Friday, March 03, 2023
Rev:	V1.4
Designed by:	RZF
Reviewed by:	
Sheet:	50 of 99

HDMI2.0 RX(OPTION2)



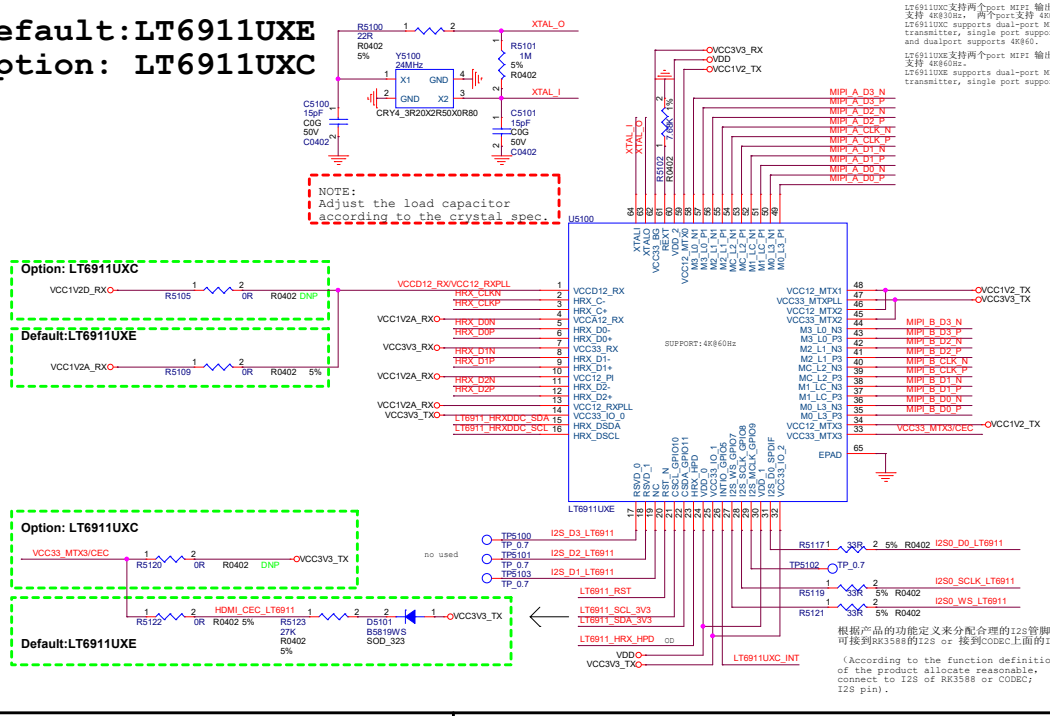
Cj<=0.4pF

The each power pin of the chip has a 0.1uF capacitor, and place the capacitors close to the pin.

Default:LT6911UXE
Option: LT6911UXC

LT6911UXC支持两个port MIPI 输出，单个port支持 4K@30Hz，两个port支持 4K@60。
LT6911UXC supports dual-port MIPI DSI/CSI transmitter, single port supports 4K@30Hz, and dualport supports 4K@60.

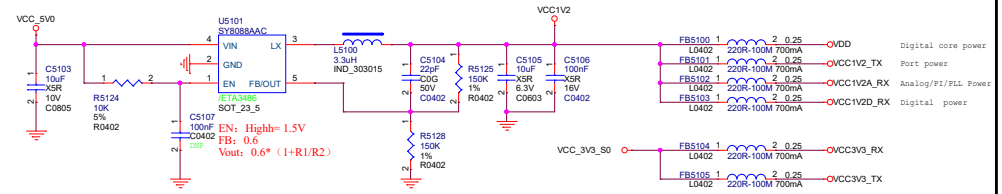
LT6911UXE支持两个port MIPI 输出，单个port支持 4K@60Hz。
LT6911UXE supports dual-port MIPI DSI/CSI transmitter, single port supports 4K@60Hz.

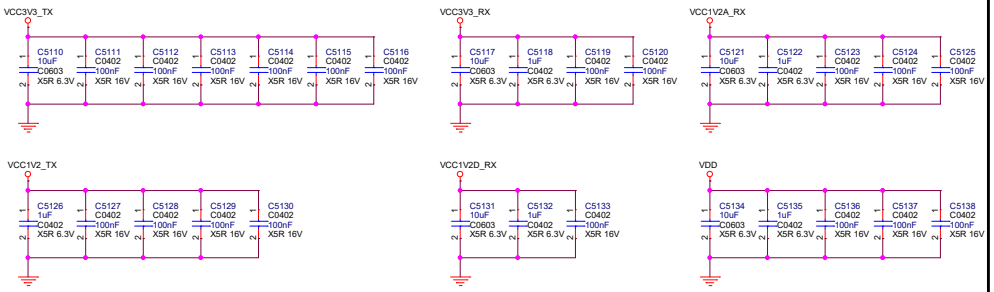


根据产品的功能定义来分配合理的I2S管脚，可接到RK3588的I2S or 接到CODEC上面的I2S;

(According to the function definition of the product allocate reasonable, connect to I2S of RK3588 or CODEC; I2S pin).

Power

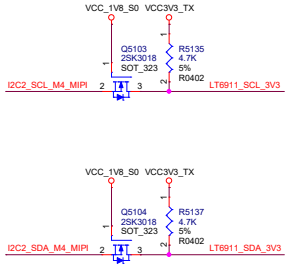




LT6911UXC & LT6911UXE HARDWARE DIFFERENCES

	LT6911UXC	LT6911UXE	DESCRIPTION
Pin1	VCCD12_RX	VCCD12_RXPLL	
Pin17	RSVD	I2S_D3_SPDIF	Audio I2S serial data 3 output, also shared as audio SPDIF output.
Pin18	RSVD	I2S_D2_GPIO2	Audio I2S serial data 2 output, also shared as general purpose I/O 2.
Pin19	NC	I2S_D1_GPIO1	Audio I2S serial data 1 output, also shared as general purpose I/O 1.
Pin29	I2S_MCLK_GPIO9	I2S_MCLK_GPIO9	Audio I2S master clock output, also shared as general purpose I/O 9.
Pin33	VCC33_MTX3	CEC	HDMI RX CEC signal.

I2C



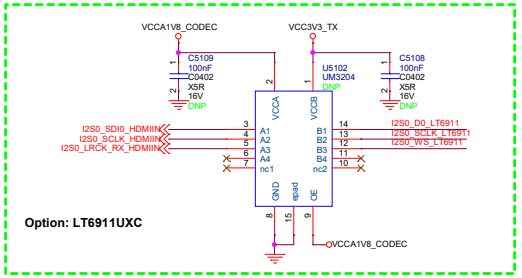
I2C地址是 0x56，用于芯片升级固件，接测试点调试，也可以外接MCU的I2C口来升级版本,速率低于 100KHz;请加上拉电阻到 3.3V.

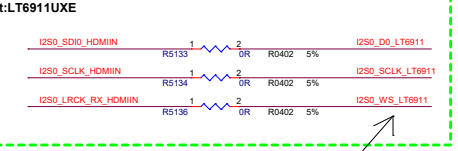
The I2C address is 0x56, it is used to upgrade the firmware of the chip, and the test point is used for debugging. The chip can also be upgraded by the external I2C of the MCU, the rate is below 100KHz; Please add pull-up resistors to 3.3V.

AUDIO

芯片可以做音频分离，输出的音频格式为I2S，I2S接口支持2声道音频，采样速率为32～192kHZ，采样大小为16～24位；芯片的I2S仅支持Master方式。

The chip can separate audio signal, and the output audio signal format supports I2S. I2S interface supports 2-channel audio, with sample rates of 32~192 kHz and sample sizes of 16-24 bits; I2S of this chip only supports Master mode.





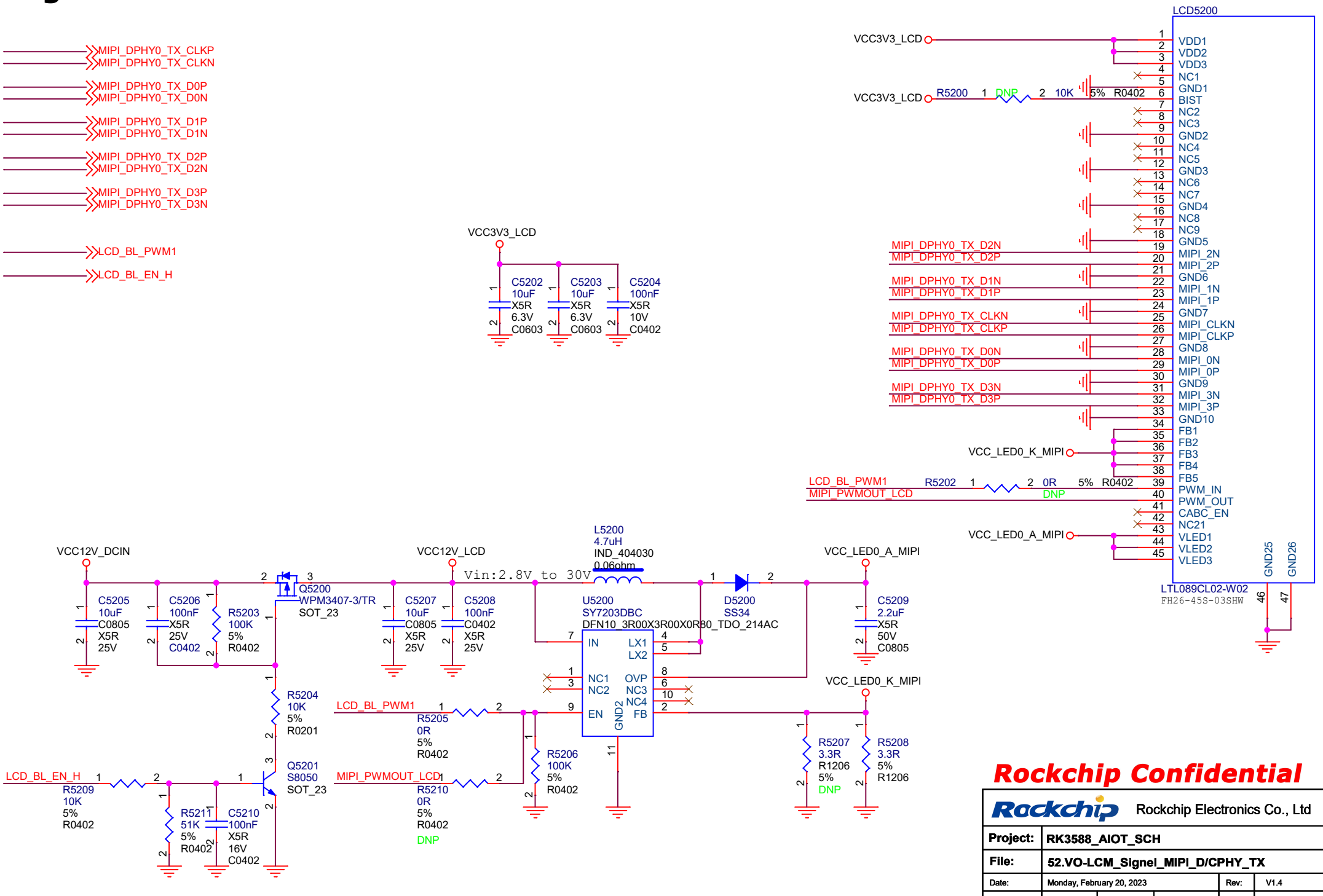
Note:
Requires firmware configuration 1.8V

Note:
SPDIF of RK3588 no support input.

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	51.V1-HDMI IN To MIPI RX(opt2)		
Date:	Wednesday, March 08, 2023	Rev:	V1.4
Designed by:	RZF	Reviewed by: Default	Sheet: 51 of 99

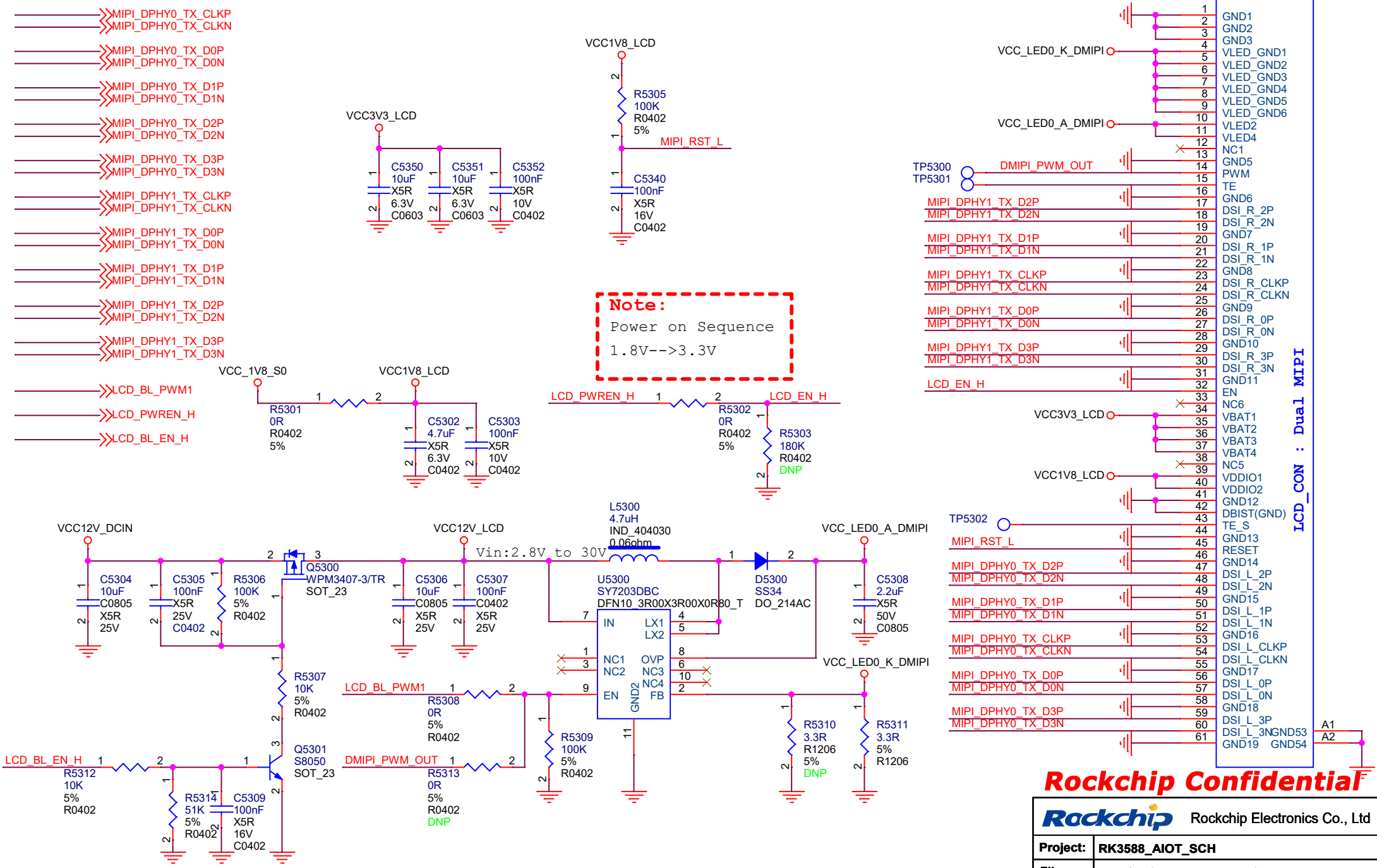
Single-MIPI0 LCM



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	52.VO-LCM_Signel_MIPI_D/CPHY_TX				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	52 of 99

Dual-MIPI LCM

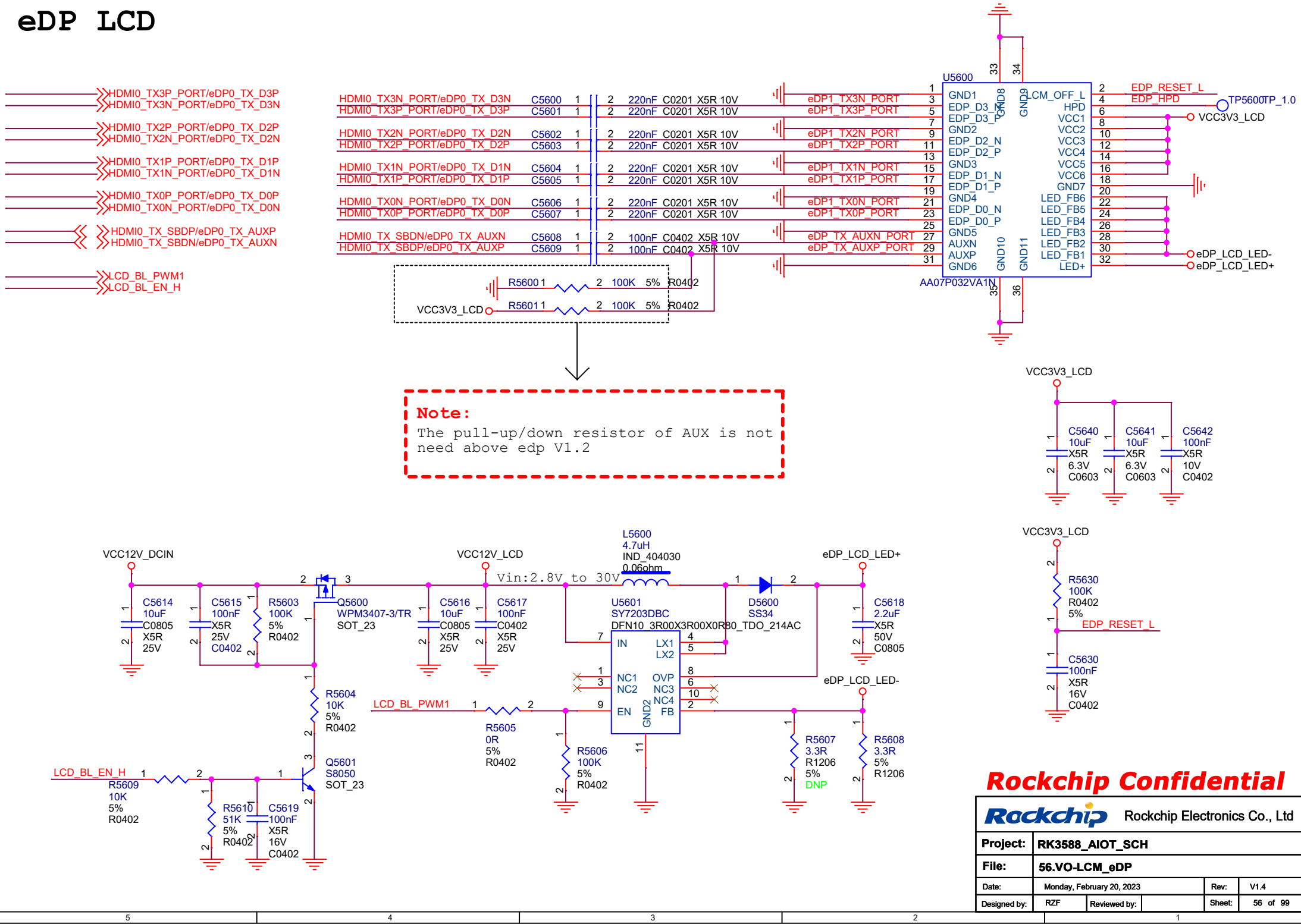


Rockchip Confidential

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	53.VO-LCM_Dual MIPI_D/CPHY TX				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	53 of 99

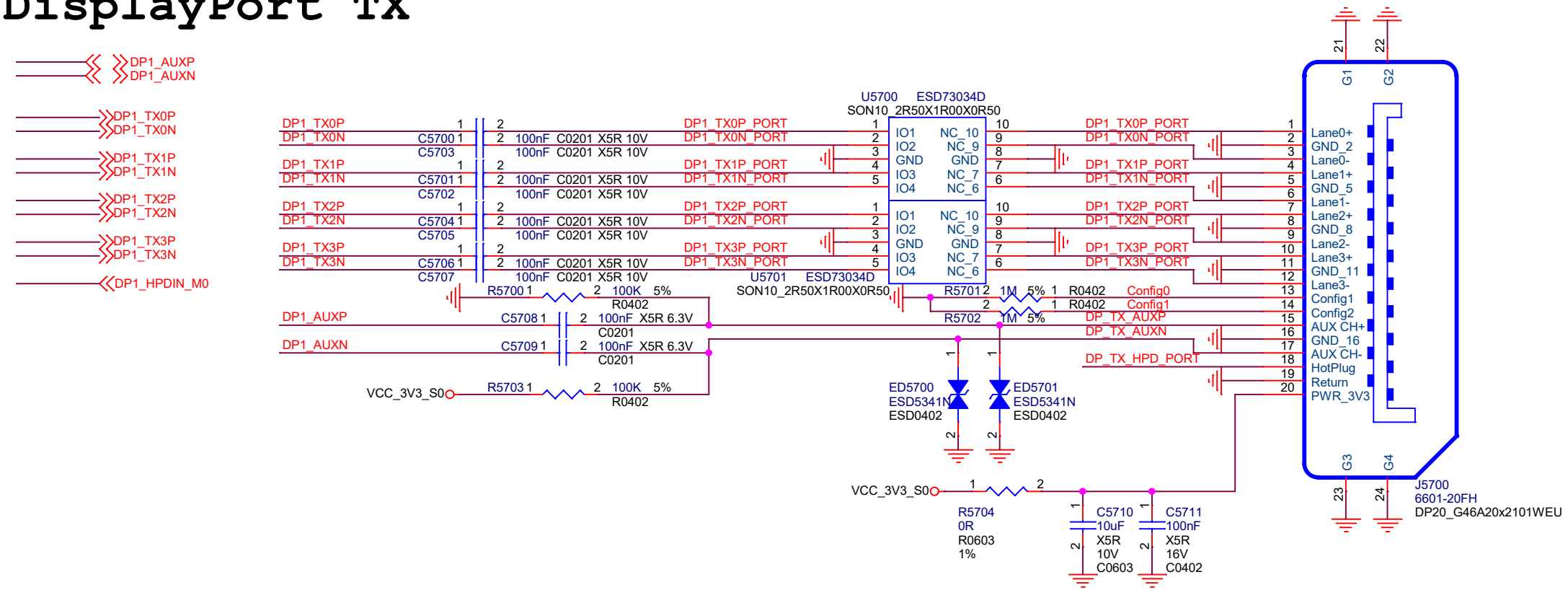
eDP LCD



Rockchip Confidential

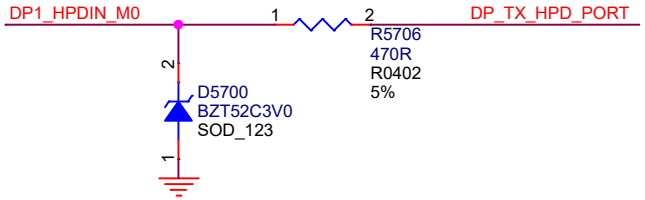
Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	56.VO-LCM_eDP		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	56 of 99

DisplayPort TX



DP_TX_HPD

HPD Voltage:2.25-3.6V

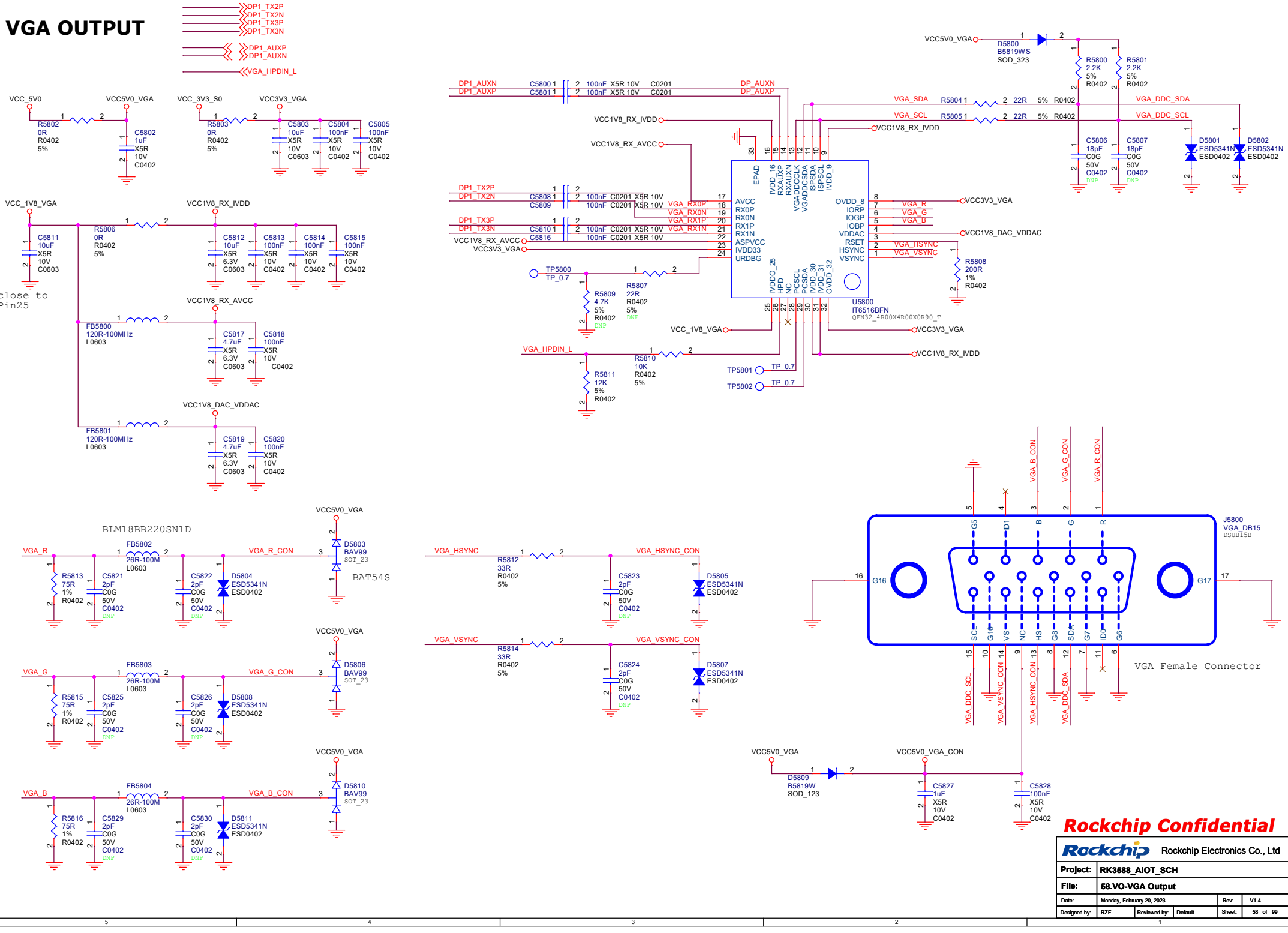


Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	57.VO-DP		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	57 of 99

Rockchip Confidential

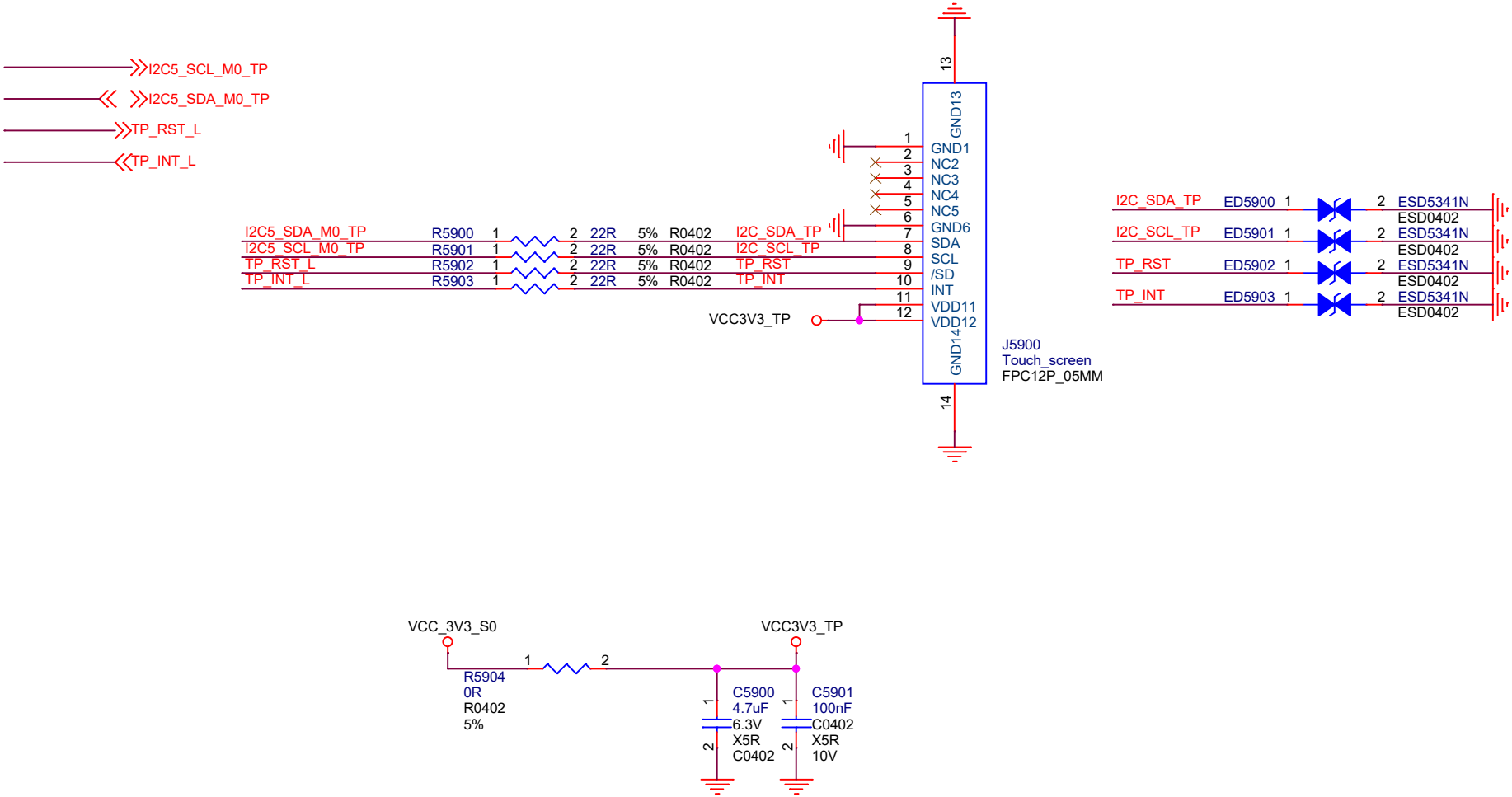
VGA OUTPUT



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	58.VO-VGA Output				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	58 of 99

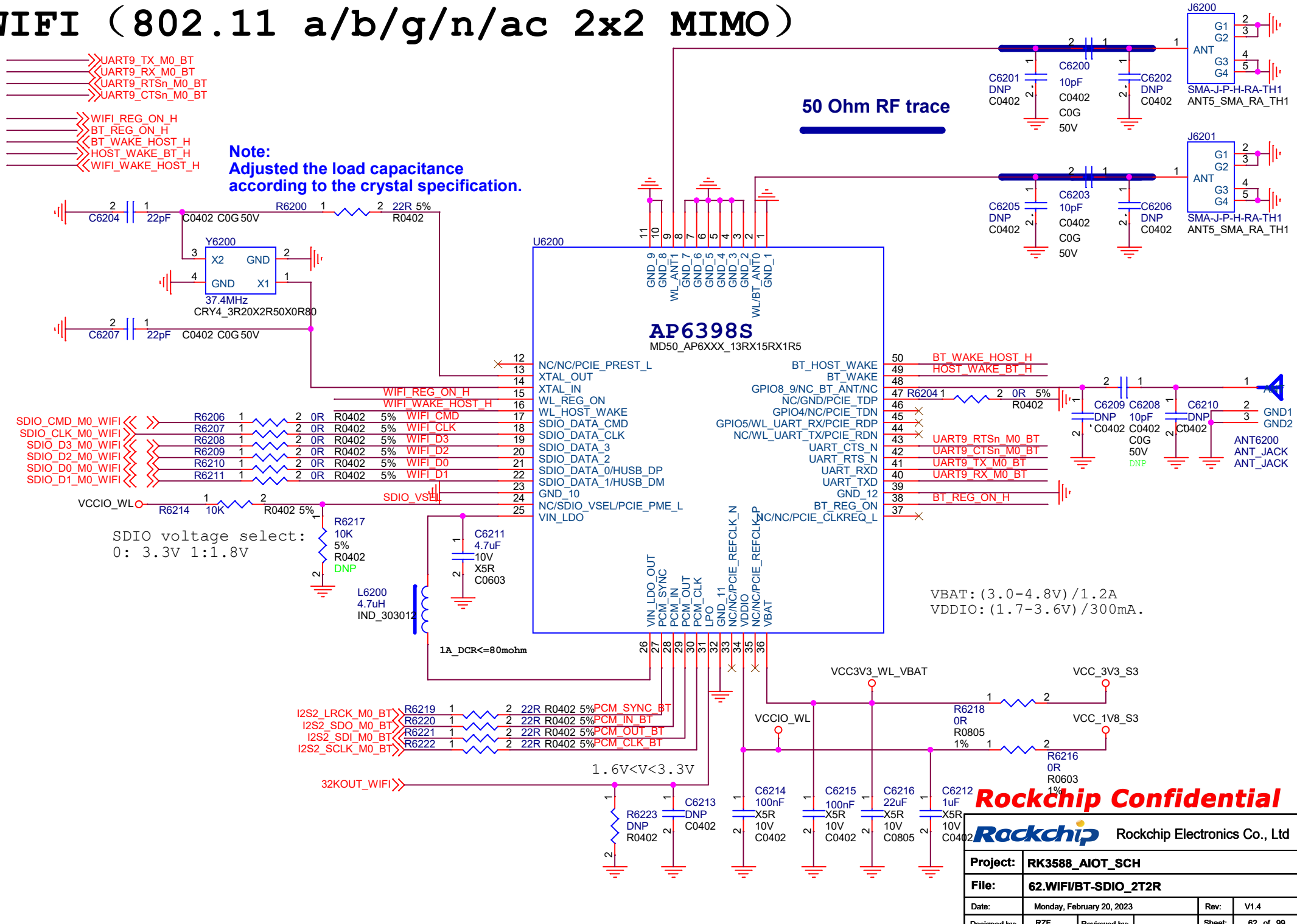
Touch Panel connector



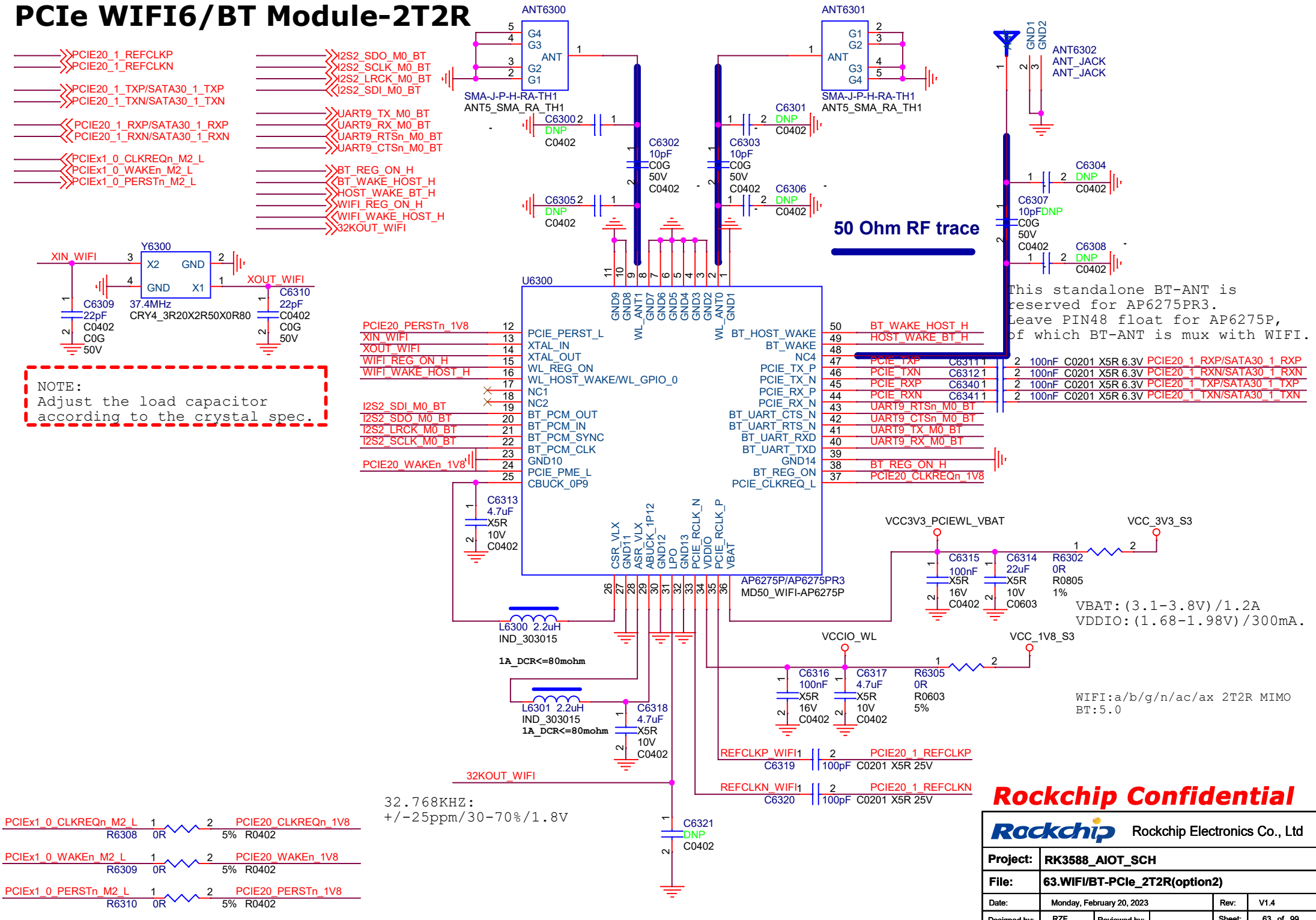
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	59.TP Connector_COF				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	59 of 99

Rockchip Confidential

WIFI（802.11 a/b/g/n/ac 2x2 MIMO）



PCIe WIFI6/BT Module-2T2R



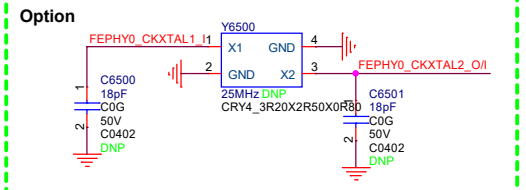
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	63.WIFI/BT-PCIe_2T2R(option2)		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	63 of 99

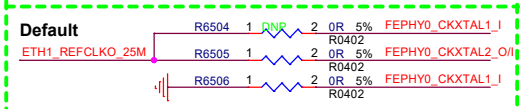
RMII

GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXEN
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXDV_CRS
GMAC1_MCLKINOUT
GMAC1_MDC
GMAC1_MDIO
ETH1_REFCLKO_25M
GMAC1_RSTn_L

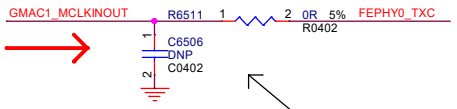
Option

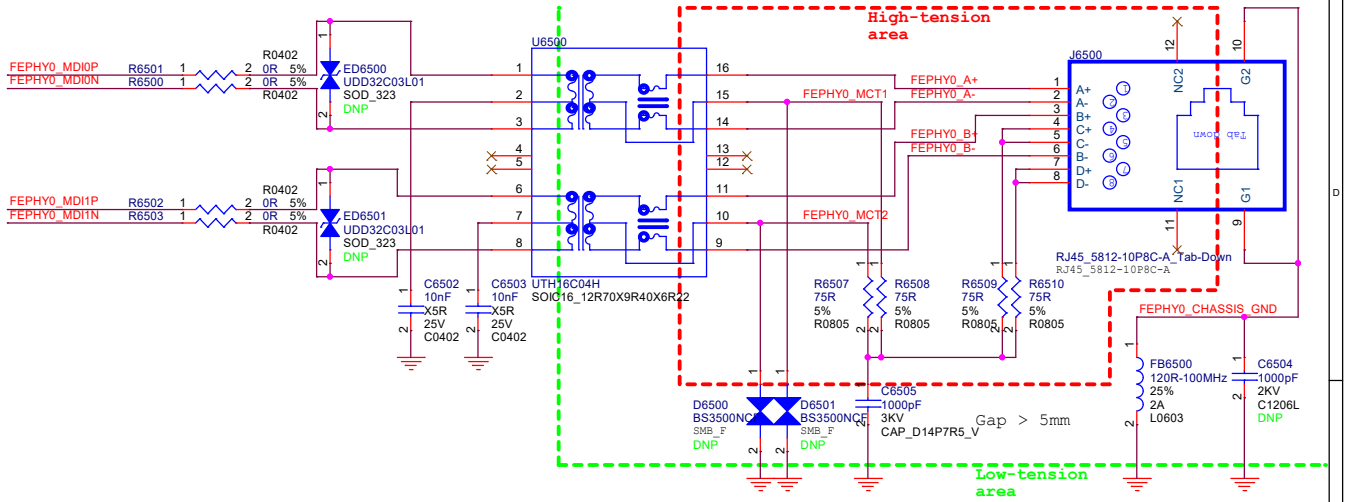


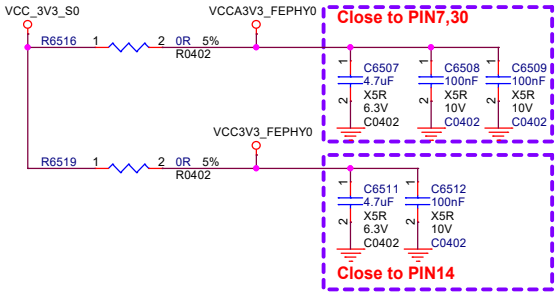
Default

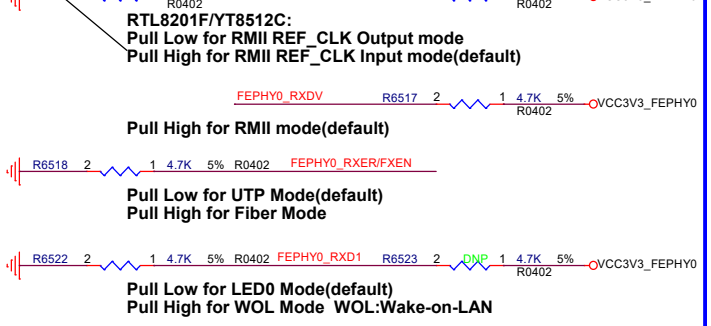


Default: Refclk:MAC output,PHY input

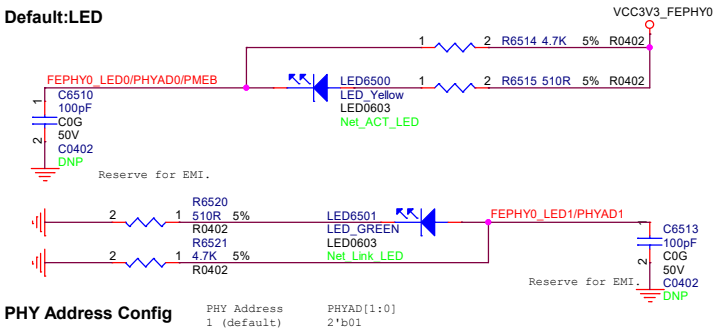






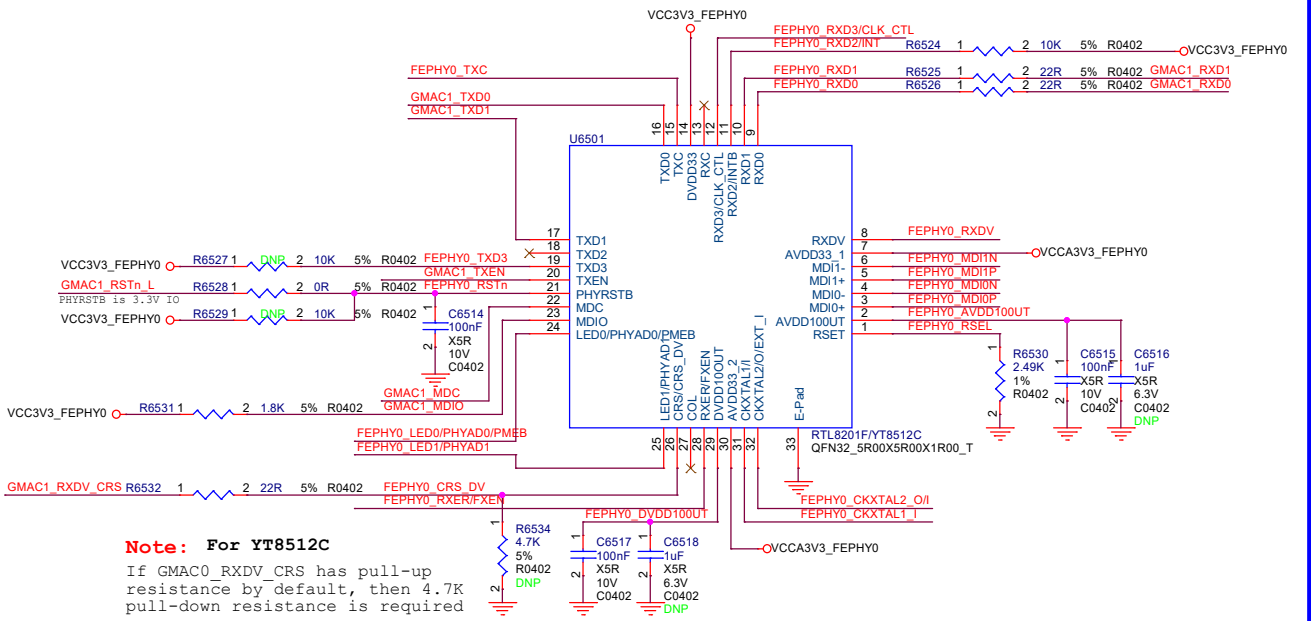


Default:LED



PHY Address Config

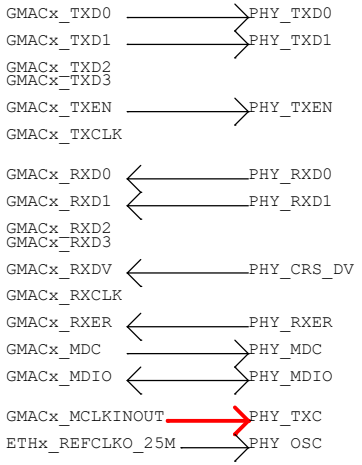
PHY Address	PHYAD[1:0]
1 (default)	2'b01



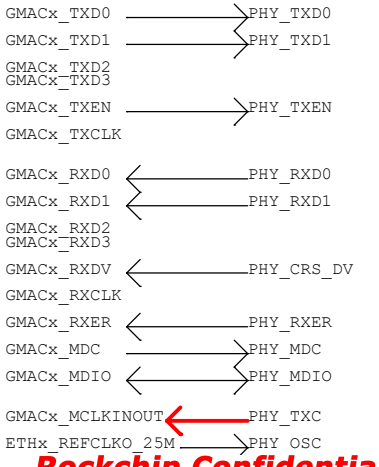
Note: For YT8512C

If GMAC0_RXDV_CRS has pull-up resistance by default, then 4.7K pull-down resistance is required

Default
Refclk:MAC output,PHY input



Refclk:MAC input,PHY output



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	65.Ethernet-RMII(option)				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	65 of 99

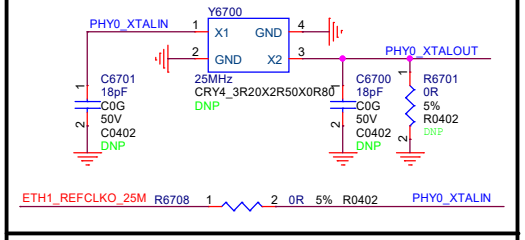
RGMII TO RJ45

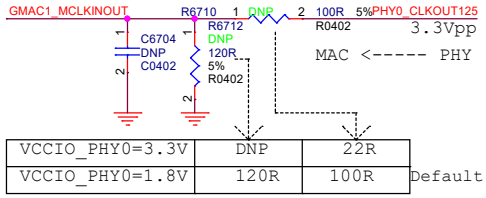
GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXD2
GMAC1_TXD3
GMAC1_TXEN
GMAC1_TXCLK

GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXD2
GMAC1_RXD3
GMAC1_RXDV_CRS

GMAC1_RXCLK
ETH1_REFCLKO_25M
GMAC1_MCLKINOUT
GMAC1_MDC
GMAC1_MDIO

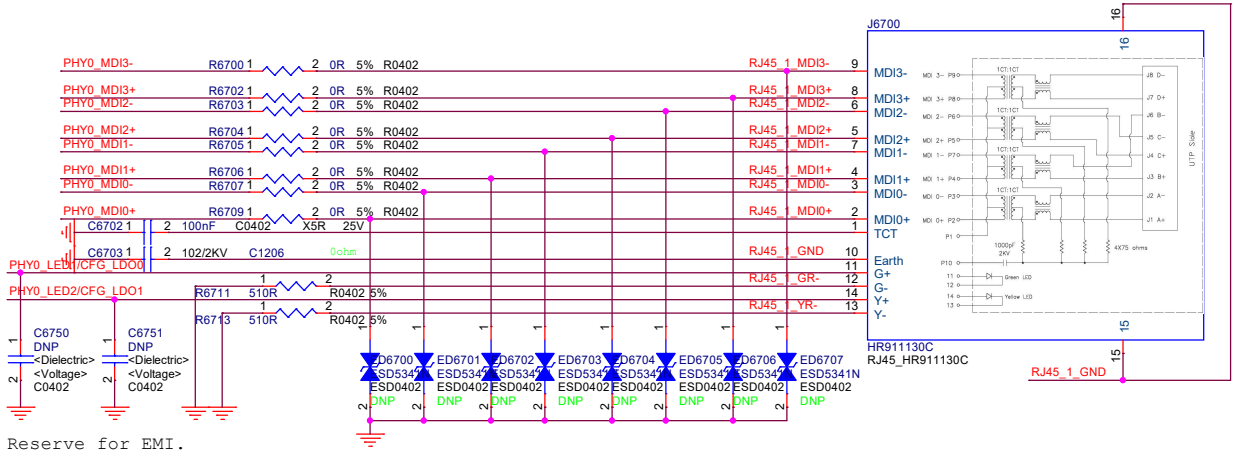
GMAC1_RSTn_L



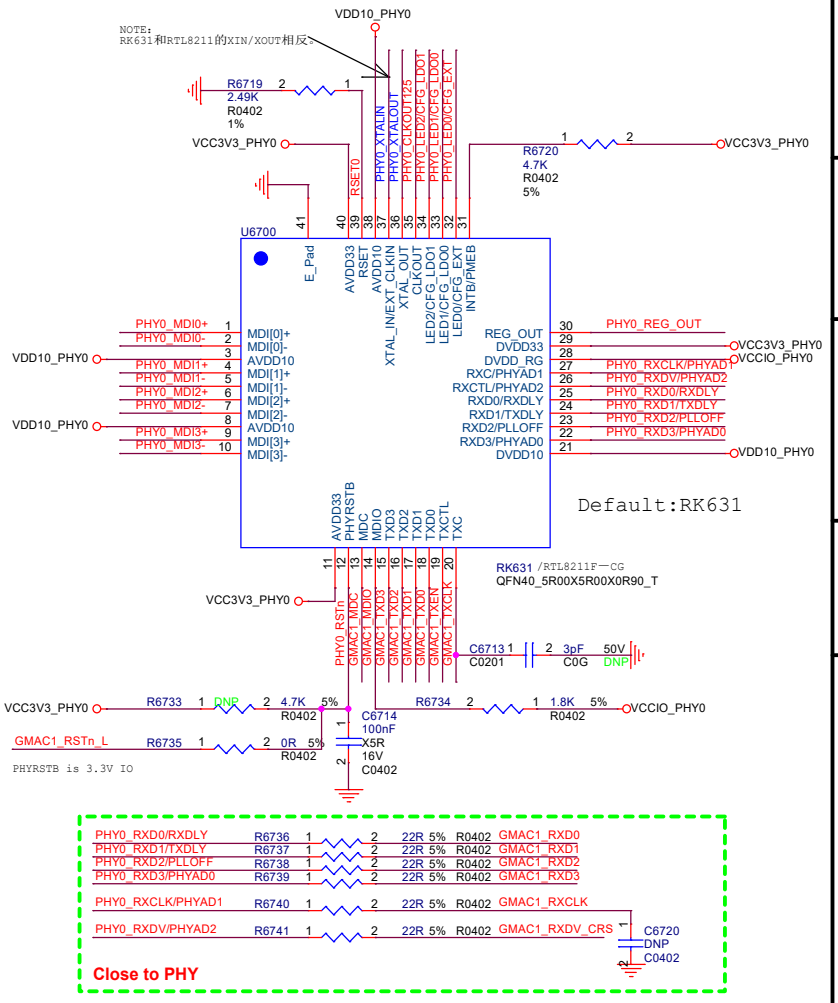


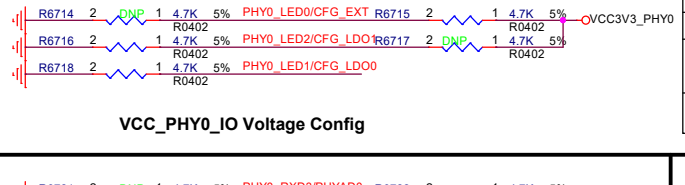
VCCIO_PHY0=3.3V	DNP	22R
VCCIO_PHY0=1.8V	120R	100R

Default



Reserve for EMI.



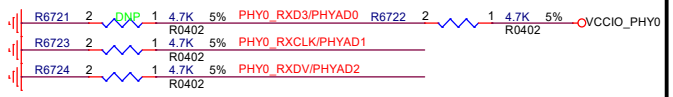


VCC_PHY0_IO Voltage Config

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V(default)	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V	1'b0	2'b10

CFG_EXT:
1:External Power Source for IO pad.
0:Integrated LDO for IO pad

CFG_LDO(1:0)
10:1.8V
00:3.3V



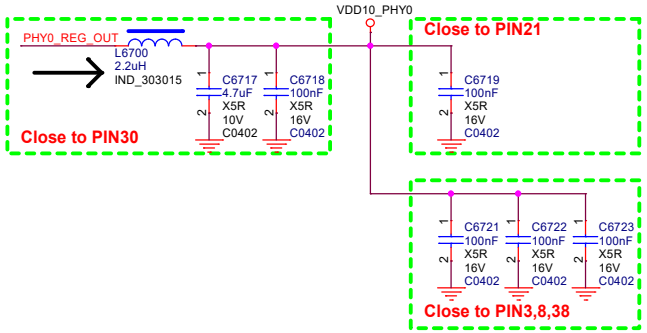
PHY Address Config

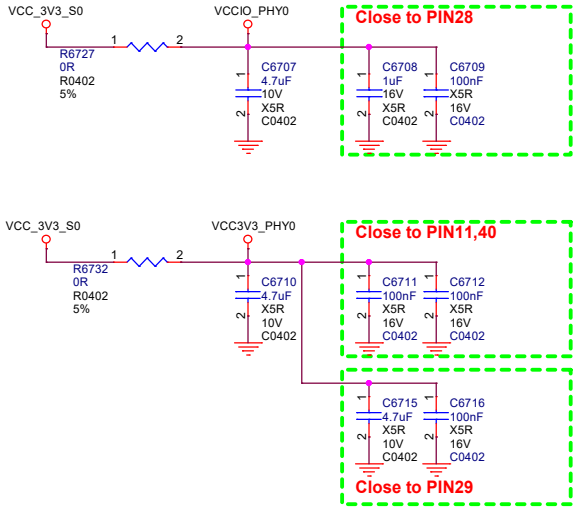
PHY Address	PHYAD[2:0]
1 (default)	3'b001

Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching

Pull-up to disable PLL @ ALDPS mode(Low power mode)

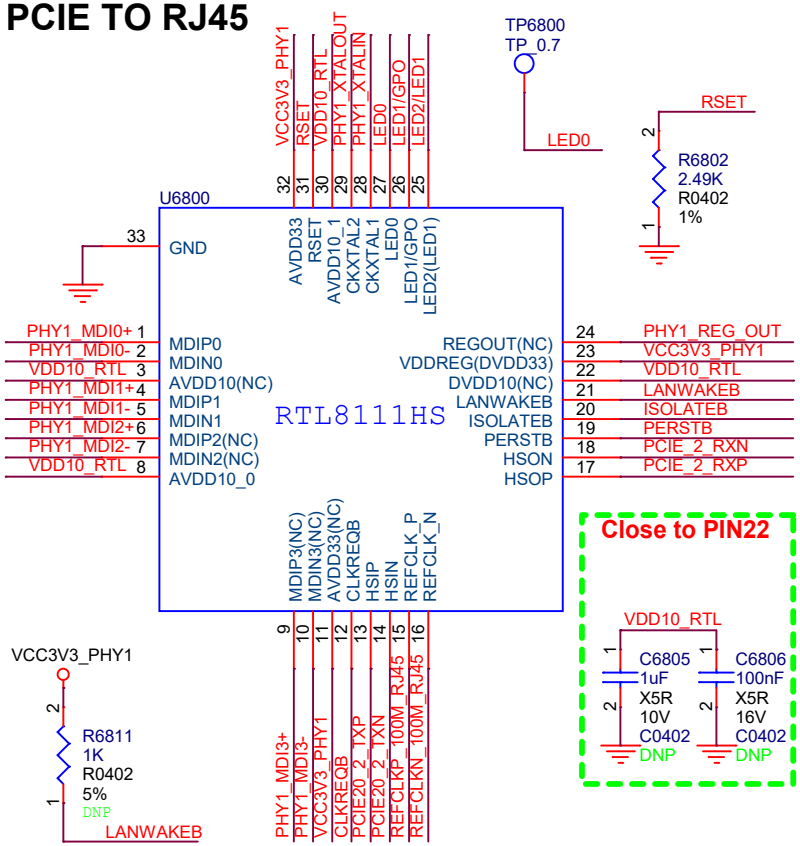


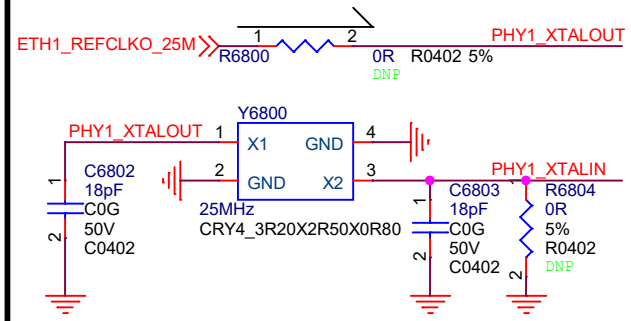


Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH			
File:	67.Ethernet-GPHY_RGMII1			
Date:	Wednesday, March 08, 2023		Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet: 67 of 99

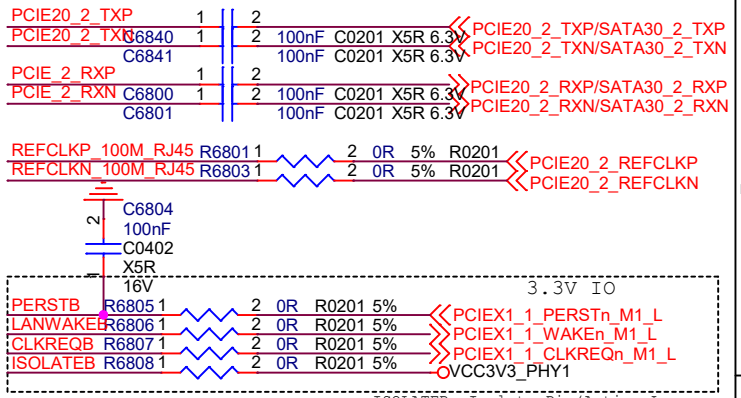
PCIE TO RJ45





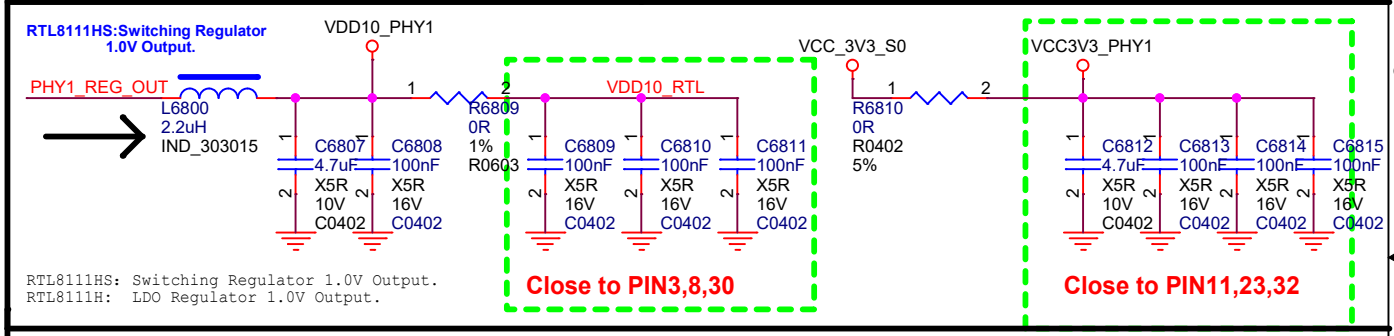
25Mhz Crystal: Stuff Y6800 C6802,No Stuff R6800,R6804
External Clock: Stuff R6804,R6800,No stuff: Y6800,C6802.

CKXTAL1(I): Input of 25Mhz Clock Reference.
CKXTAL2(IO): Input of External Clock Source
Output of 25Mhz Clock Reference.

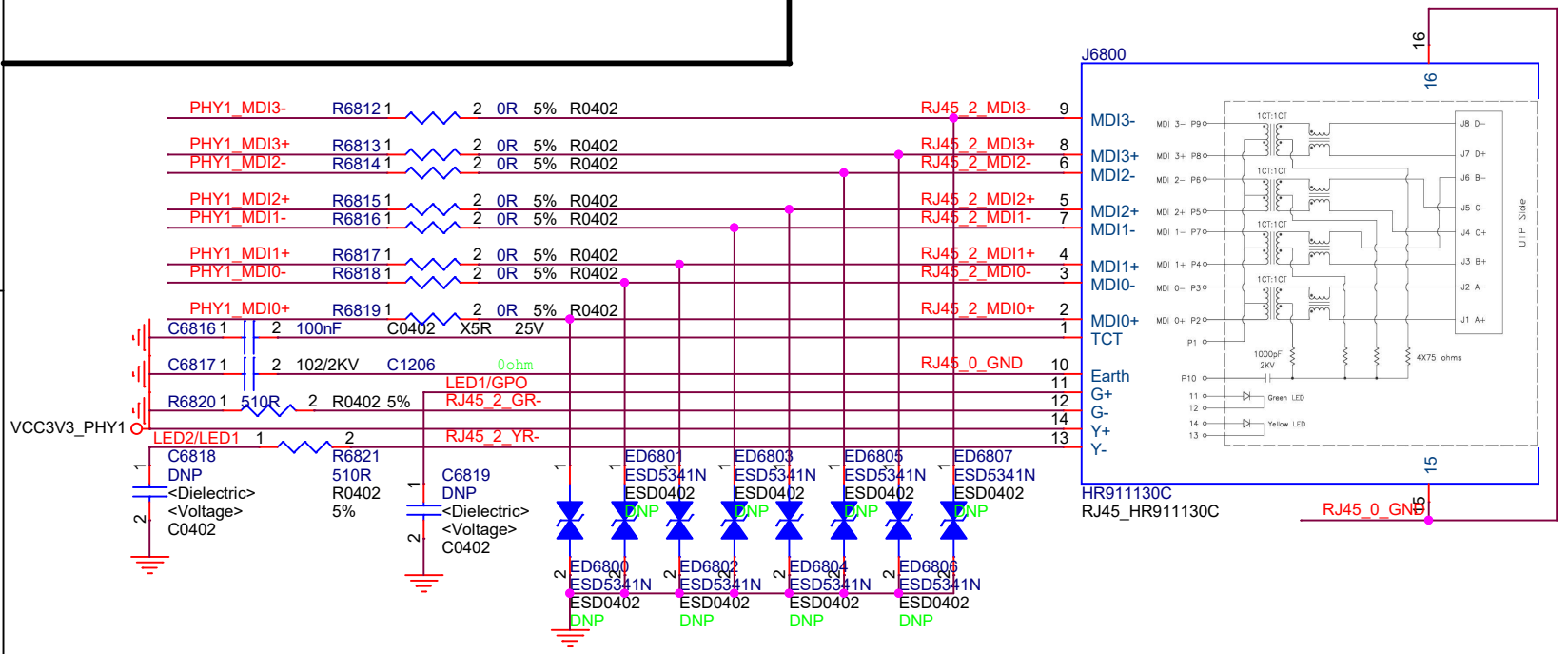


LANWAKEB:Power Management Event (Open Drain;Active Low,1.8V/3.3V compatible input/output mode with a weak external pull resistor)

ISOLATEB :Isolate Pin(Active Low, 1.8V/3,3V compatible input)Used to isolate the RTL8111HS from the PCI Express bus,The RTL8111HS will not drive its PCI Express input as long as the Isolate pin is asserted.



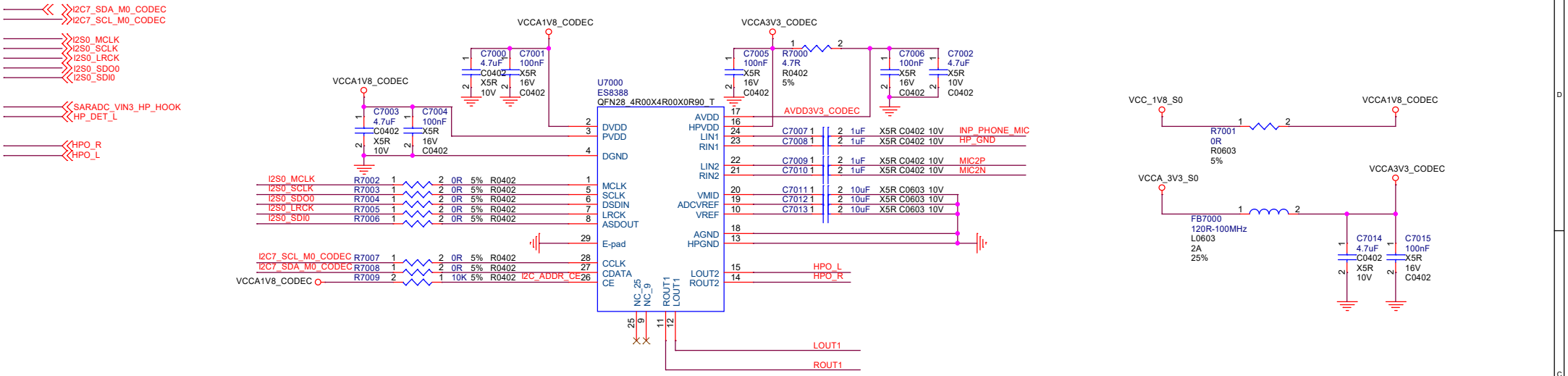
RTL8111HS: Switching Regulator 1.0V Output.
RTL8111H: LDO Regulator 1.0V Output.



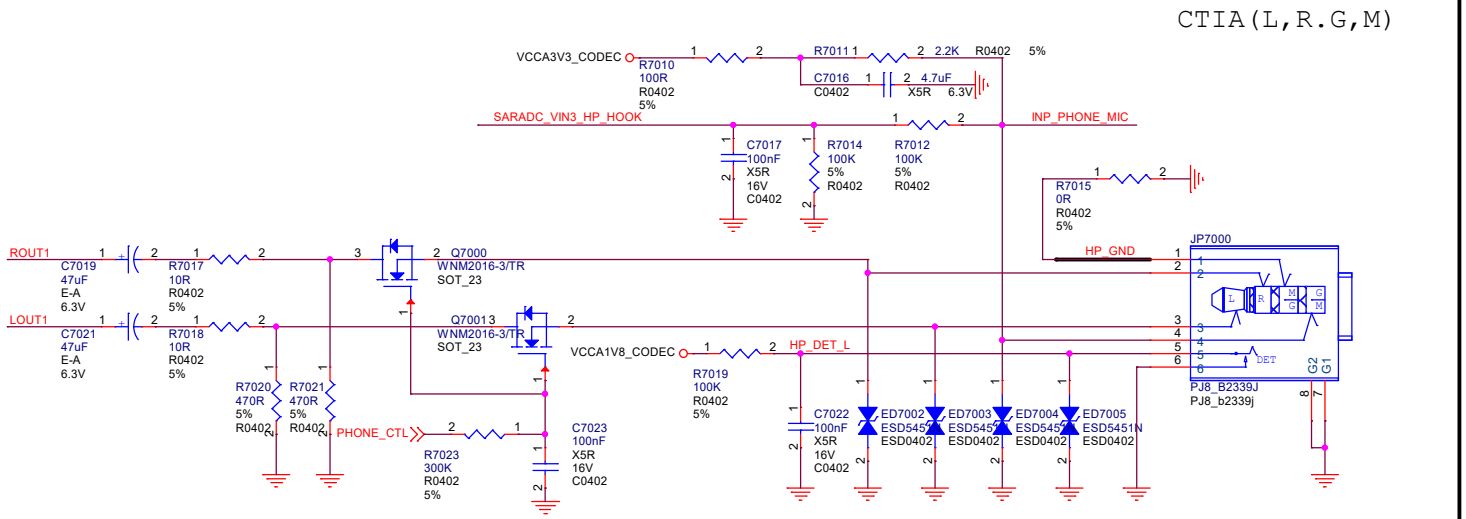
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	68.Ethernet-PCIE				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	68 of 99

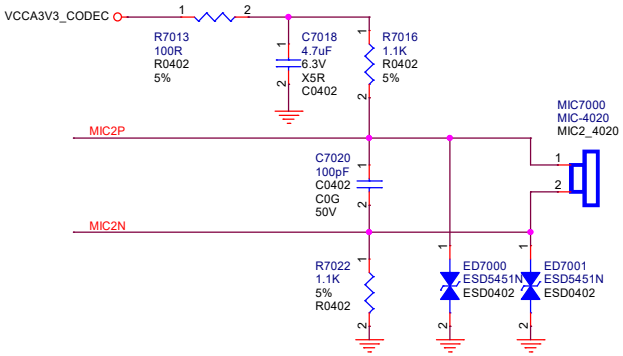
CODEC ES8388



EARPHONE



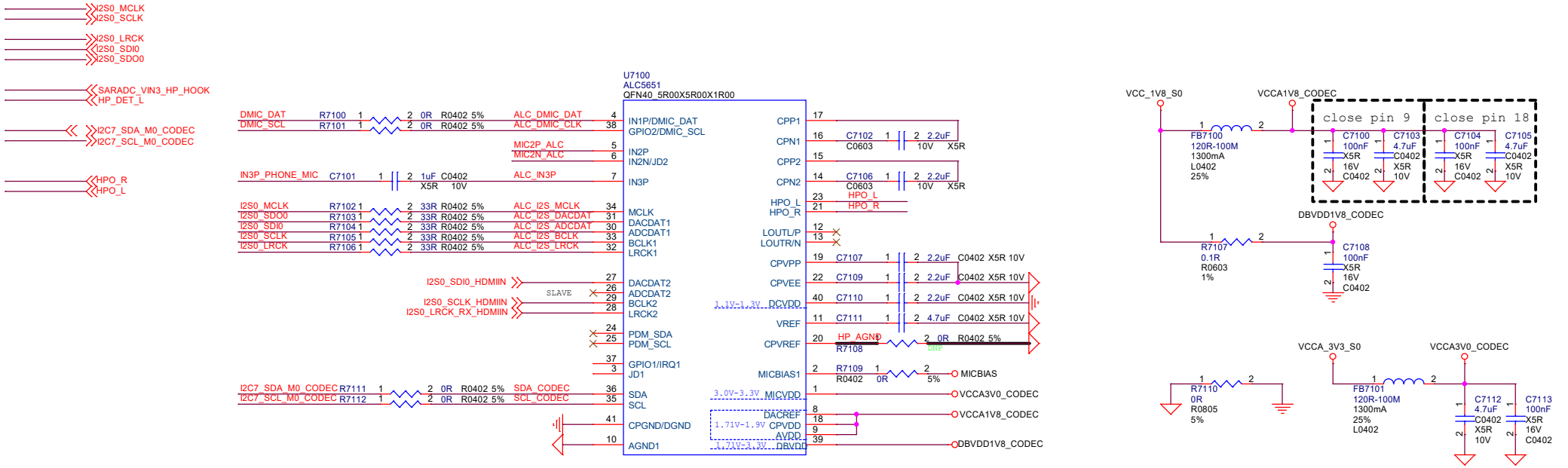
Analog MIC



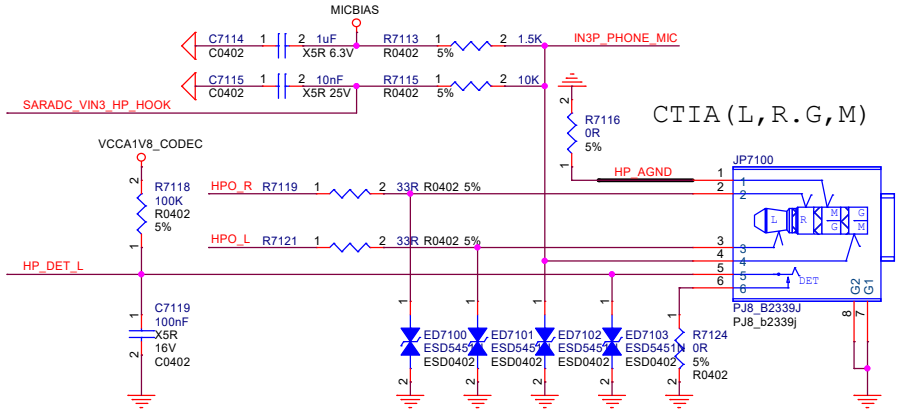
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	Audio Codec-ALC5651				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	70 of 99

CODEC ALC5651



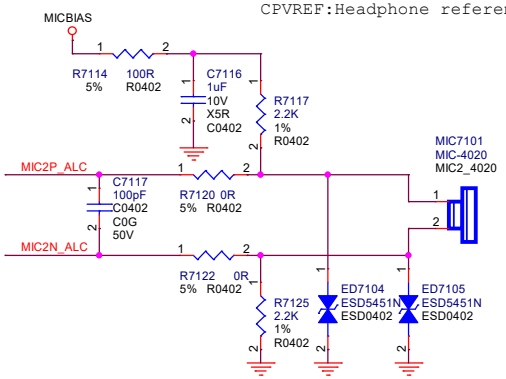
EARPHONE



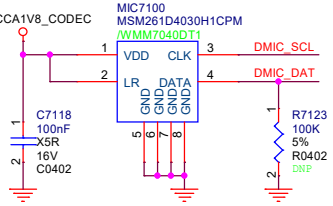
Analog MIC

Power Sequence:
DBVDD-MICVDD
DBVDD<150mA
MICVDD<10mA

CPVREF:Headphone reference ground.



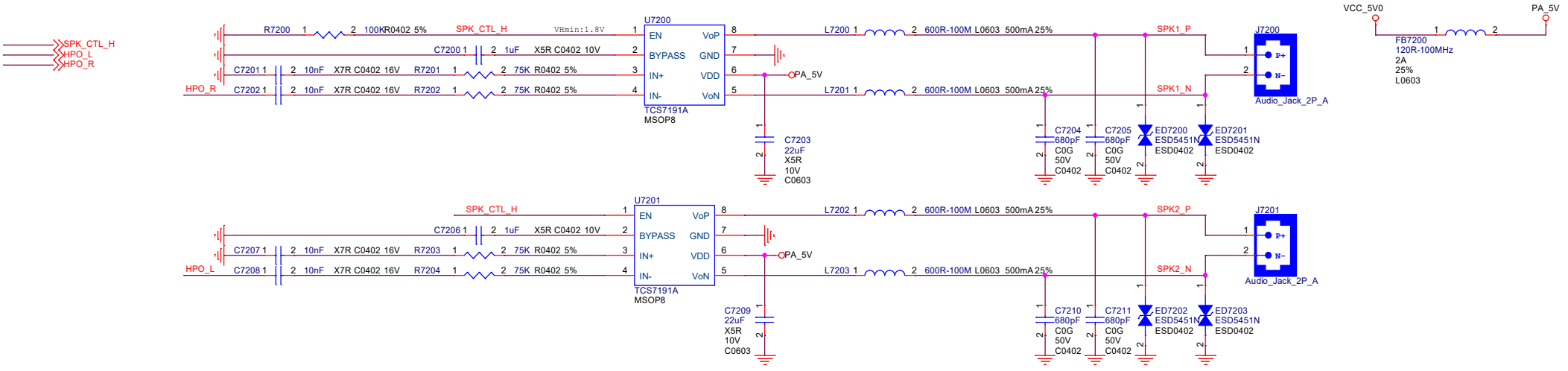
DIGITAL MIC



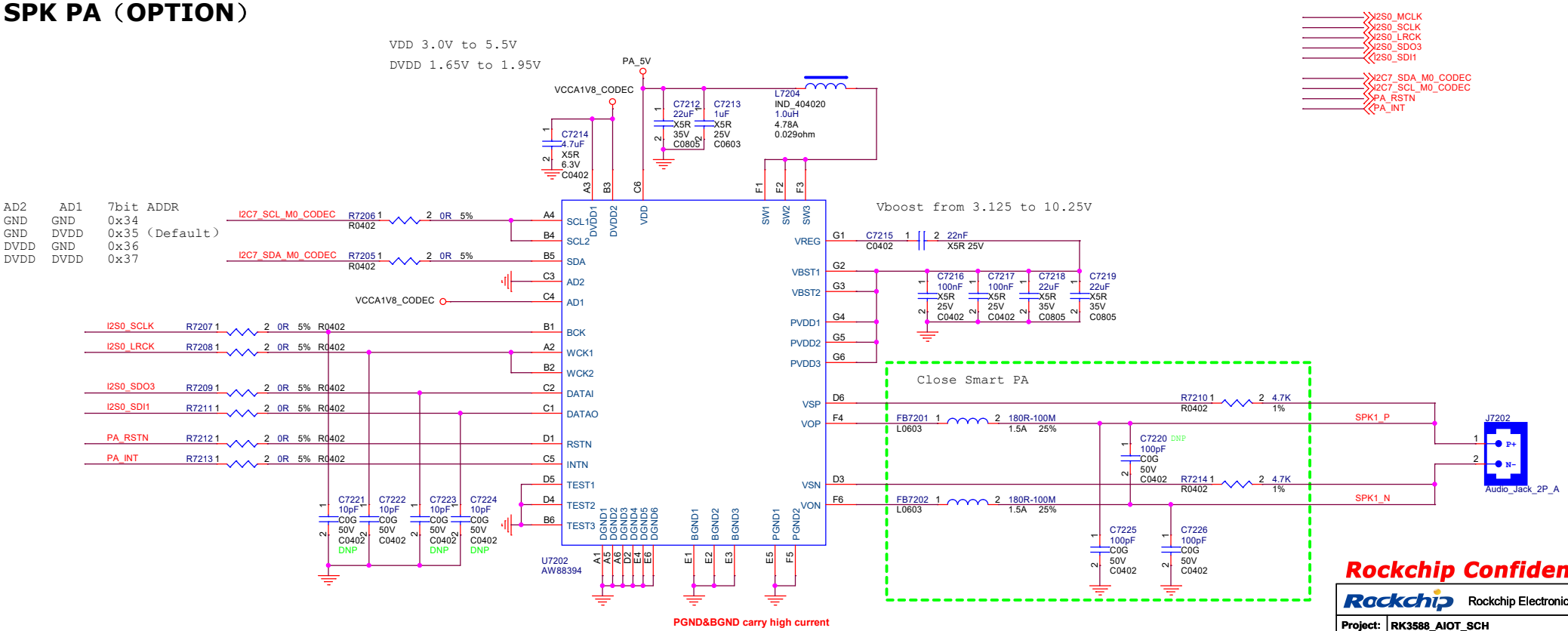
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	71.Audio Codec(option)				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	71 of 99

Rockchip Confidential

SPK PA（Default））

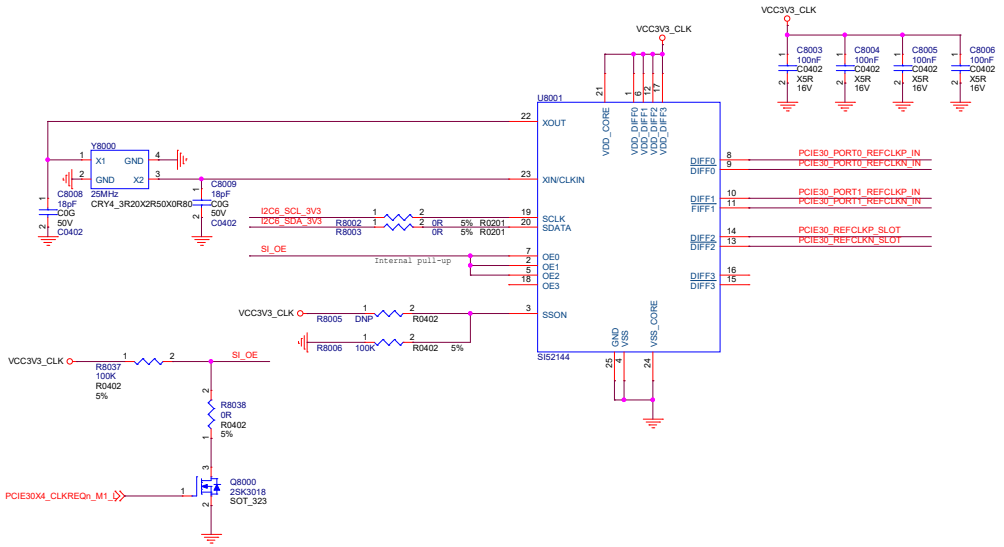


SPK PA（OPTION）

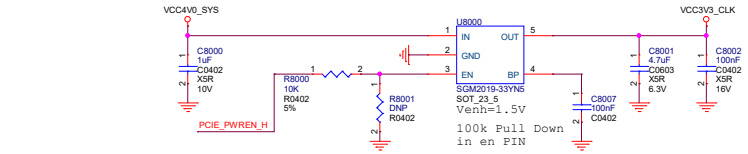


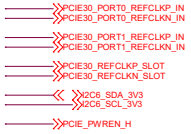
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	Audio Codec-ALC5651		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by:	Sheet:	72 of 99

Crystal Generator(OPTION0)



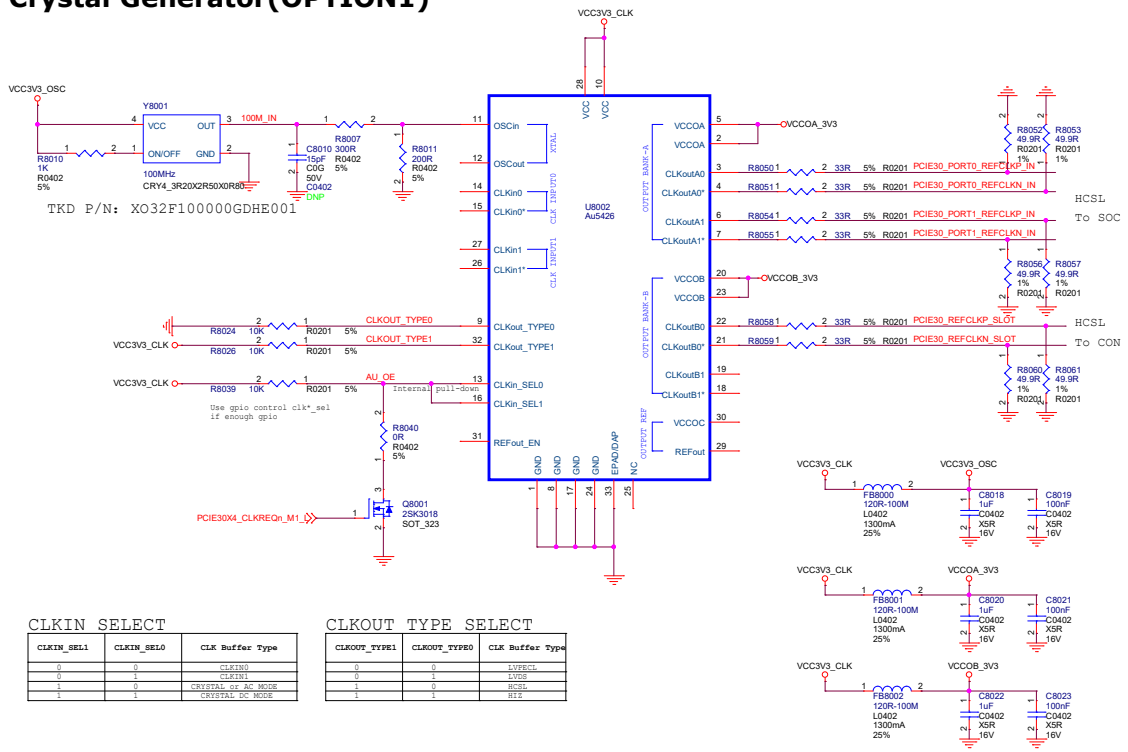
PCIe3.0 POWER





Note:
Please select one option

Crystal Generator(OPTION1)



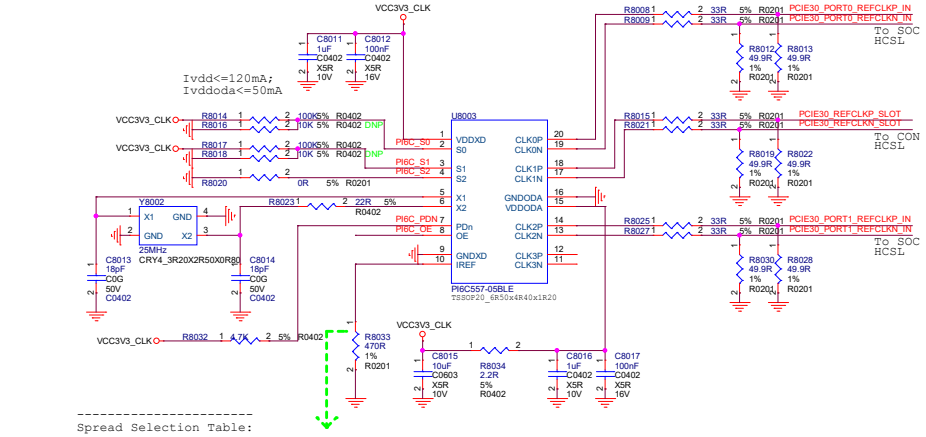
CLKIN SELECT

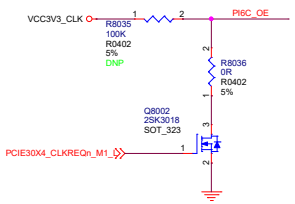
CLKIN_SEL1	CLKIN_SEL0	CLK Buffer Type
0	0	CLKIN0
0	1	CLKIN1
1	0	CRYSTAL OF AC MODE
1	1	CRYSTAL DC MODE

CLKOUT TYPE SELECT

CLKOUT_TYPE1	CLKOUT_TYPE0	CLK Buffer Type
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	HIZ

Crystal Generator(OPTION2)

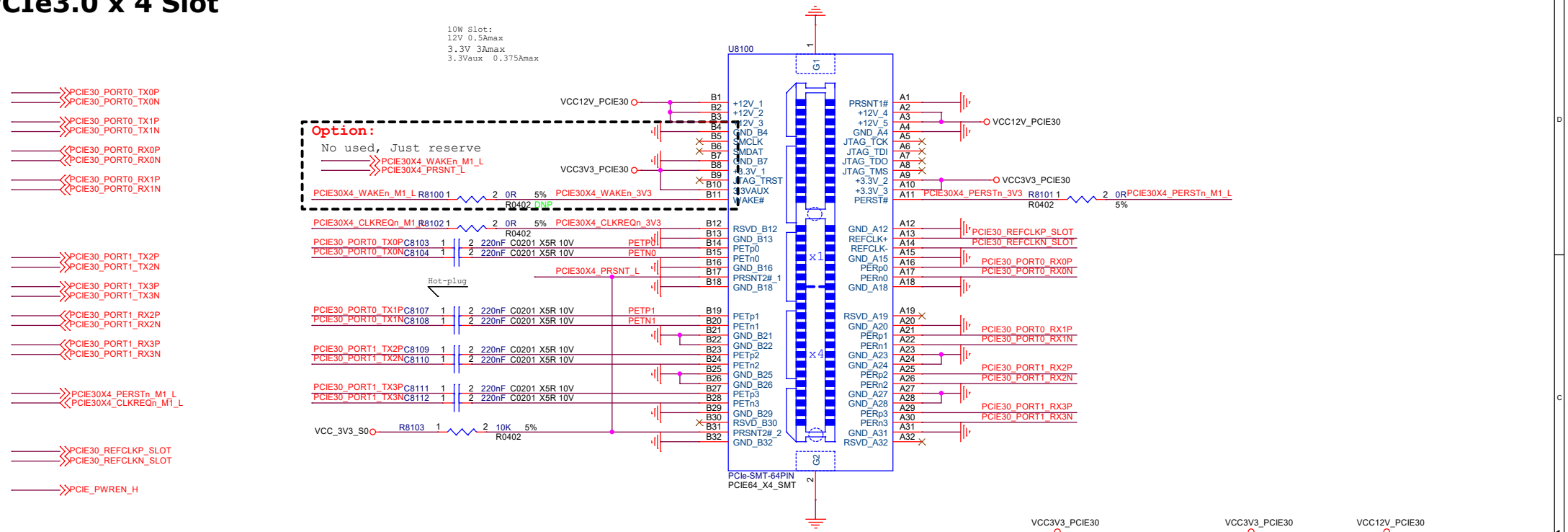




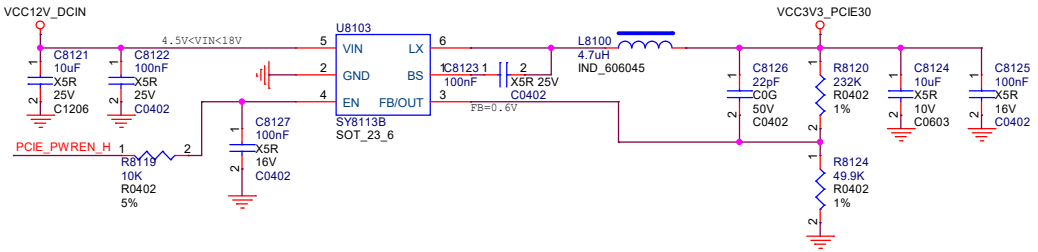
Rockchip Confidential

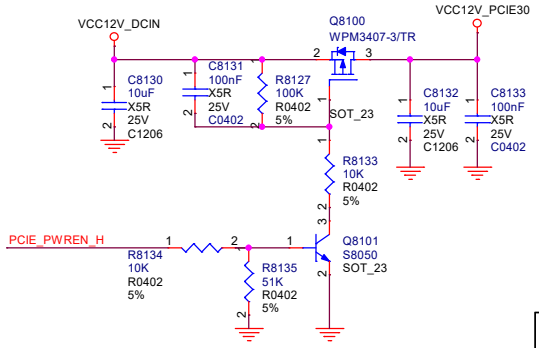
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	80.PCIE-PCIE3.0 CLK GENERATOR		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by:	RZF	Reviewed by:	Sheet: 80 of 99

PCIe3.0 x 4 Slot



PCIe3.0 POWER

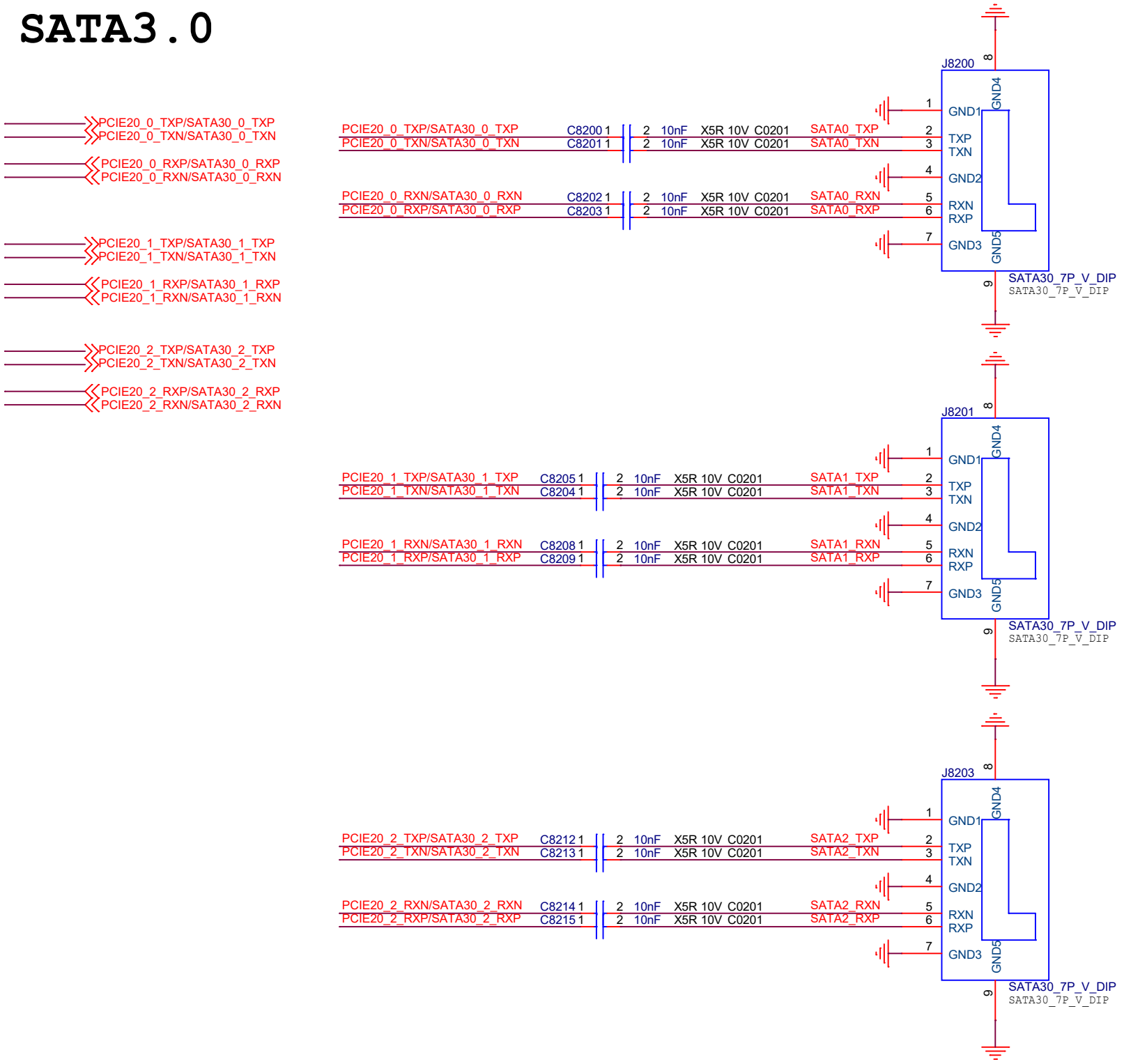




Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	81.PCIE-PCIE3.0_Slot				
Date:	Monday, February 20, 2023		Rev:	V1.4	
Designed by:	RZF	Reviewed by:		Sheet:	81 of 99

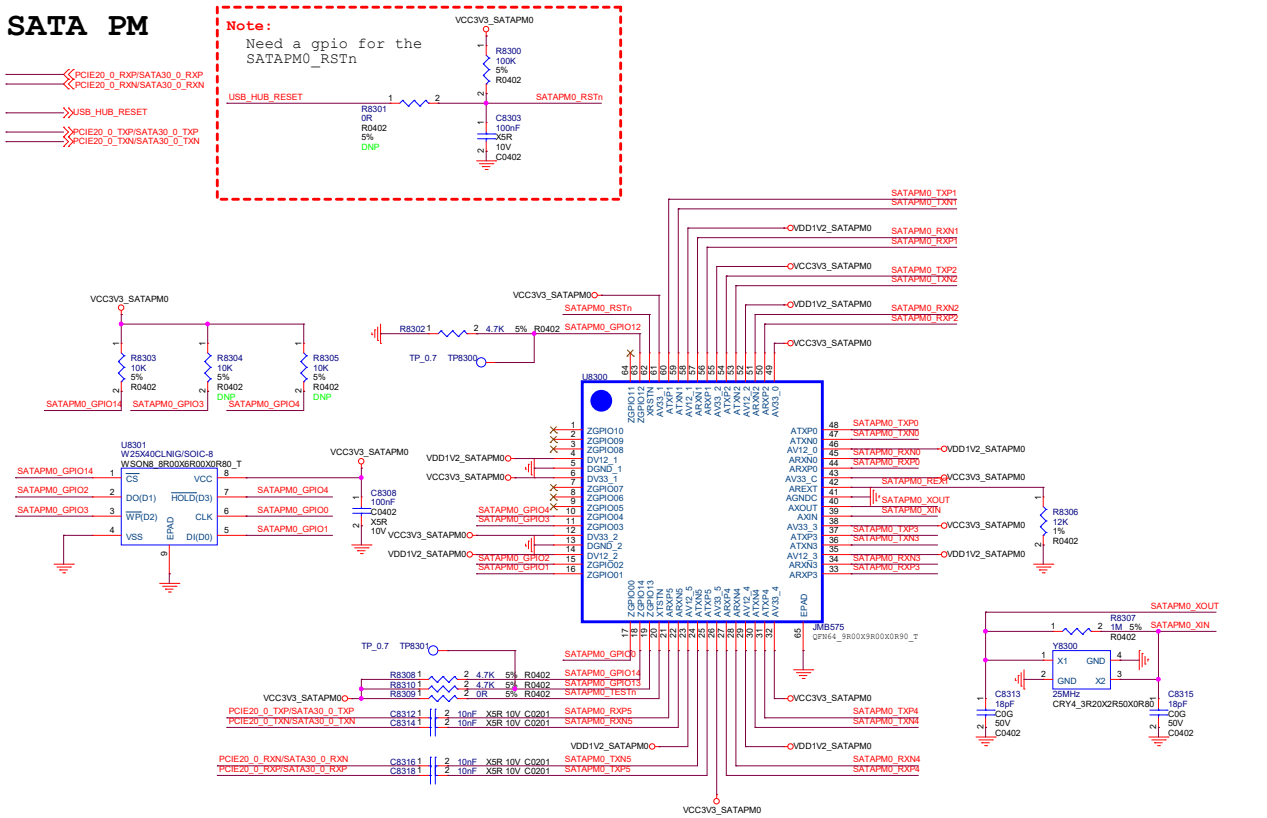
SATA3.0

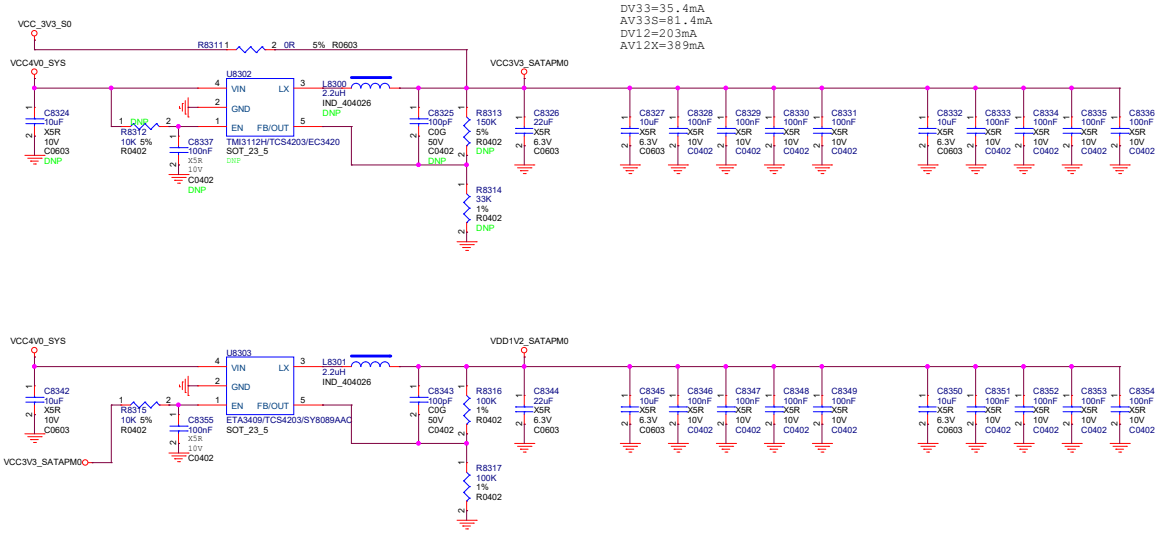


Rockchip Confidential

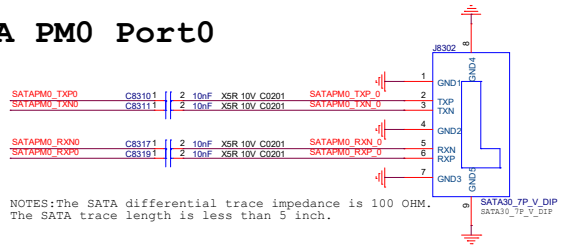
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	82.SATA-SATA3.0 Slot_7P				
Date:	Friday, March 03, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	82 of 99

SATA PM



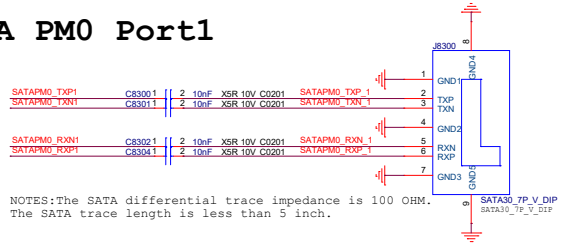


SATA PM0 Port0



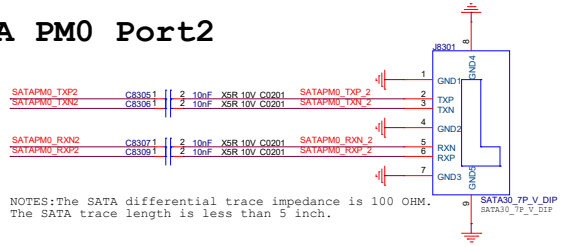
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port1



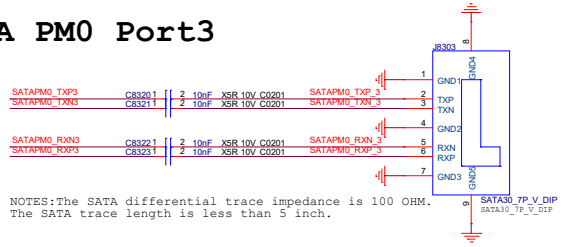
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port2



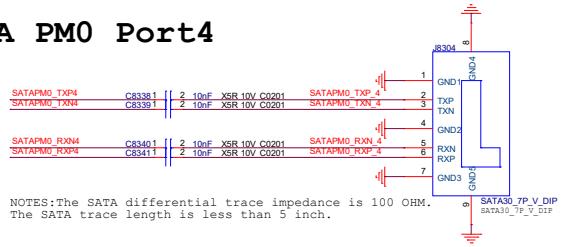
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port3



NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

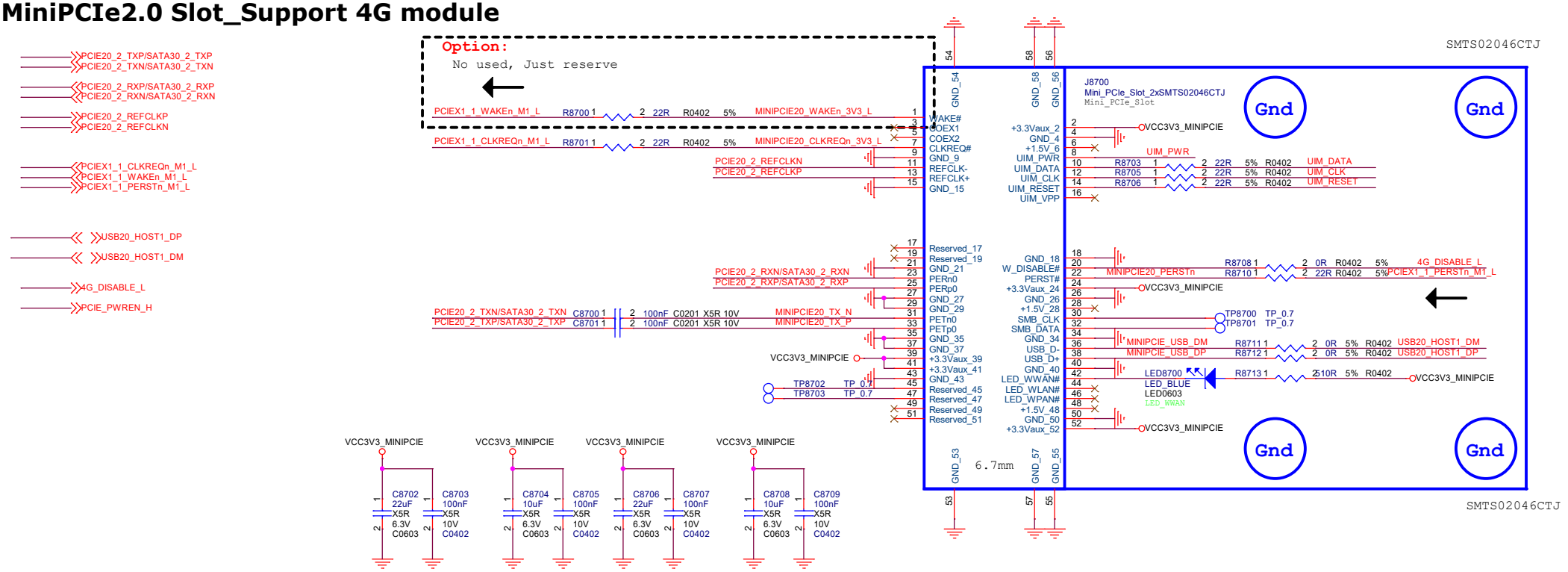
SATA PM0 Port4



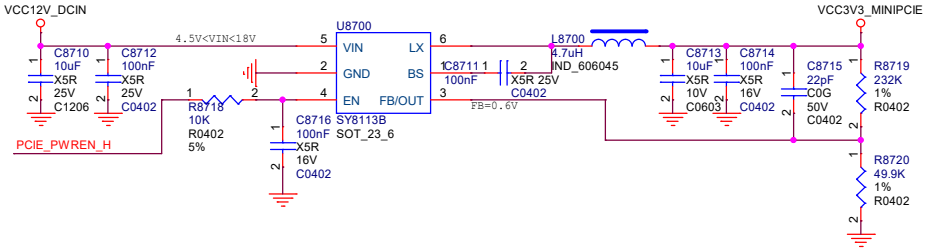
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	83.SATA-SATA PM0(option)		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by:	RZF	Reviewed by: Default	Sheet: 83 of 99

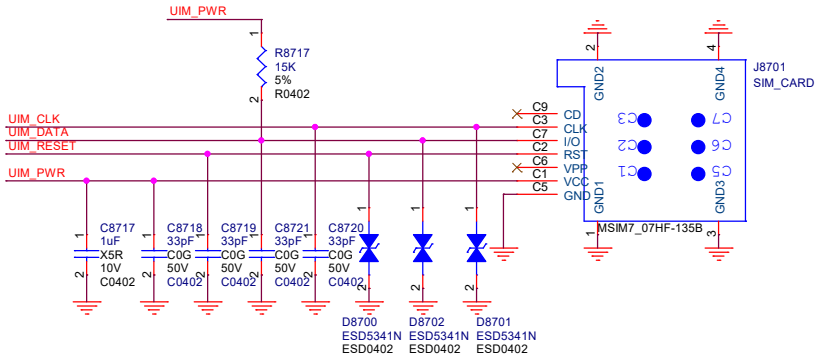
MiniPCIe2.0 Slot_Support 4G module



MiniPCIe2.0 Slot Power



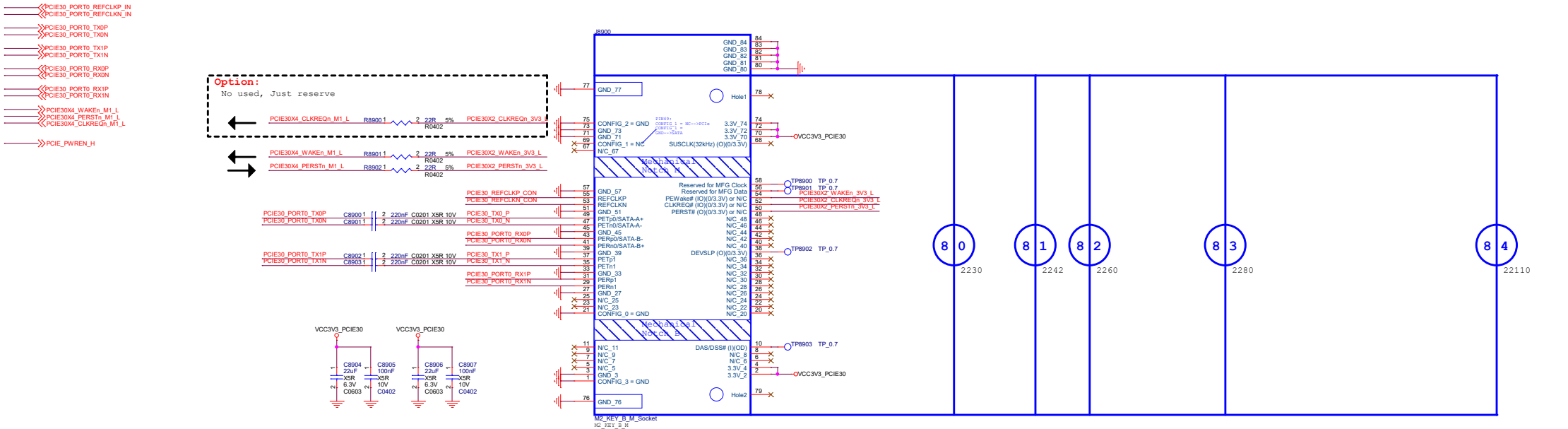
Sim Card



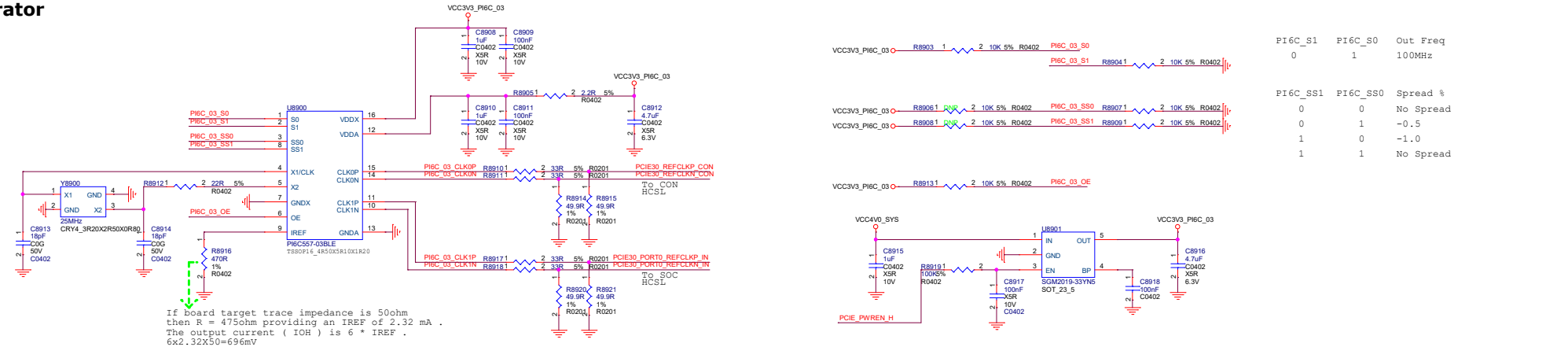
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	87.MiniPCIe2.0 Slot(option)				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:	Default	Sheet:	87 of 99

M.2_PCIe3.0 x 2Lanes



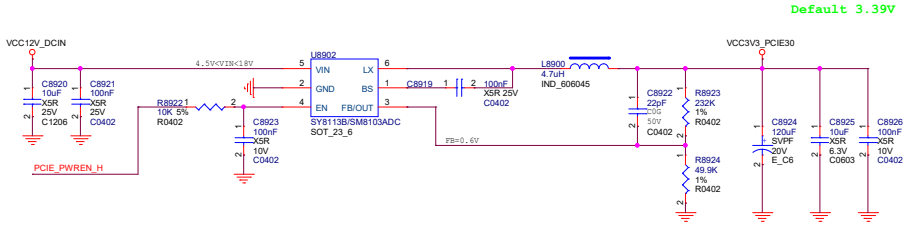
Crystal Generator



PI6C_S1	PI6C_S0	Out Freq
0	1	100MHz

PI6C_SS1	PI6C_SS0	Spread %
0	0	No Spread
0	1	-0.5
1	0	-1.0
1	1	No Spread

M.2 Power

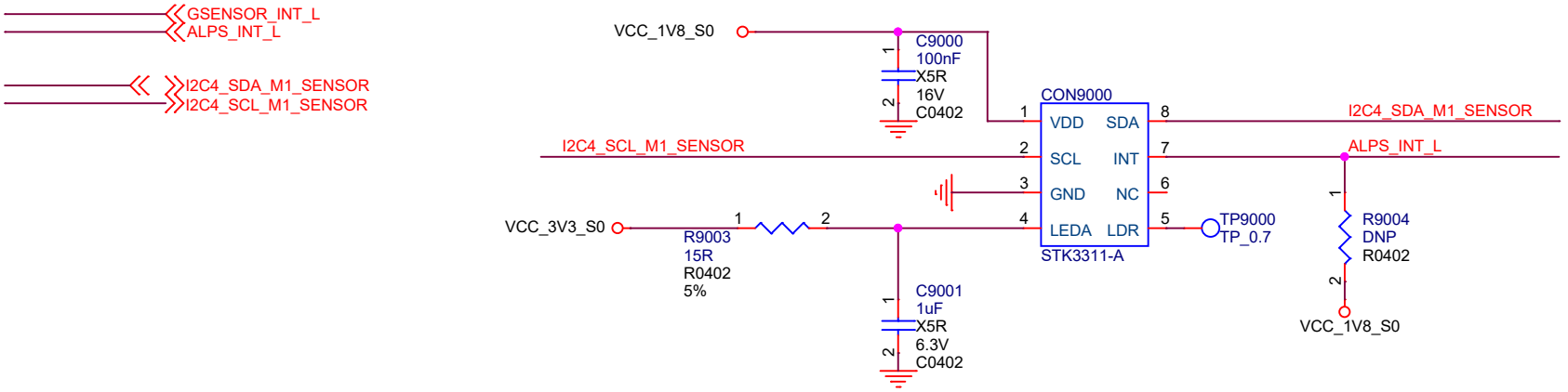


Rockchip Confidential

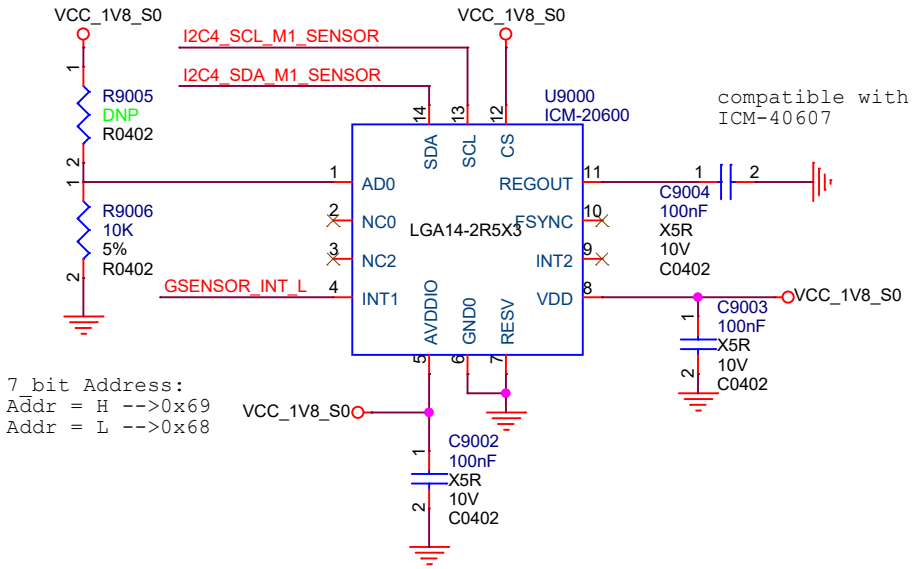
Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	89.PCIE-M.2(option)		
Date:	Monday, February 20, 2023	Rev:	V1.4
Designed by: RZF	Reviewed by: Default	Sheet:	89 of 99

Sensor

Ambient Light+Proximity Sensor



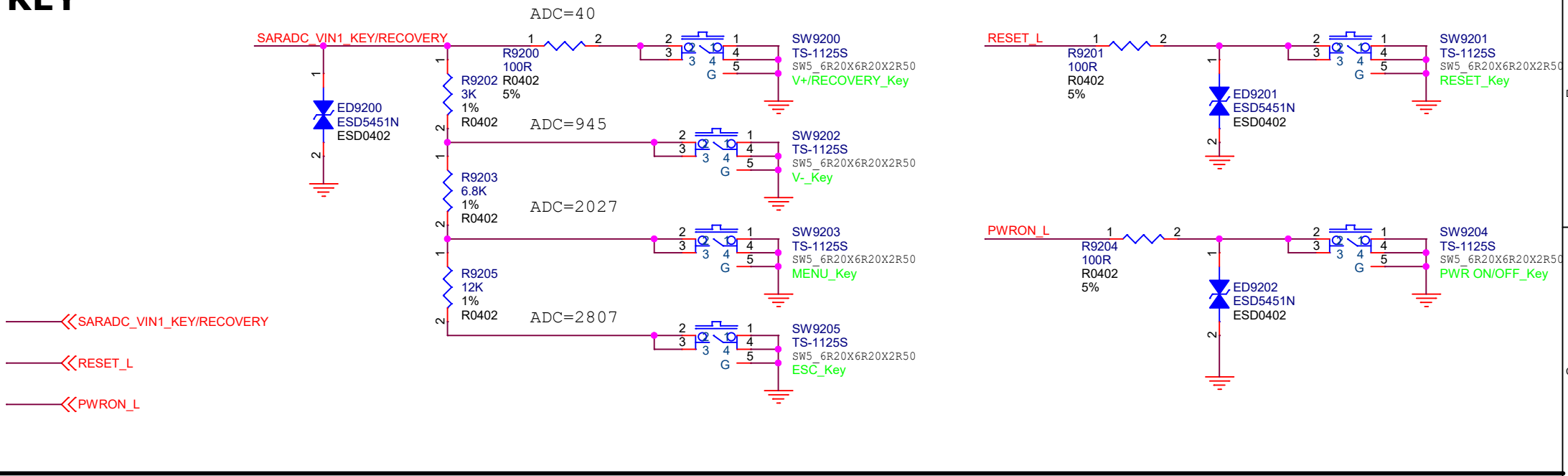
Gyroscope+G-sensor

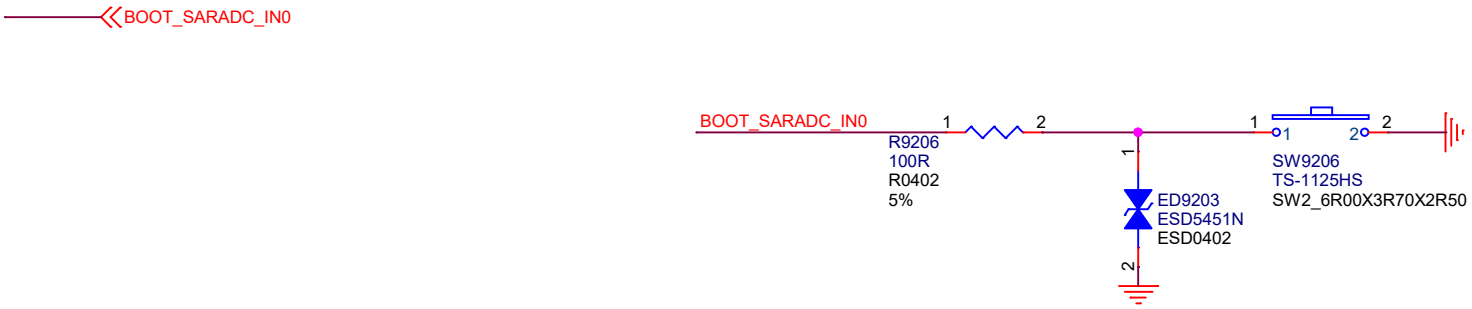


Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	90.SENSOR				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	90 of 99

KEY



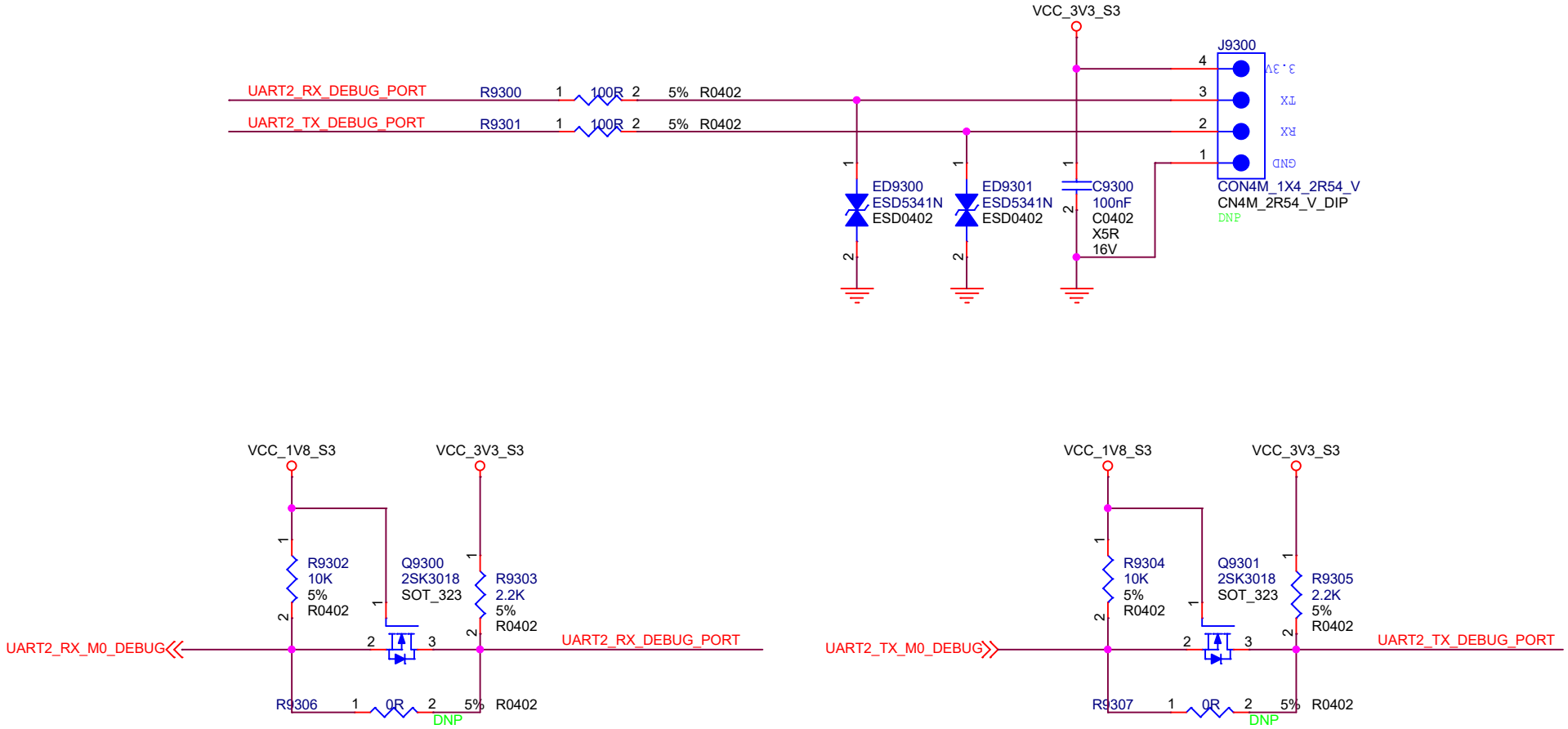


Note:
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	92.KEY Array				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	92 of 99

UART TO USB(DEBUG)



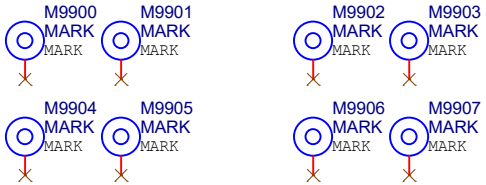
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	93.Debug UART				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	93 of 99

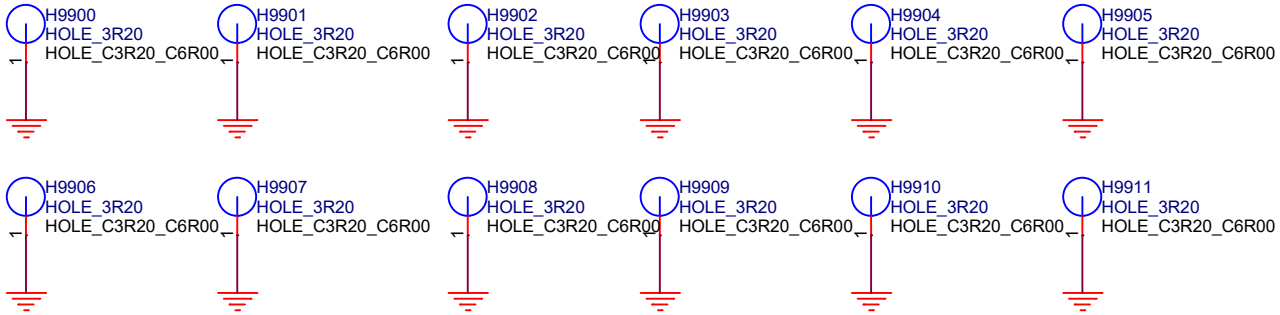
Mark

TOP Mark

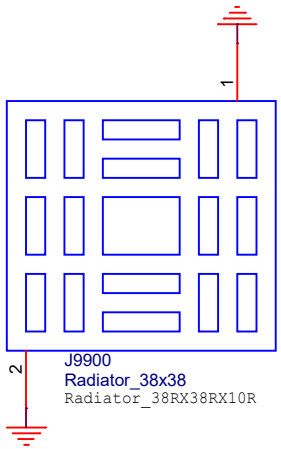
BOTTOM Mark



HOLE



HEATSINK



FAN:8CMX8CM

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	99.Mark/Hole/Heatsink				
Date:	Monday, February 20, 2023			Rev:	V1.4
Designed by:	RZF	Reviewed by:		Sheet:	99 of 99