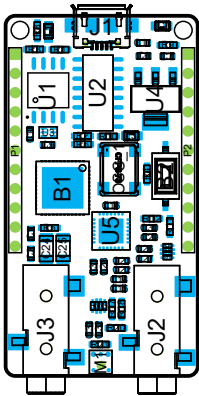


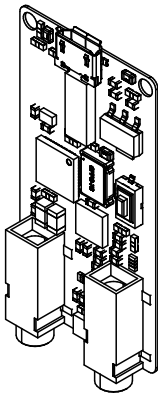
NodeFPGA

Title	Page number
FPGA & Flash Memory	1
USB & MCU	2
Power & IO	3
Audio Codec	4

View from Top side (Scale 1:1)



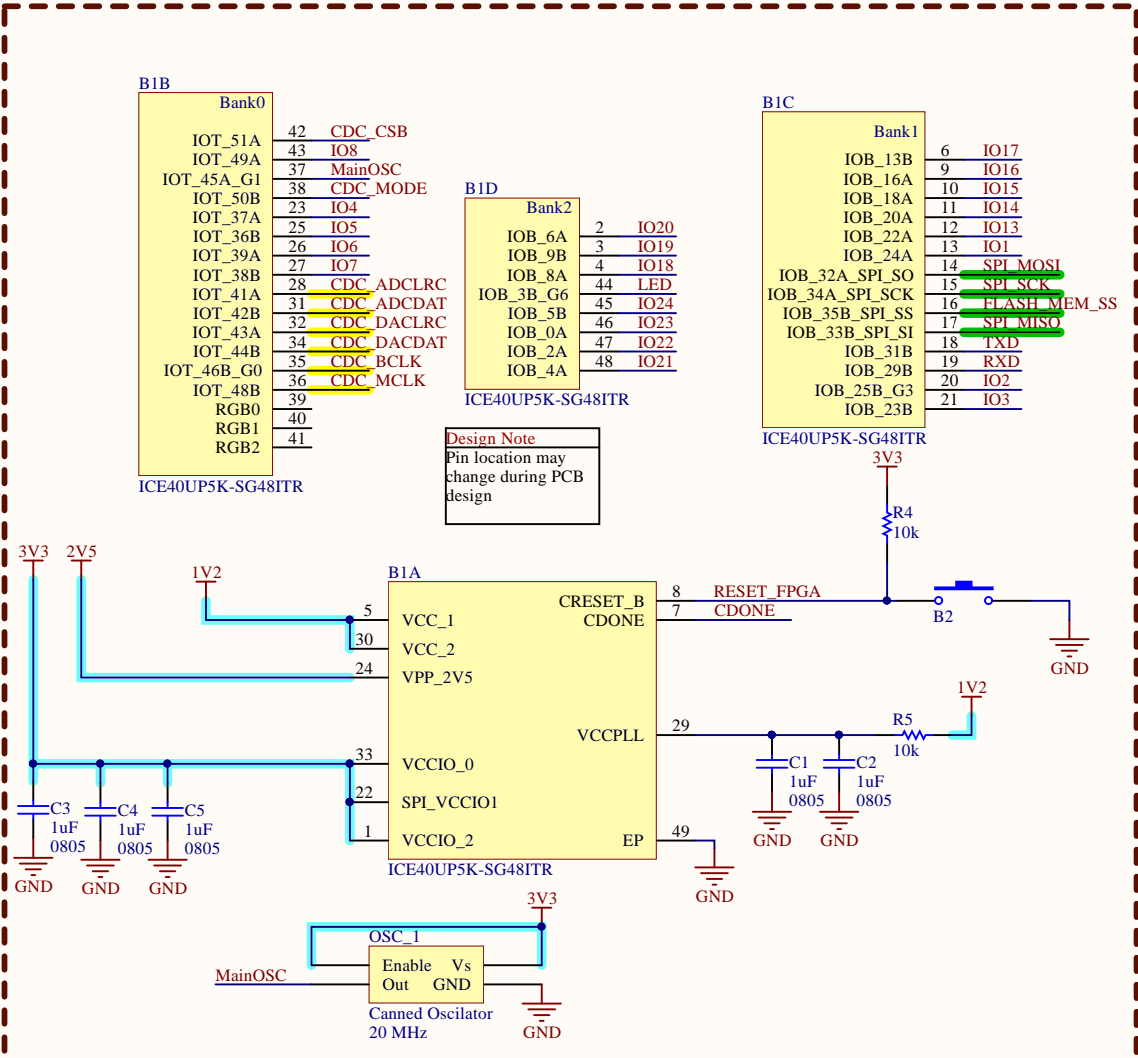
View from Top side (Scale 1:1)



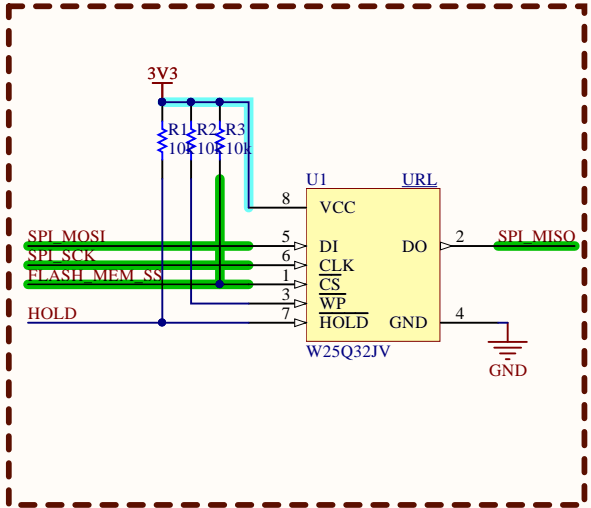
To be updated as
project develops

FPGA & Flash Memory

ICE40UP5K



FLASH MEMORY



Sheet title: **FPGA & Flash Memory**

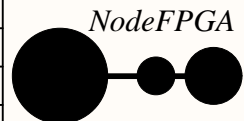
Project title: **NodeFPGA.PrjPcb**

Designer: **Luis Sánchez Velasco**

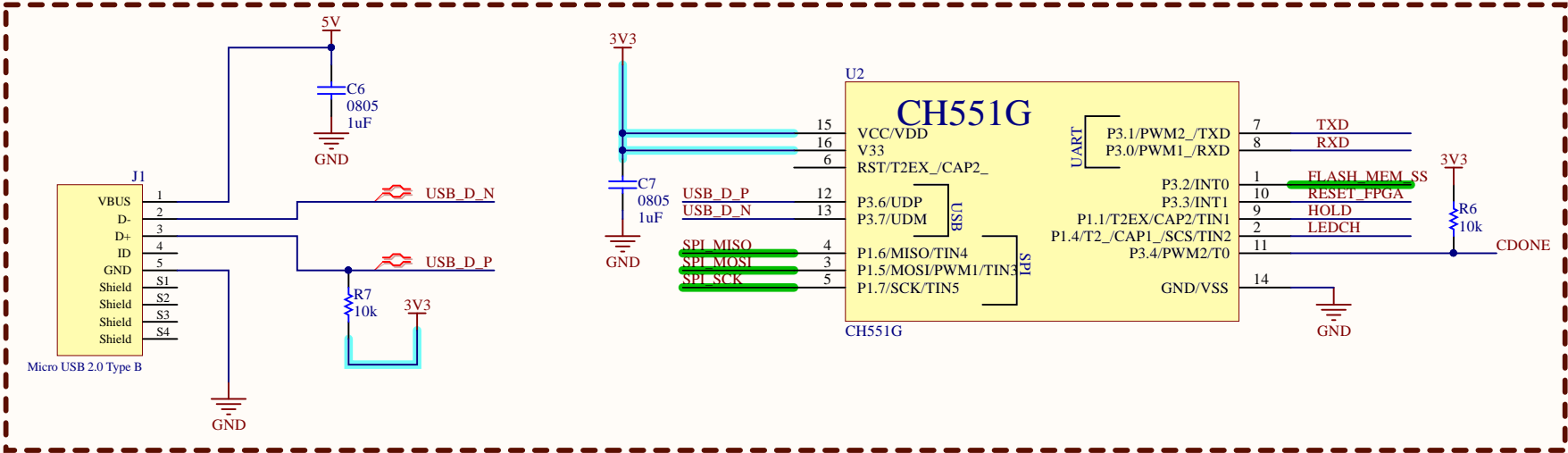
Date: **08/06/2019**

Revision: **0**

Sheet 1 of 4



USB & Microcontroller



Sheet title: **USB & Microcontroller**

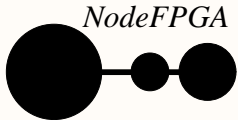
Project title: **NodeFPGA.PrjPcb**

Designer: **Luis Sánchez Velasco**

Date: **08/06/2019**

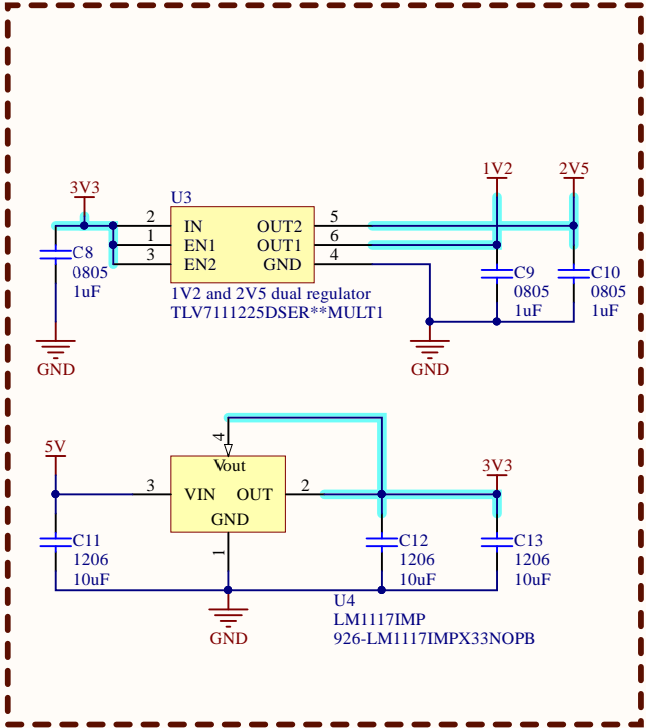
Revision: **0**

Sheet 2 of 4

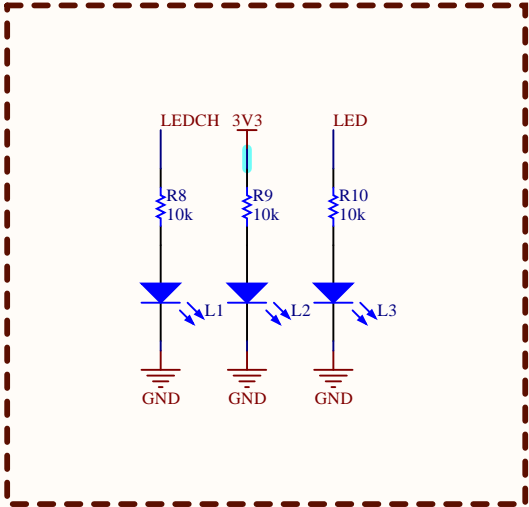


Power & IO

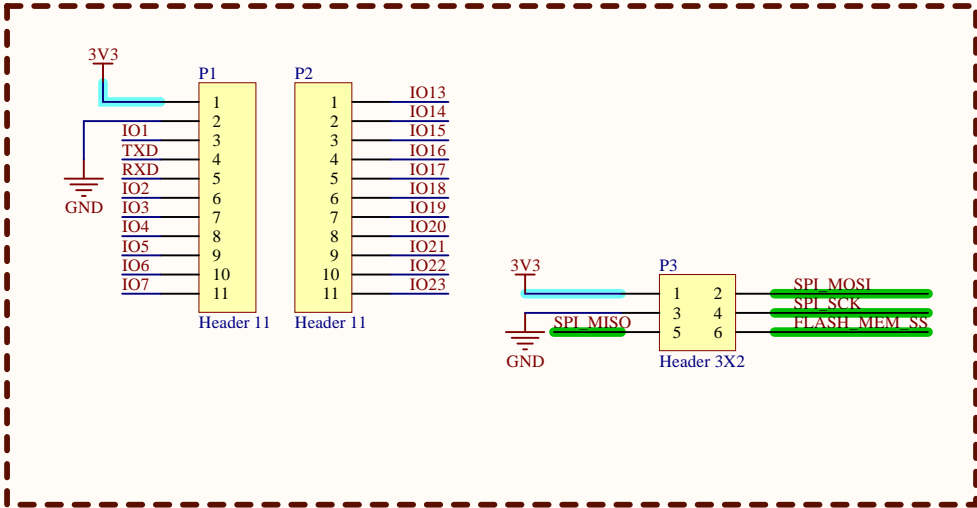
V REGULATORS



STATUS LEDS



PIN HEADERS



Sheet title: **Power & IO**

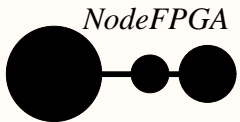
Project title: **NodeFPGA.PrjPcb**

Designer: **Luis Sánchez Velasco**

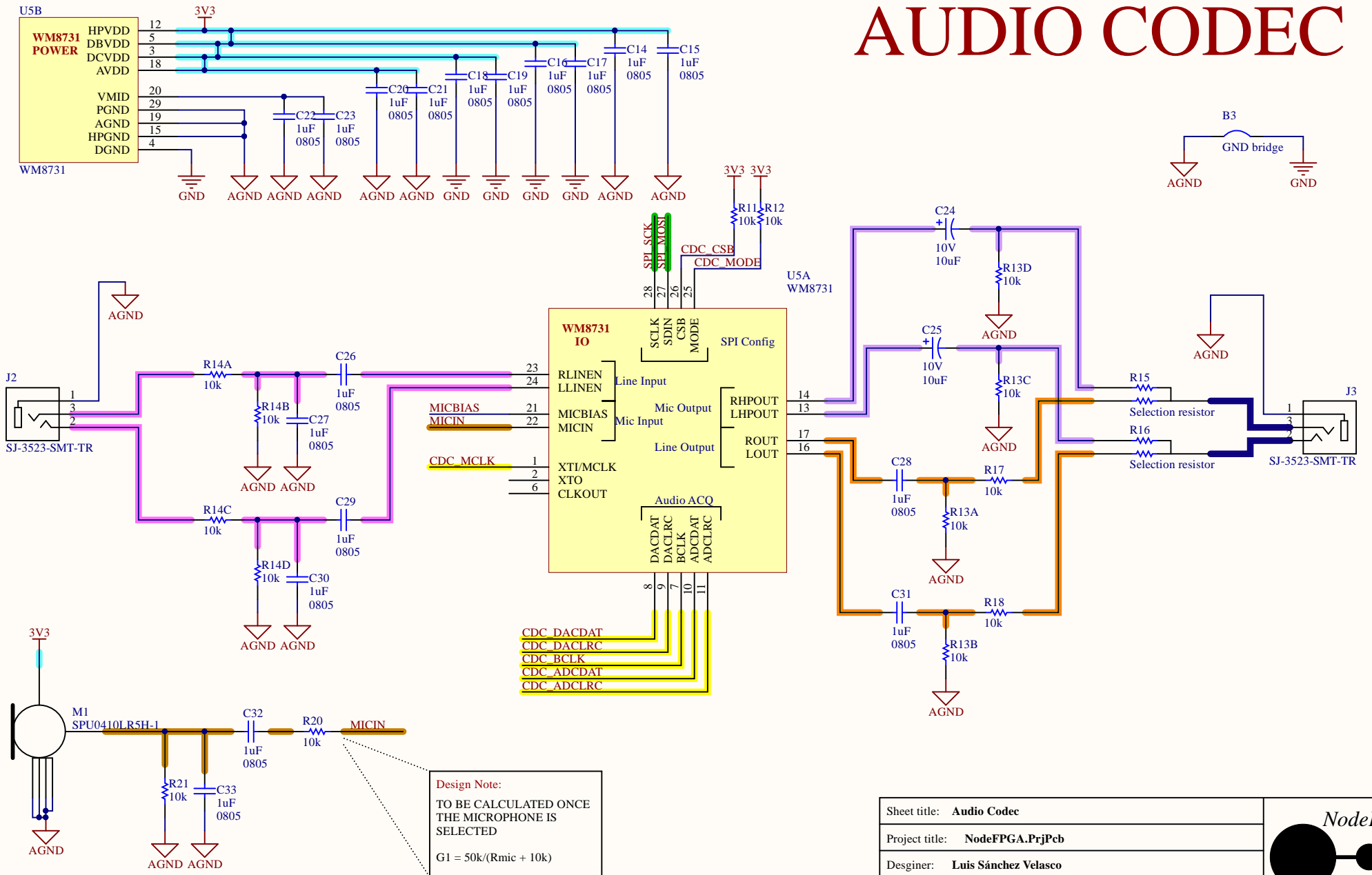
Date: **08/06/2019**


Revision: **0**

Sheet 3 of 4



AUDIO CODEC



Sheet title: Audio Codec		
Project title: NodeFPGA.PrjPcb		
Designer: Luis Sánchez Velasco		
Date: 08/06/2019	Revision: 0	

