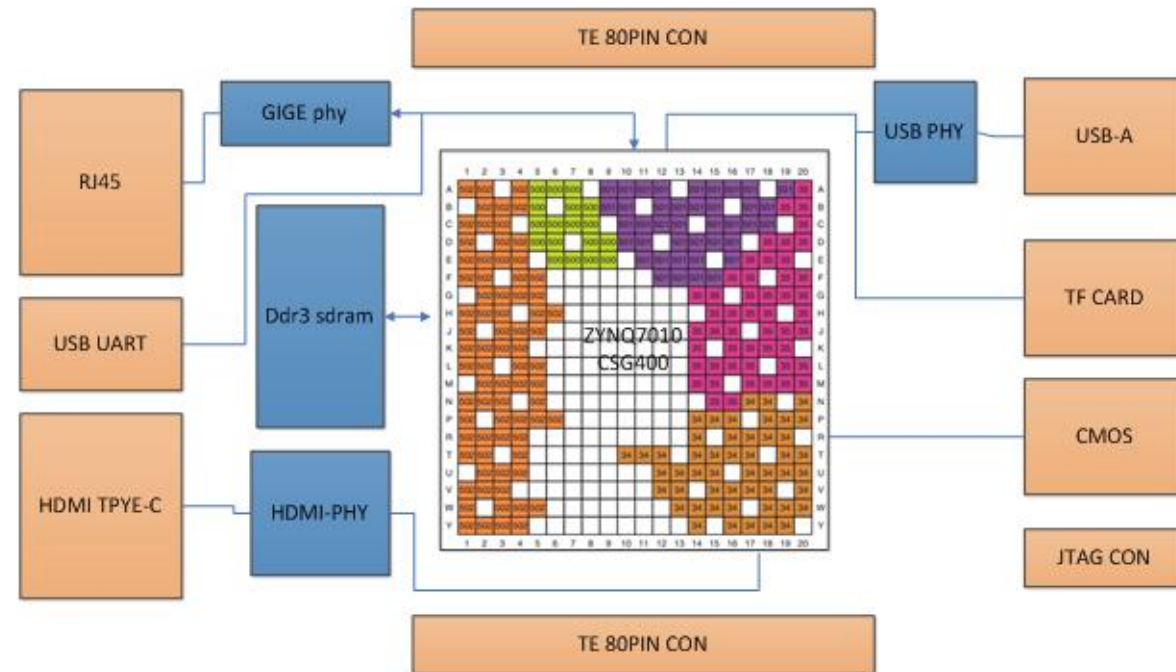
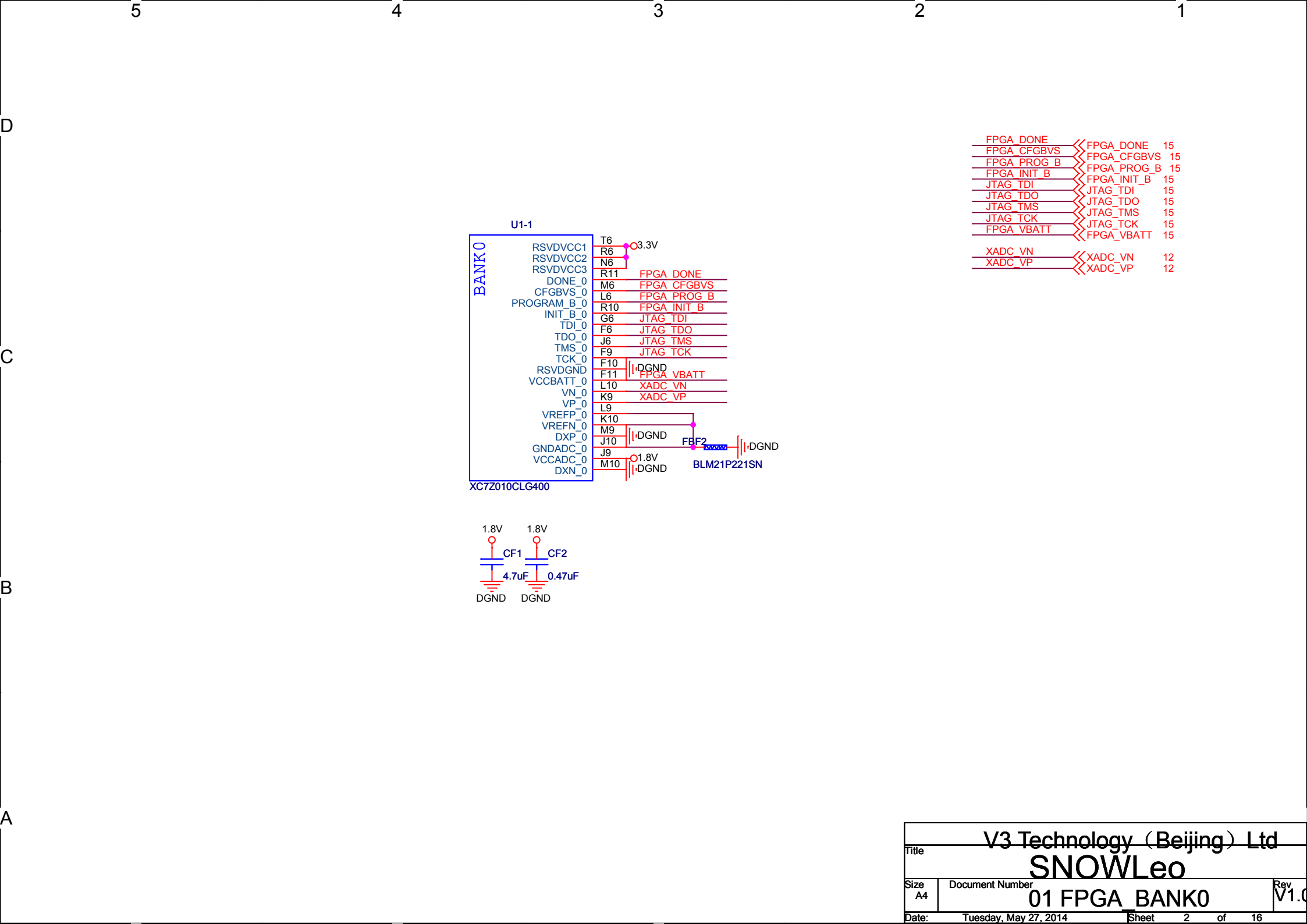


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 PAGE3 02 FPGA_BANK13_NC
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power on sequence
 1 ISL8014A->1.0V
 2 LM26420->1.8V, 1.5V



D

C

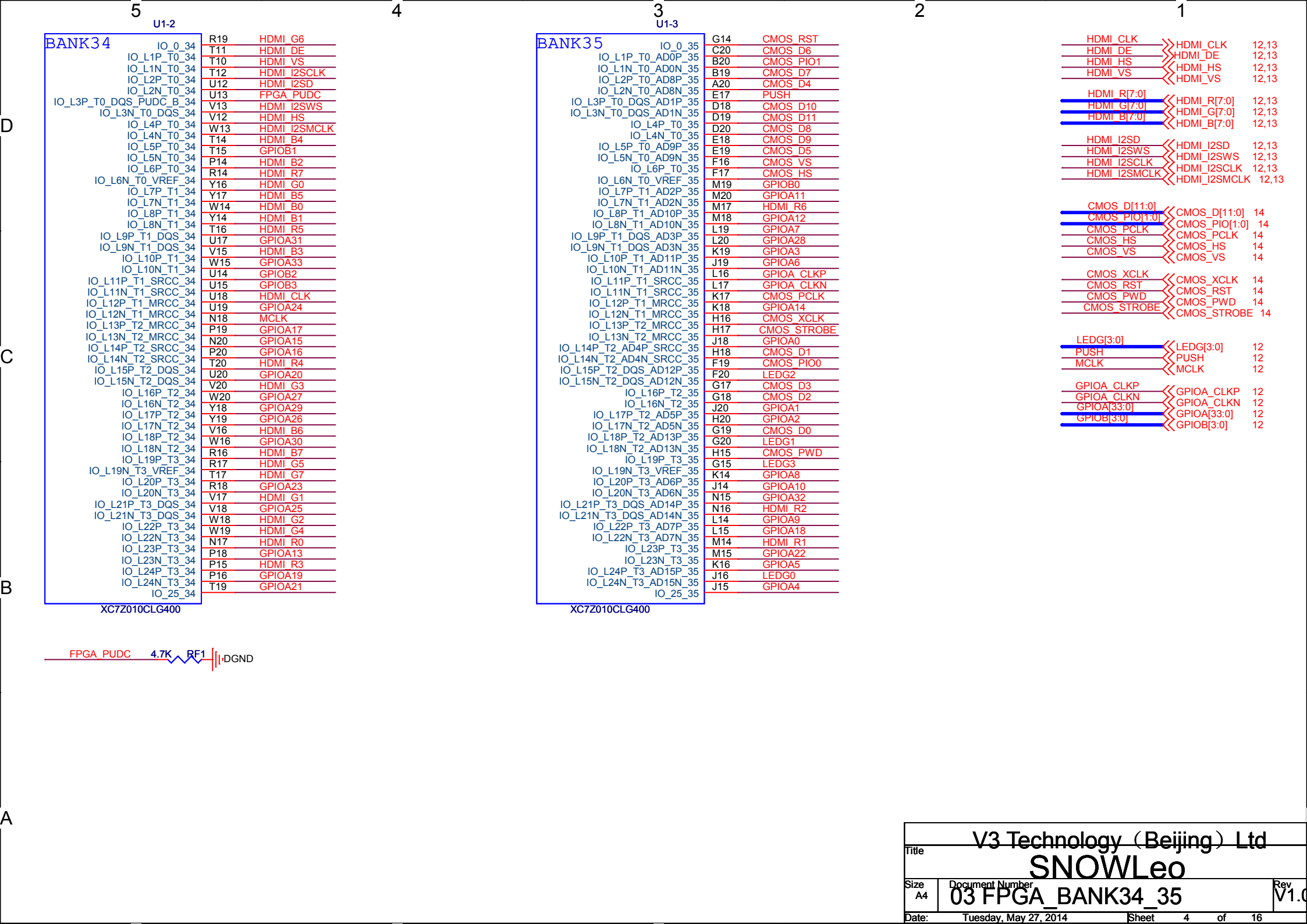
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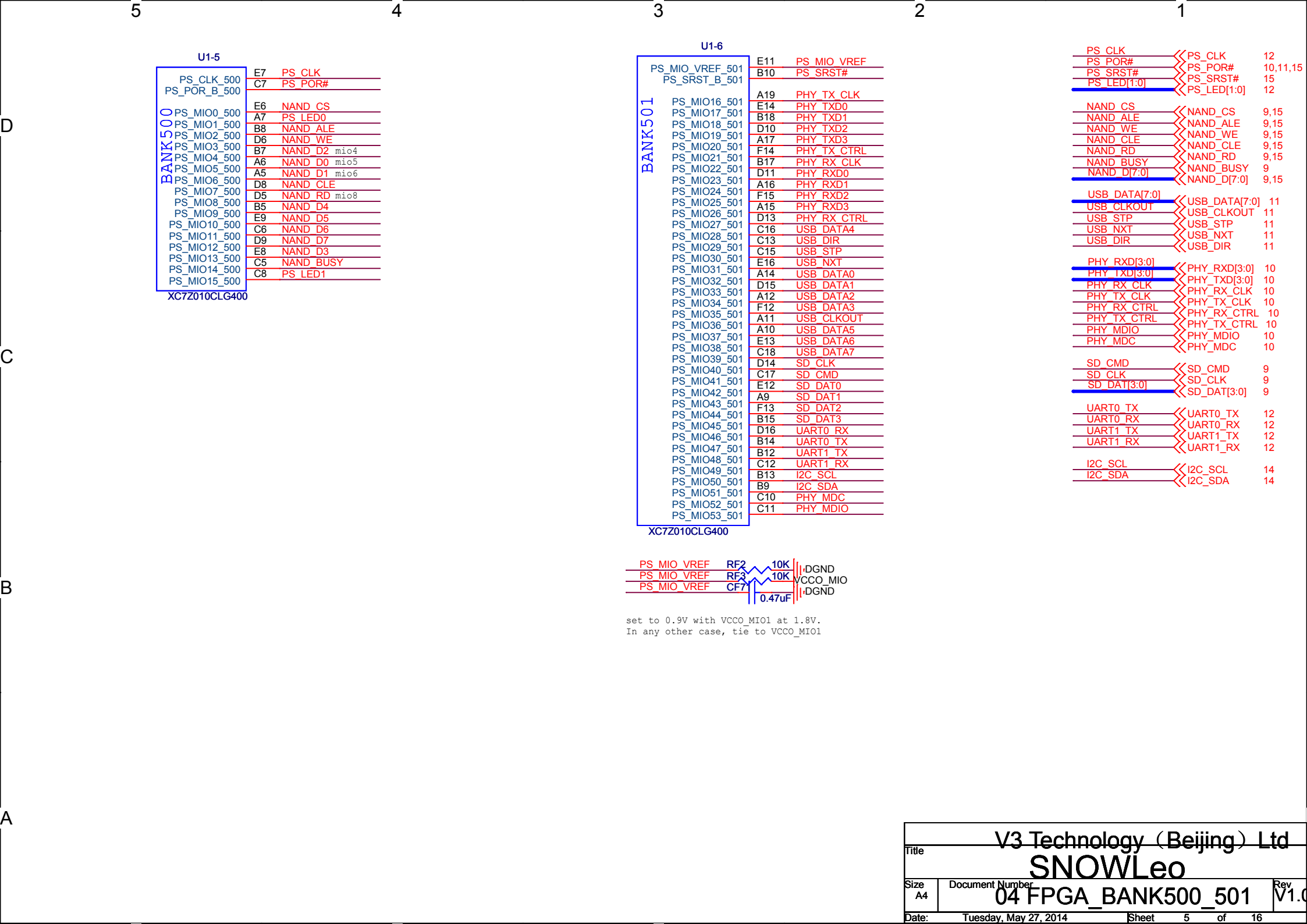
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U1-4

NC FOR 7010 BANK13	IO_L6N_T0_VREF_13	V5
	IO_L11P_T1_SRCC_13	U7
	IO_L11N_T1_SRCC_13	V7
	IO_L12P_T1_MRCC_13	T9
	IO_L12N_T1_MRCC_13	U10
	IO_L13P_T2_MRCC_13	Y7
	IO_L13N_T2_MRCC_13	Y6
	IO_L14P_T2_SRCC_13	Y9
	IO_L14N_T2_SRCC_13	Y8
	IO_L15P_T2_DQS_13	V8
	IO_L15N_T2_DQS_13	W8
	IO_L16P_T2_13	W9
	IO_L16N_T2_13	U9
	IO_L17P_T2_13	U8
	IO_L17N_T2_13	W11
	IO_L18P_T2_13	Y11
	IO_L18N_T2_13	T5
	IO_L19P_T3_13	U5
	IO_L19N_T3_VREF_13	Y12
	IO_L20P_T3_13	Y13
	IO_L20N_T3_13	V11
	IO_L21P_T3_DQS_13	V10
	IO_L21N_T3_DQS_13	V6
	IO_L22P_T3_13	W6
	IO_L22N_T3_13	

XC7Z010CLG400





Title

Size

Date:

V3 Technology (Beijing) Ltd

A4

Tuesday, May 27, 2014

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Document Number

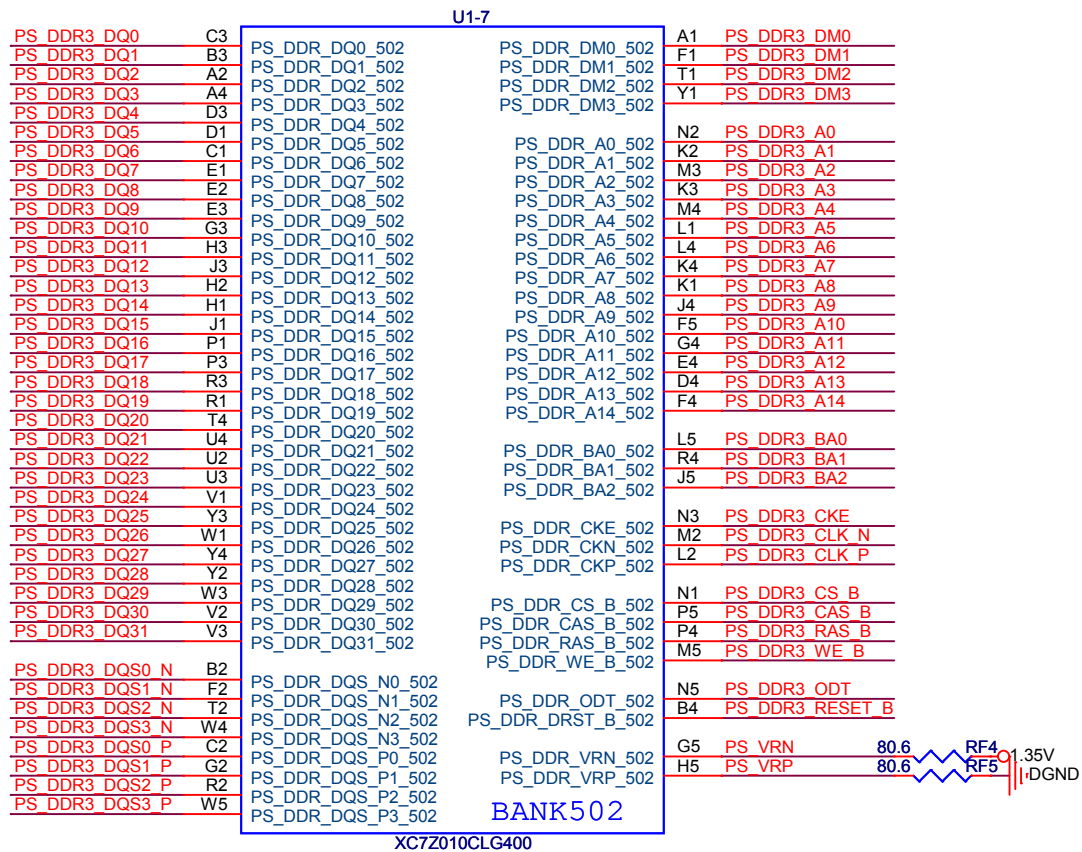
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PS_DDR3_DQ[31:0] << PS_DDR3_DQ[31:0] 8

PS_DDR3_DQS3_N << PS_DDR3_DQS3_N 8

PS_DDR3_DQS3_P << PS_DDR3_DQS3_P 8

PS_DDR3_DQS2_N << PS_DDR3_DQS2_N 8

PS_DDR3_DQS2_P << PS_DDR3_DQS2_P 8

PS_DDR3_DQS1_N << PS_DDR3_DQS1_N 8

PS_DDR3_DQS1_P << PS_DDR3_DQS1_P 8

PS_DDR3_DQS0_N << PS_DDR3_DQS0_N 8

PS_DDR3_DQS0_P << PS_DDR3_DQS0_P 8

PS_DDR3_DM[3:0] << PS_DDR3_DM[3:0] 8

PS_DDR3_RAS_B << PS_DDR3_RAS_B 8

PS_DDR3_CAS_B << PS_DDR3_CAS_B 8

PS_DDR3_WE_B << PS_DDR3_WE_B 8

PS_DDR3_CKE << PS_DDR3_CKE 8

PS_DDR3_CS_B << PS_DDR3_CS_B 8

PS_DDR3_ODT << PS_DDR3_ODT 8

PS_DDR3_CLK_N << PS_DDR3_CLK_N 8

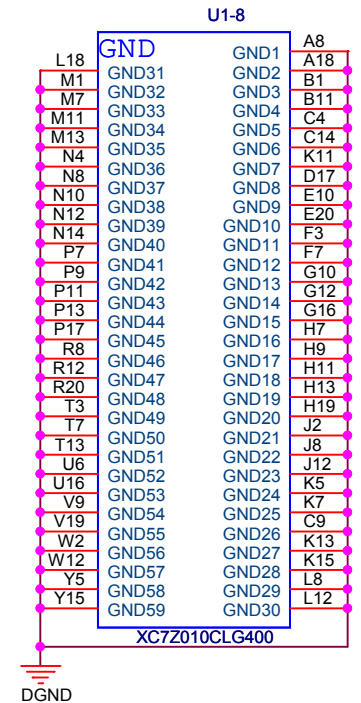
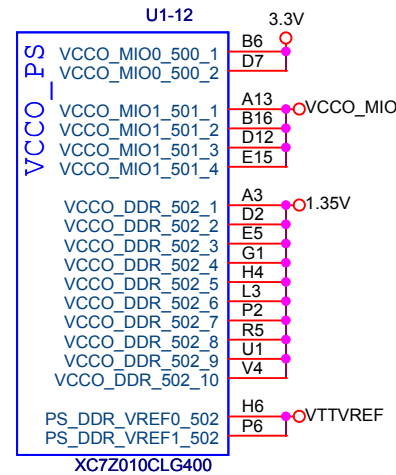
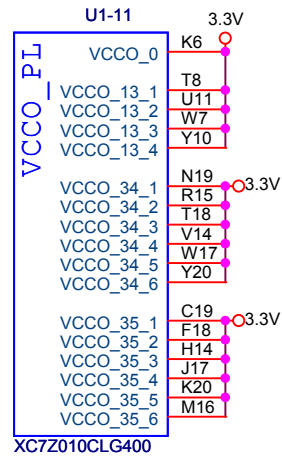
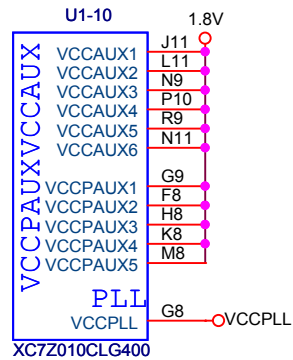
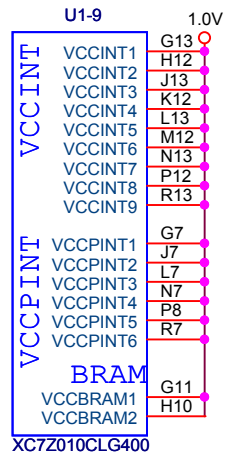
PS_DDR3_CLK_P << PS_DDR3_CLK_P 8

PS_DDR3_RESET_B << PS_DDR3_RESET_B 8

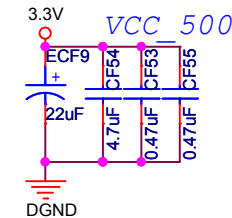
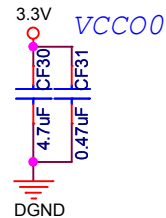
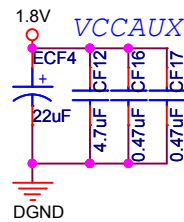
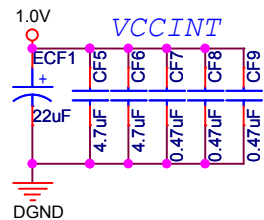
PS_DDR3_BA[2:0] << PS_DDR3_BA[2:0] 8

PS_DDR3_A[14:0] << PS_DDR3_A[14:0] 8

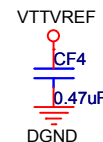
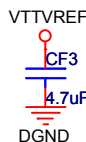
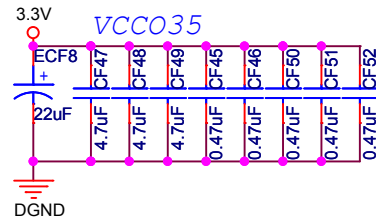
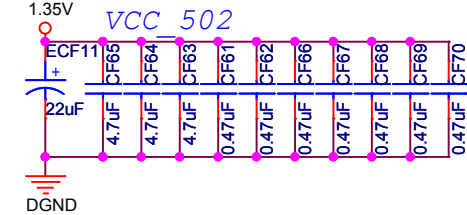
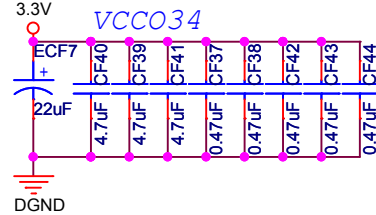
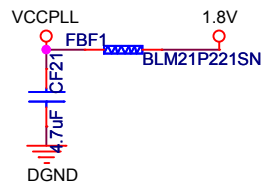
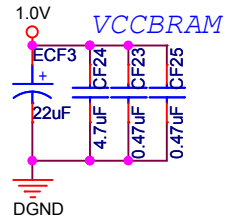
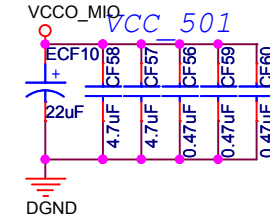
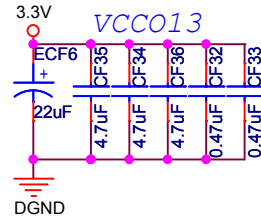
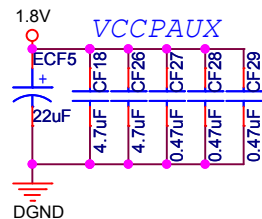
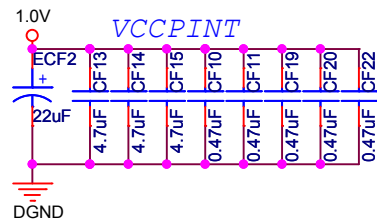
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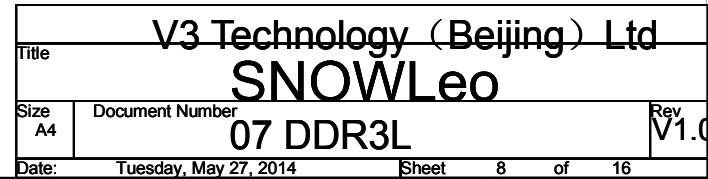
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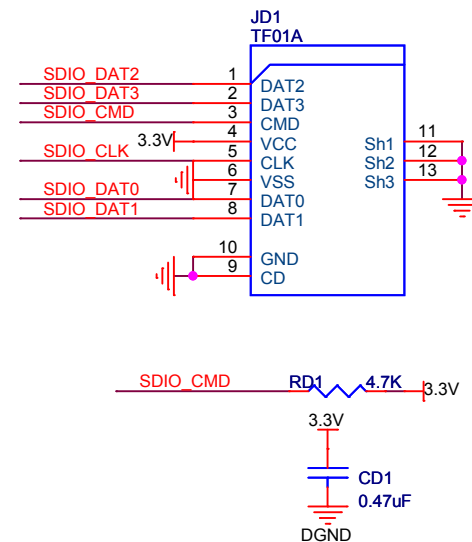
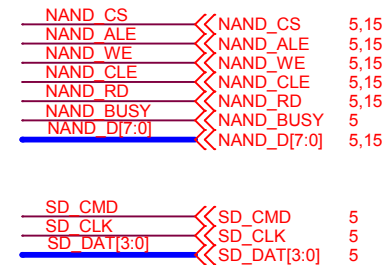
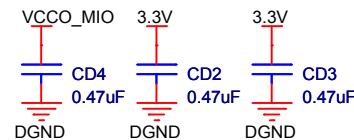
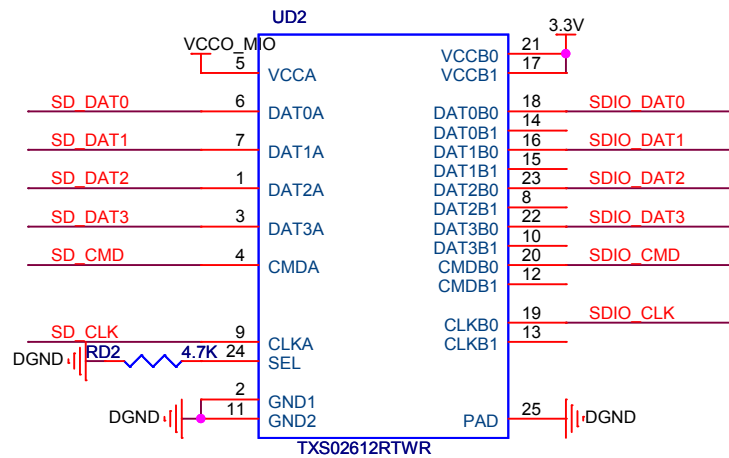
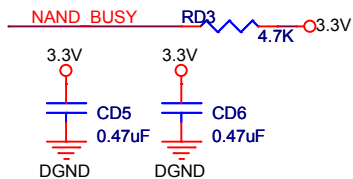
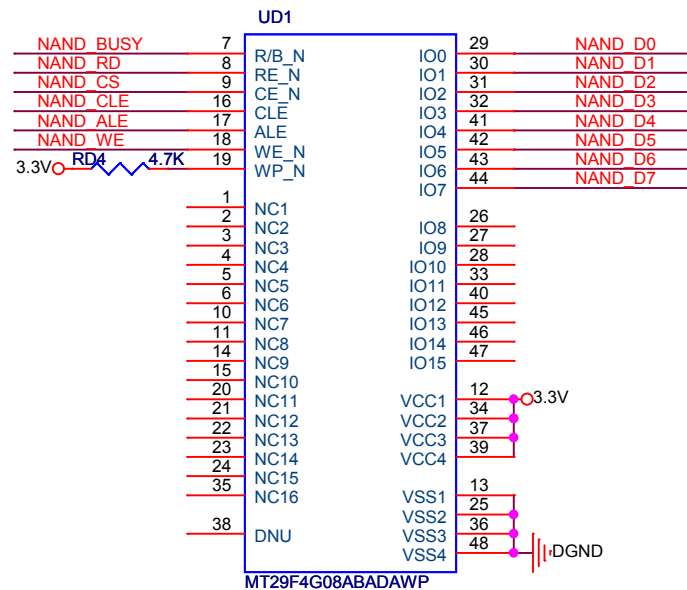


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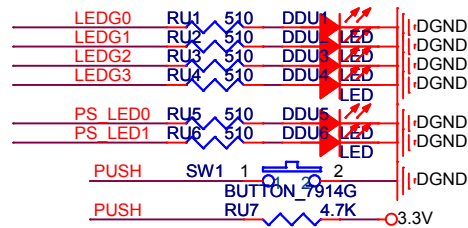


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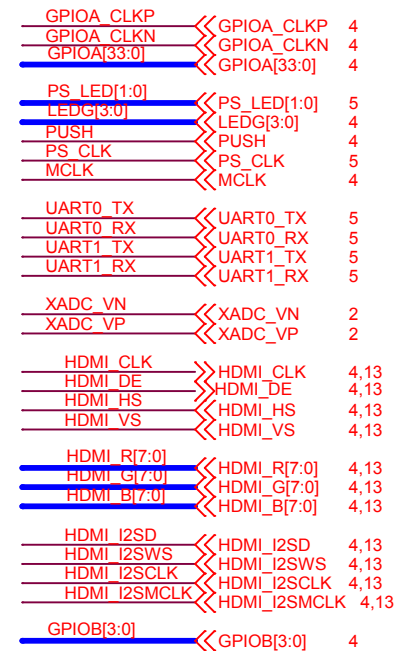
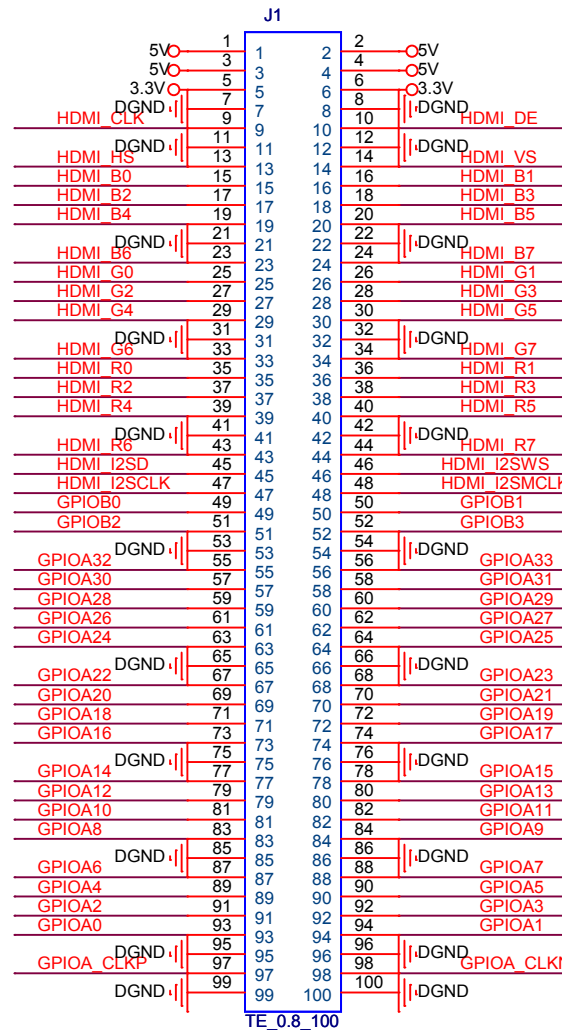
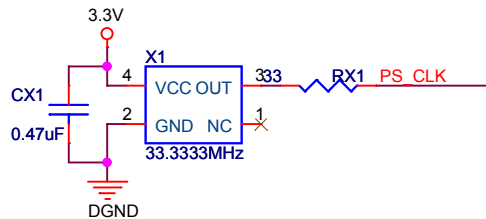
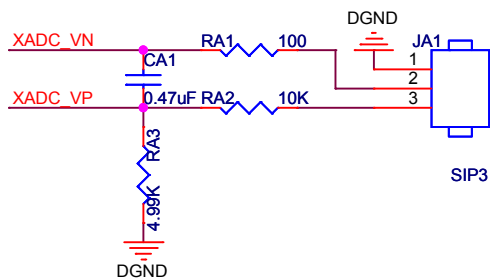
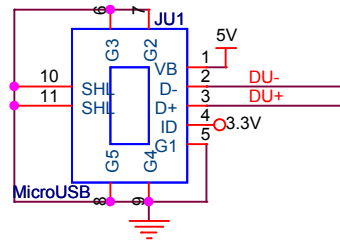
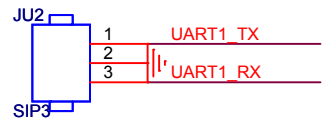
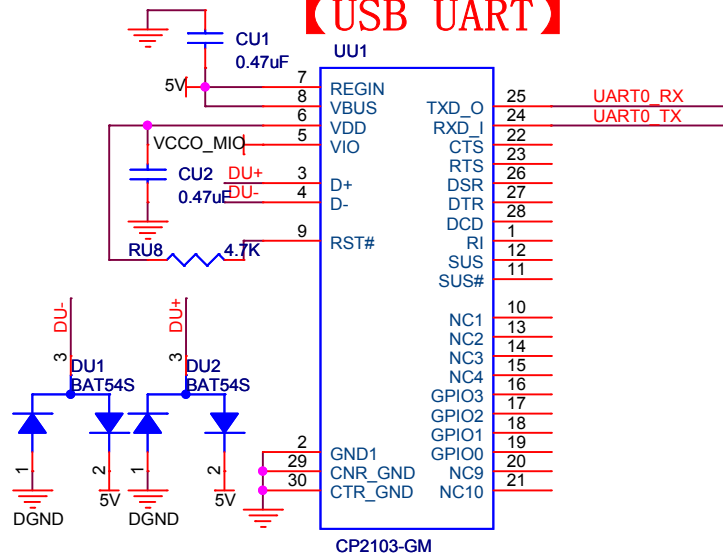
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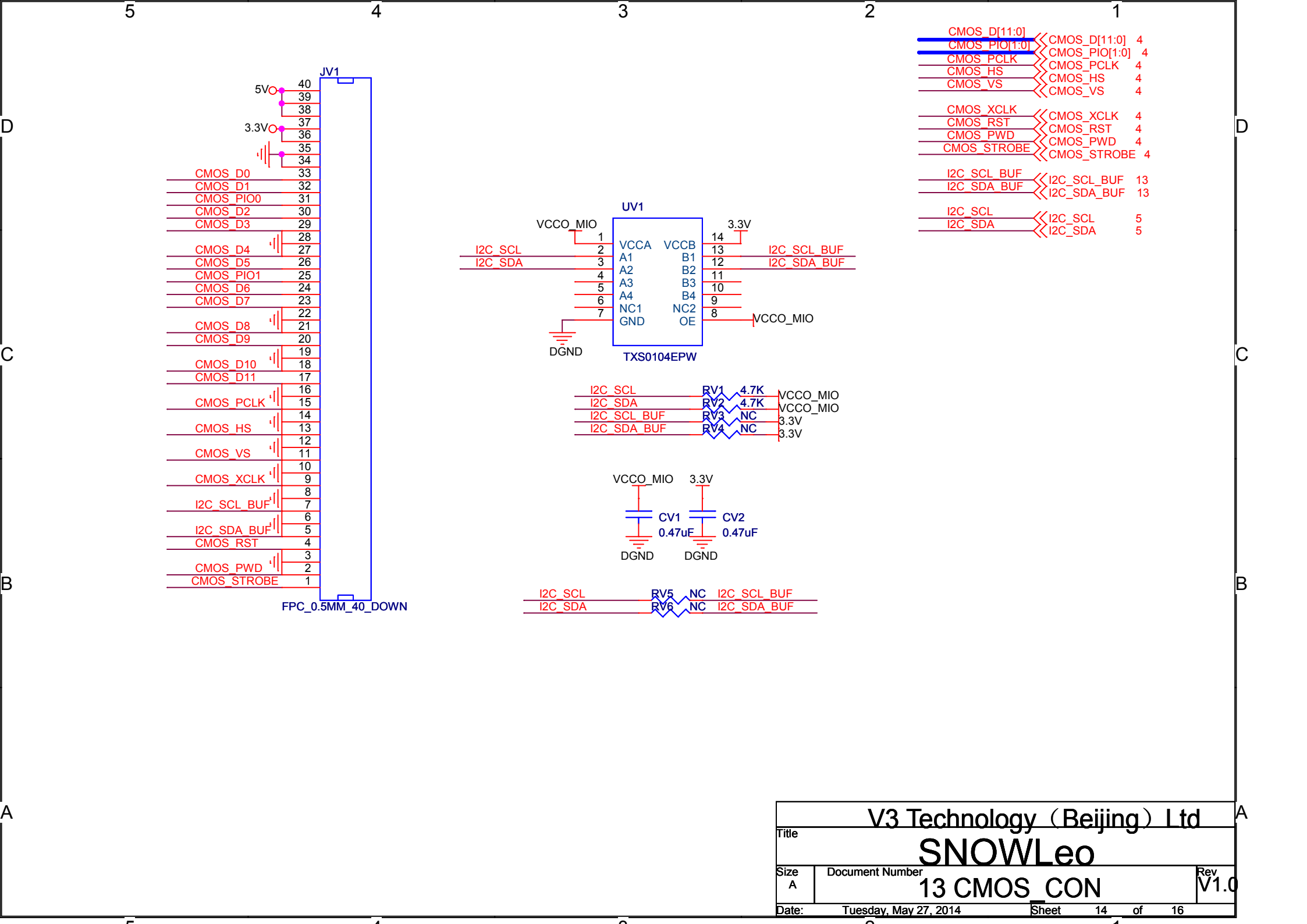
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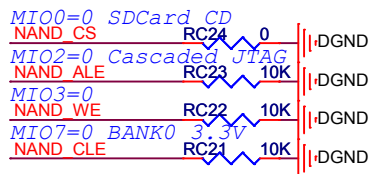
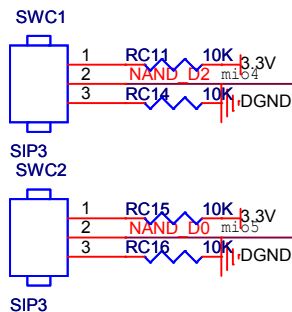
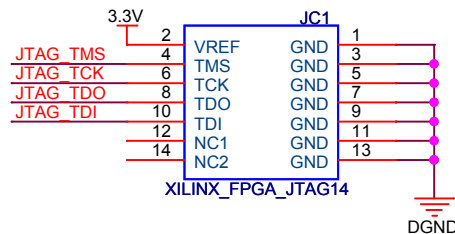
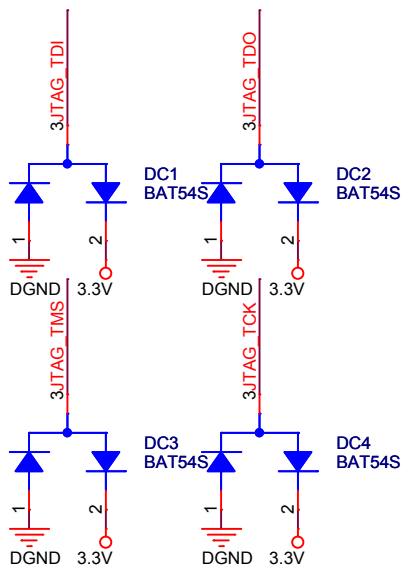
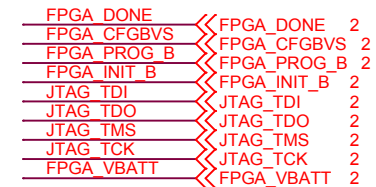
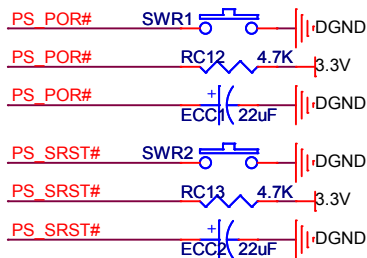
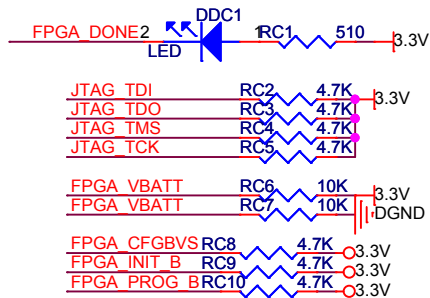
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【USB UART】

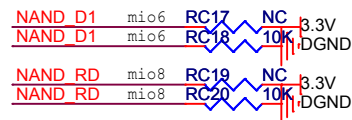






	MIO[6]	MIO[5]	MIO[4]	MIO[3]
JTAG	0	0	0	0
NAND	0	1	1	0
SD	1	1	1	0
PLL Used	0			
PLL Bypassed	1			

MIO Bank1 Voltage
MIO8 0 2.5 V, 3.3 V
MIO8 1 1.8 V



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