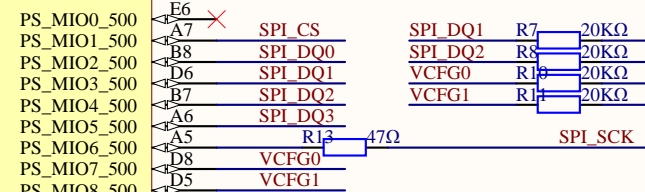
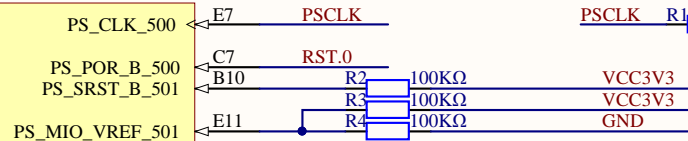
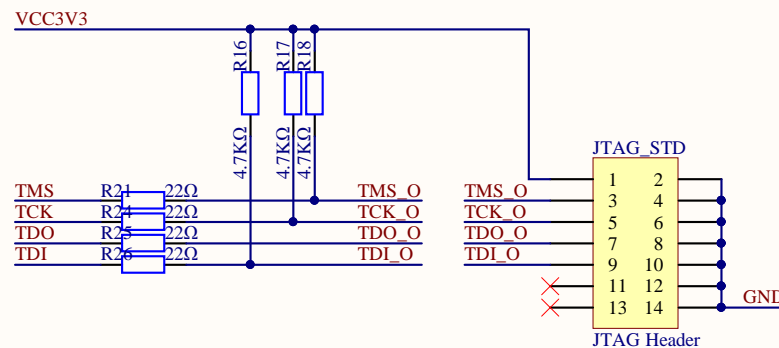
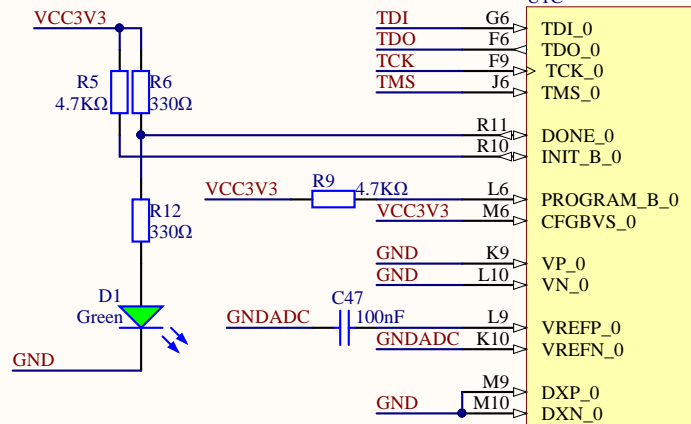
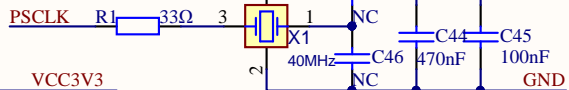
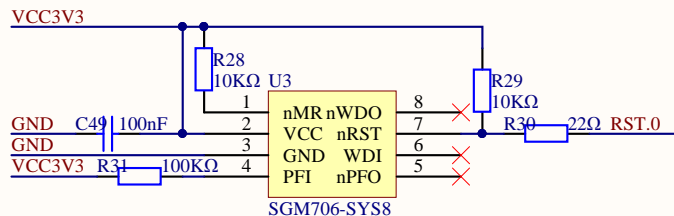
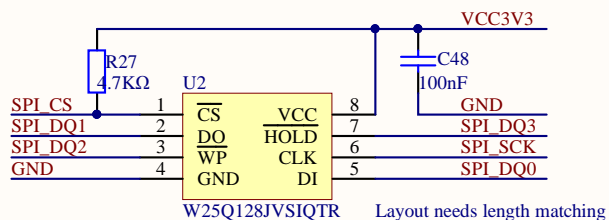
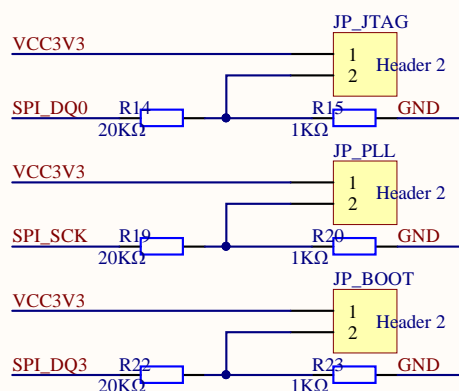


U1D XC7Z010-1CLG400I



MIO1 and MIO0 in 3.3V mode



Title

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Revision

Date: 12/9/2020

Sheet of

File: Z:\swap\CantCantZynq\Sheet2.SchDoc

Drawn By:

U1A XC7Z010-1CLG400I

BANK 34

IO_0_34	R19	SW0
IO_L1P_T0_34	T11	SO_B1C2
IO_L1N_T0_34	T10	SIO2_B1C2
IO_L2P_T0_34	T12	Q1_P
IO_L2N_T0_34	U12	Q1_N
IO_L3P_T0_DQS_PUDC_B_34	U13	Q2_P
IO_L3N_T0_DQS_34	V13	Q2_N
IO_L4P_T0_34	V12	SCK_B1
IO_L4N_T0_34	W13	SIO2_B1C3
IO_L5P_T0_34	T14	SO_B1C1
IO_L5N_T0_34	T15	SI_B1C1
IO_L6P_T0_34	P14	UART_RX
IO_L6N_T0_VREF_34	R14	SIO2_B1C1
IO_L7P_T1_34	Y16	SIO2_B1C4
IO_L7N_T1_34	Y17	SIO3_B1C4
IO_L8P_T1_34	W14	Q3_P
IO_L8N_T1_34	Y14	Q3_N
IO_L9P_T1_DQS_34	T16	SIO3_B1C2
IO_L9N_T1_DQS_34	U17	LED2
IO_L10P_T1_34	V15	SIO3_B1C1
IO_L10N_T1_34	W15	SO_B1C3
IO_L11P_T1_SRCC_34	U14	CE_B1
IO_L11N_T1_SRCC_34	U15	SI_B1C2
IO_L12P_T1_MRCC_34	U18	ETH_CS
IO_L12N_T1_MRCC_34	U19	SYSCLK
IO_L13P_T2_MRCC_34	N18	SD_SCK
IO_L13N_T2_MRCC_34	P19	BTN1
IO_L14P_T2_SRCC_34	N20	HDMI_D2_P
IO_L14N_T2_SRCC_34	P20	HDMI_D2_N
IO_L15P_T2_DQS_34	T20	SW1
IO_L15N_T2_DQS_34	U20	LED0
IO_L16P_T2_34	V20	HDMI_CLK_P
IO_L16N_T2_34	W20	HDMI_CLK_N
IO_L17P_T2_34	Y18	Q4_P
IO_L17N_T2_34	Y19	Q4_N
IO_L18P_T2_34	V16	SI_B1C3
IO_L18N_T2_34	W16	SO_B1C4
IO_L19P_T3_34	R16	ETH_MISO
IO_L19N_T3_VREF_34	R17	SD_DAT3
IO_L20P_T3_34	T17	ETH_RST
IO_L20N_T3_34	R18	SD_DAT2
IO_L21P_T3_DQS_34	V17	LED3
IO_L21N_T3_DQS_34	V18	ETH_MOSI
IO_L22P_T3_34	W18	SIO3_B1C3
IO_L22N_T3_34	W19	SI_B1C4
IO_L23P_T3_34	N17	SD_DAT0
IO_L23N_T3_34	P18	SD_CMD
IO_L24P_T3_34	P15	UART_TX
IO_L24N_T3_34	P16	SIO2_B2C2
IO_25_34	T19	LED1

U1B XC7Z010-1CLG400I

BANK 35

IO_0_35	G14	CE_B2
IO_L1P_T0_AD0P_35	C20	P2_P
IO_L1N_T0_AD0N_35	B20	P2_N
IO_L2P_T0_AD8P_35	B19	P5_P
IO_L2N_T0_AD8N_35	A20	P5_N
IO_L3P_T0_DQS_AD1P_35	E17	SCK_B2
IO_L3N_T0_DQS_AD1N_35	D18	SIO3_B2C2
IO_L4P_T0_35	D19	P1_P
IO_L4N_T0_35	D20	P1_N
IO_L5P_T0_AD9P_35	E18	SI_B2C4
IO_L5N_T0_AD9N_35	E19	IO6
IO_L6P_T0_35	F16	SIO3_B2C1
IO_L6N_T0_VREF_35	F17	SO_B2C4
IO_L7P_T1_AD2P_35	M19	SD_DAT1
IO_L7N_T1_AD2N_35	M20	SD_NCD
IO_L8P_T1_AD10P_35	M17	HDMI_D0_P
IO_L8N_T1_AD10N_35	M18	HDMI_D0_N
IO_L9P_T1_DQS_AD3P_35	L19	ETH_INT
IO_L9N_T1_DQS_AD3N_35	L20	ETH_SCLK
IO_L10P_T1_AD11P_35	K19	IO1
IO_L10N_T1_AD11N_35	J19	USBRXD
IO_L11P_T1_SRCC_35	L16	HDMI_D1_P
IO_L11N_T1_SRCC_35	L17	HDMI_D1_N
IO_L12P_T1_MRCC_35	K17	SYSCLK2
IO_L12N_T1_MRCC_35	K18	IO3
IO_L13P_T2_MRCC_35	H16	SIO2_B2C4
IO_L13N_T2_MRCC_35	H17	IO4
IO_L14P_T2_AD4P_SRCC_35	J18	USBTXD
IO_L14N_T2_AD4N_SRCC_35	H18	USBnINT
IO_L15P_T2_DQS_AD12P_35	F19	P4_P
IO_L15N_T2_DQS_AD12N_35	F20	P4_N
IO_L16P_T2_35	G17	SI_B2C2
IO_L16N_T2_35	G18	IO5
IO_L17P_T2_AD5P_35	J20	USBD2_P
IO_L17N_T2_AD5N_35	H20	USBD2_N
IO_L18P_T2_AD13P_35	G19	P3_P
IO_L18N_T2_AD13N_35	G20	P3_N
IO_L19P_T3_35	H15	SIO3_B2C3
IO_L19N_T3_VREF_35	G15	SI_B2C3
IO_L20P_T3_AD6P_35	K14	SO_B2C3
IO_L20N_T3_AD6N_35	J14	SIO2_B2C3
IO_L21P_T3_DQS_AD14P_35	N15	SO_B2C1
IO_L21N_T3_DQS_AD14N_35	N16	
IO_L22P_T3_AD7P_35	L14	SO_B2C2
IO_L22N_T3_AD7N_35	L15	BTN0
IO_L23P_T3_35	M14	SIO2_B2C1
IO_L23N_T3_35	M15	
IO_L24P_T3_AD15P_35	K16	IO2
IO_L24N_T3_AD15N_35	J16	SIO3_B2C4
IO_25_35	J15	SI_B2C1

U1E XC7Z010-1CLG400I

C3	PS_DDR_DQ0_502	PS_DDR_CKP_502	L2
B3	PS_DDR_DQ1_502	PS_DDR_CKN_502	M2
A2	PS_DDR_DQ2_502	PS_DDR_CKE_502	N3
A4	PS_DDR_DQ3_502		
D3	PS_DDR_DQ4_502	PS_DDR_CS_B_502	N1
D1	PS_DDR_DQ5_502	PS_DDR_CS_B_502	P4
C1	PS_DDR_DQ6_502	PS_DDR_CAS_B_502	P5
E1	PS_DDR_DQ7_502	PS_DDR_WE_B_502	M5
E2	PS_DDR_DQ8_502		
E3	PS_DDR_DQ9_502	PS_DDR_BA0_502	L5
G3	PS_DDR_DQ10_502	PS_DDR_BA1_502	R4
H3	PS_DDR_DQ11_502	PS_DDR_BA2_502	J5
J3	PS_DDR_DQ12_502		
H2	PS_DDR_DQ13_502	PS_DDR_A0_502	N2
H1	PS_DDR_DQ14_502	PS_DDR_A1_502	K2
J1	PS_DDR_DQ15_502	PS_DDR_A2_502	M3
P1	PS_DDR_DQ16_502	PS_DDR_A3_502	K3
P3	PS_DDR_DQ17_502	PS_DDR_A4_502	M4
R1	PS_DDR_DQ18_502	PS_DDR_A5_502	L1
T4	PS_DDR_DQ19_502	PS_DDR_A6_502	L4
U4	PS_DDR_DQ20_502	PS_DDR_A7_502	K4
U2	PS_DDR_DQ21_502	PS_DDR_A8_502	K1
U3	PS_DDR_DQ22_502	PS_DDR_A9_502	J4
V1	PS_DDR_DQ23_502	PS_DDR_A10_502	F5
Y3	PS_DDR_DQ24_502	PS_DDR_A11_502	G4
W1	PS_DDR_DQ25_502	PS_DDR_A12_502	E4
Y2	PS_DDR_DQ26_502	PS_DDR_A13_502	D4
Y4	PS_DDR_DQ27_502	PS_DDR_A14_502	F4
W3	PS_DDR_DQ28_502		
V2	PS_DDR_DQ29_502	PS_DDR_ODT_502	N5
V3	PS_DDR_DQ30_502		
	PS_DDR_DQ31_502	PS_DDR_DRST_B_502	B4
A1	PS_DDR_DM0_502		
F1	PS_DDR_DM1_502		
T1	PS_DDR_DM2_502		
Y1	PS_DDR_DM3_502		
C2	PS_DDR_DQS_P0_502		
B2	PS_DDR_DQS_N0_502		
G2	PS_DDR_DQS_P1_502		
F2	PS_DDR_DQS_N1_502	PS_DDR_VRN_502	G5
R2	PS_DDR_DQS_P2_502	PS_DDR_VRP_502	H5
T2	PS_DDR_DQS_N2_502		
W5	PS_DDR_DQS_P3_502	PS_DDR_VREF0_502	H6
W4	PS_DDR_DQS_N3_502	PS_DDR_VREF1_502	P6

27 left, can get 8 or 16 more on PSRAM
another 8 from LED SW BTN

lower: 8led + 8normal (1 pmod compatible)

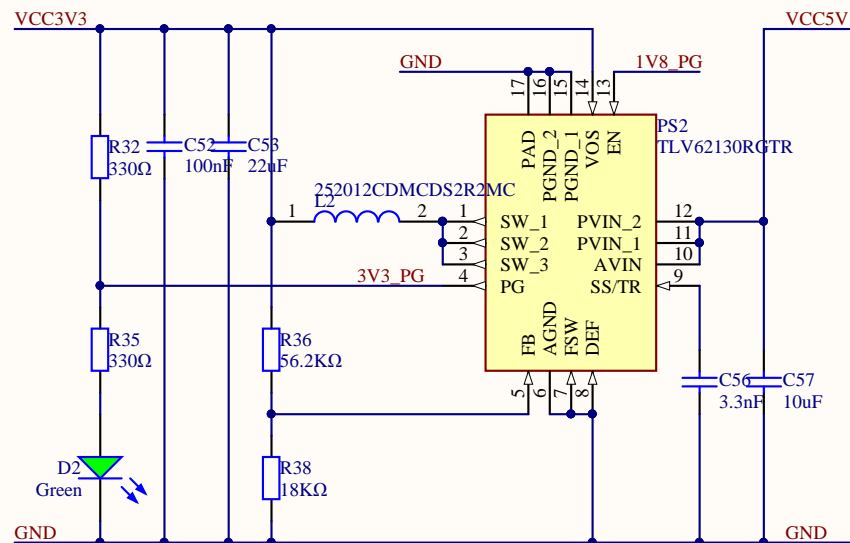
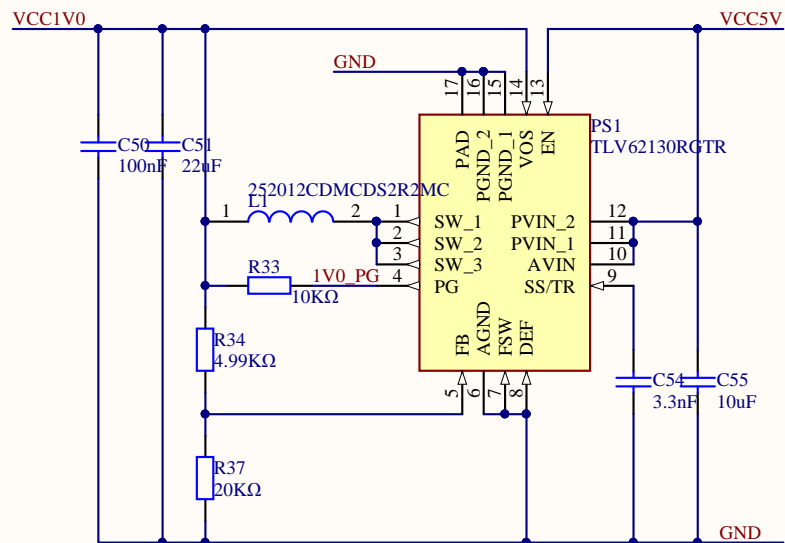
upper: 8RAM + 16normal(3 pmod compatible)

PYNQ hat: 45 IO total, 12 lower, 33 upper
RPI header: 28x IO, 1x 3V3, 2x 5V

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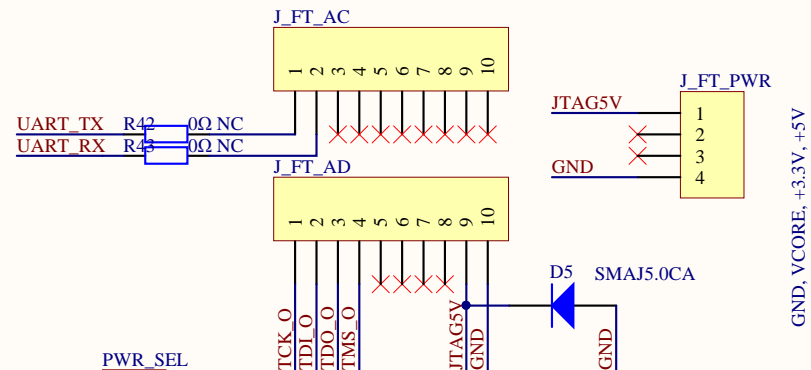
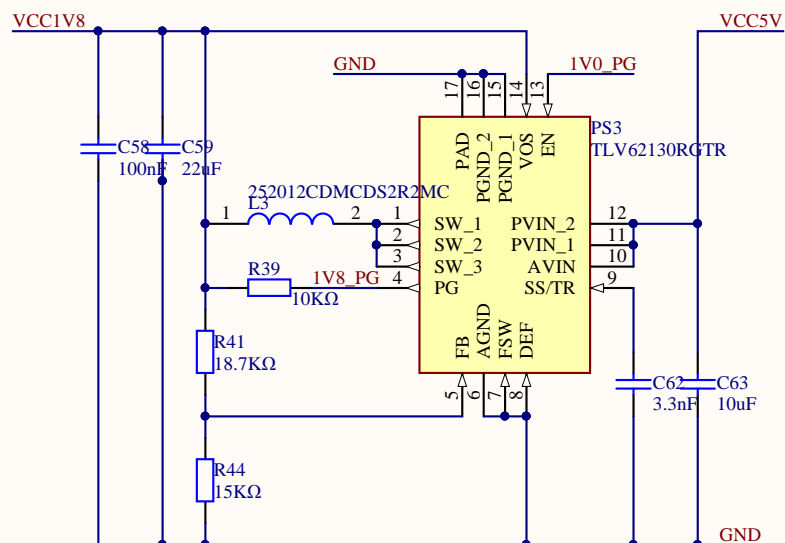
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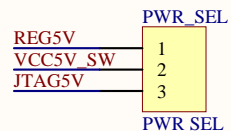


B

B



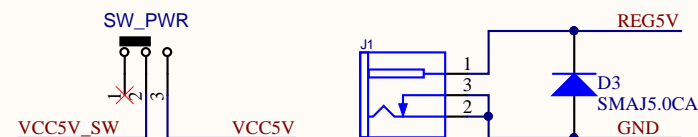
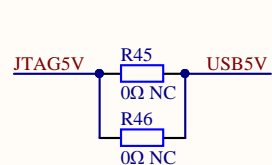
C



AC9 8 7 6 5 4 3 2 1 0

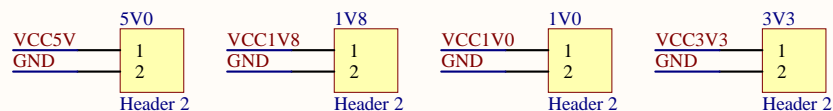
Top-down view of CJMCU-FT232HL

AD0 1 2 3 4 5 6 7, +5V, GND

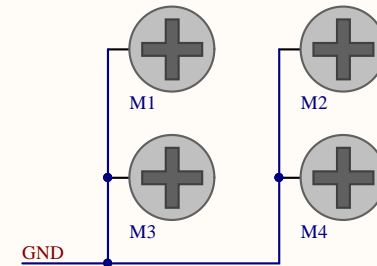
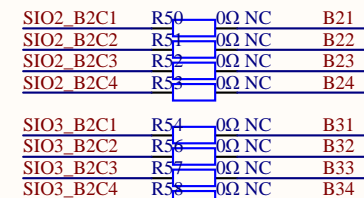
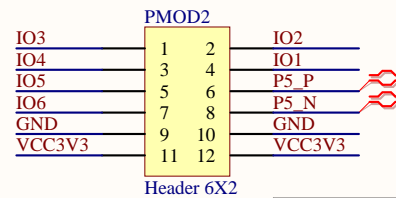
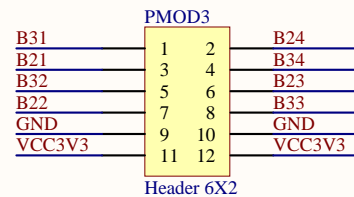
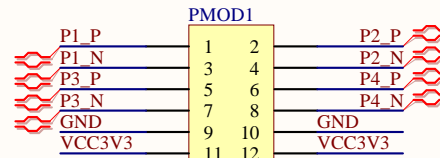
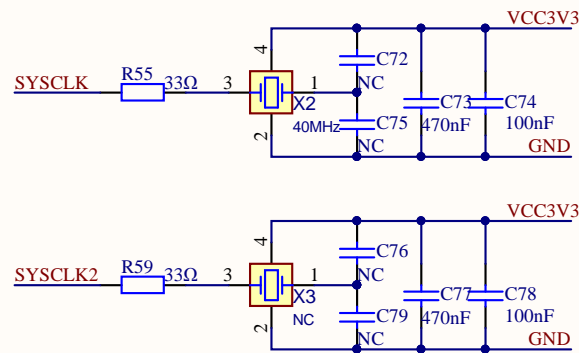
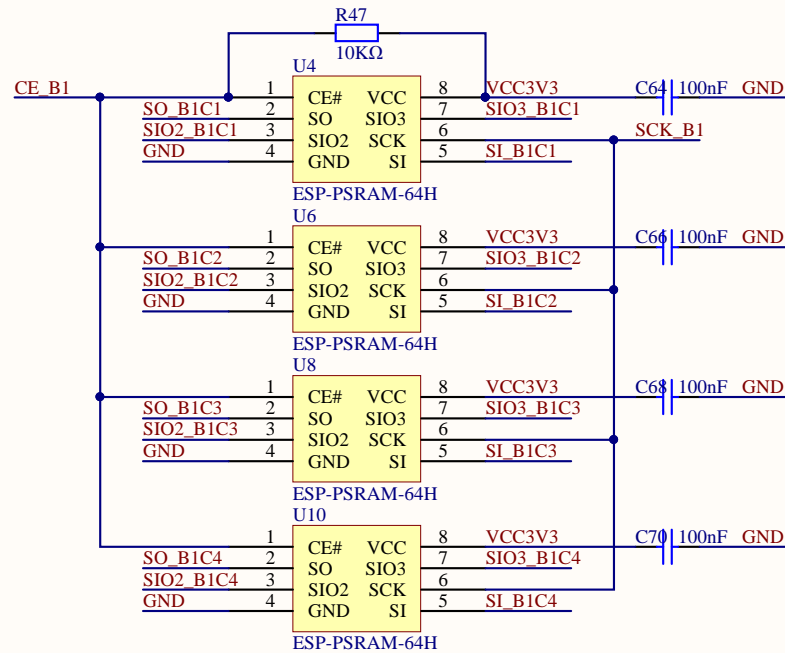


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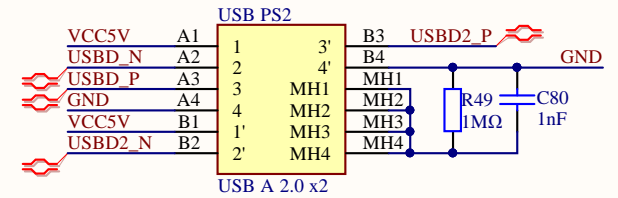
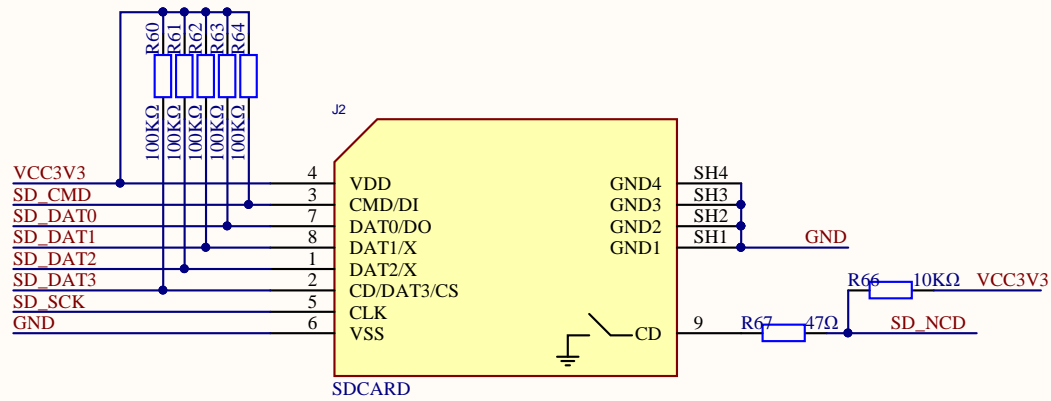
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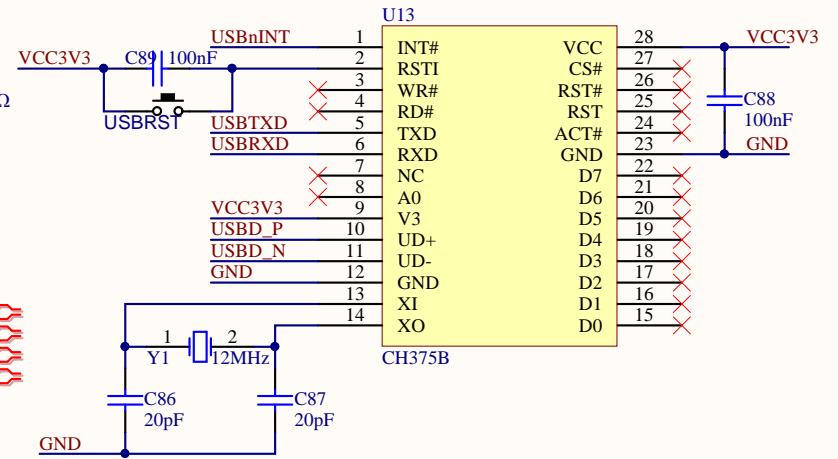
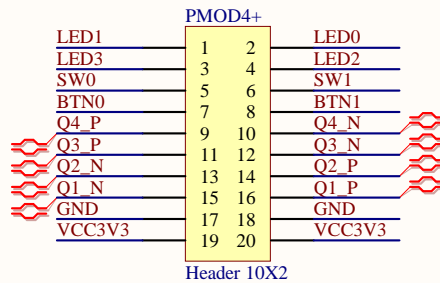
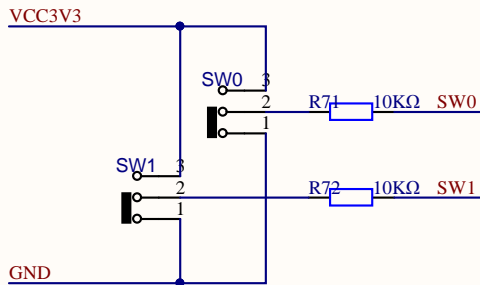
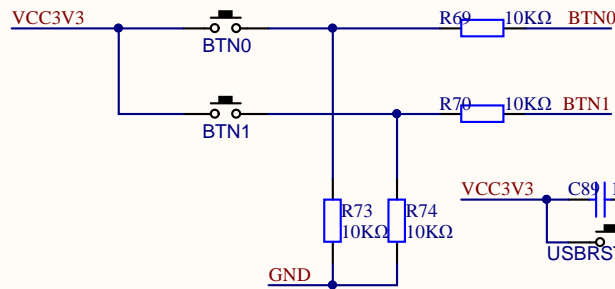
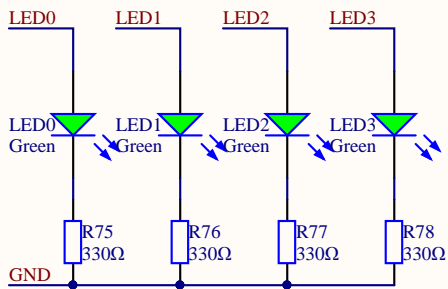
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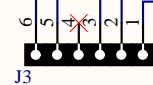
This USB is not serious
The only recommended usage is PS/2 keyboard



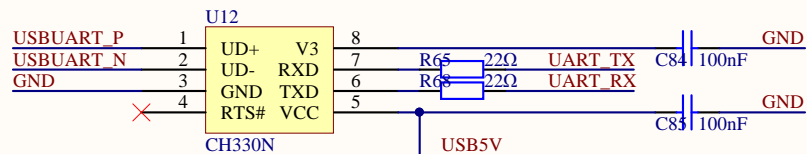
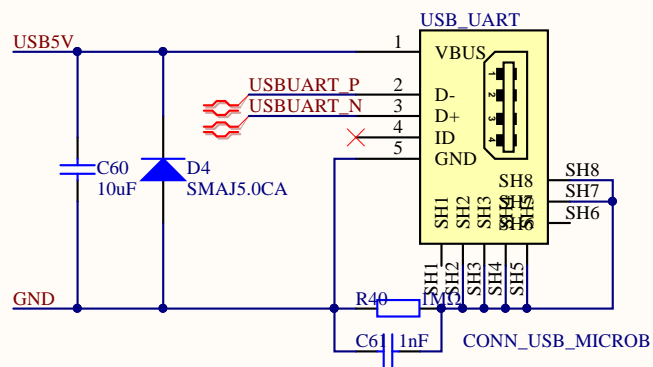
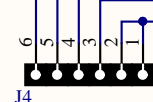
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W5500-Lite Module
ETH_MISO
ETH_RST

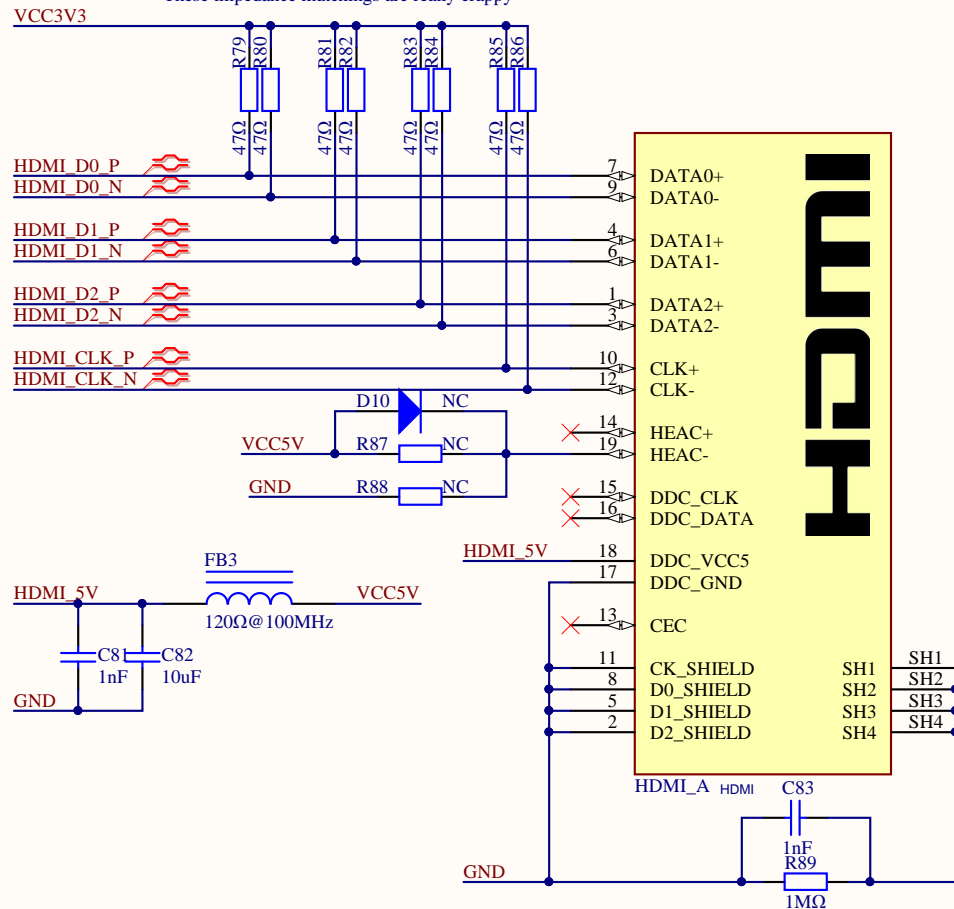
VCC3V3
GND



ETH_INT
ETH_CS
ETH_SCLK
ETH_MOSI
GND



These impedance matchings are really crappy



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