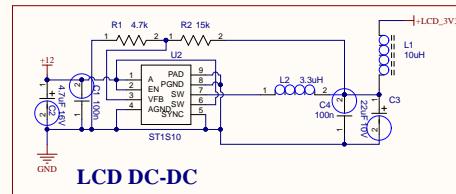


7Inch version

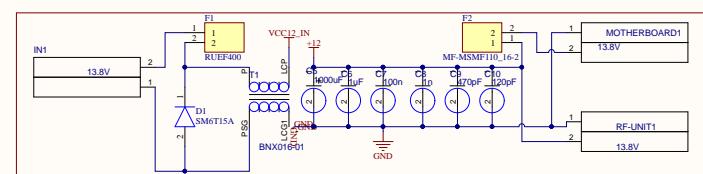
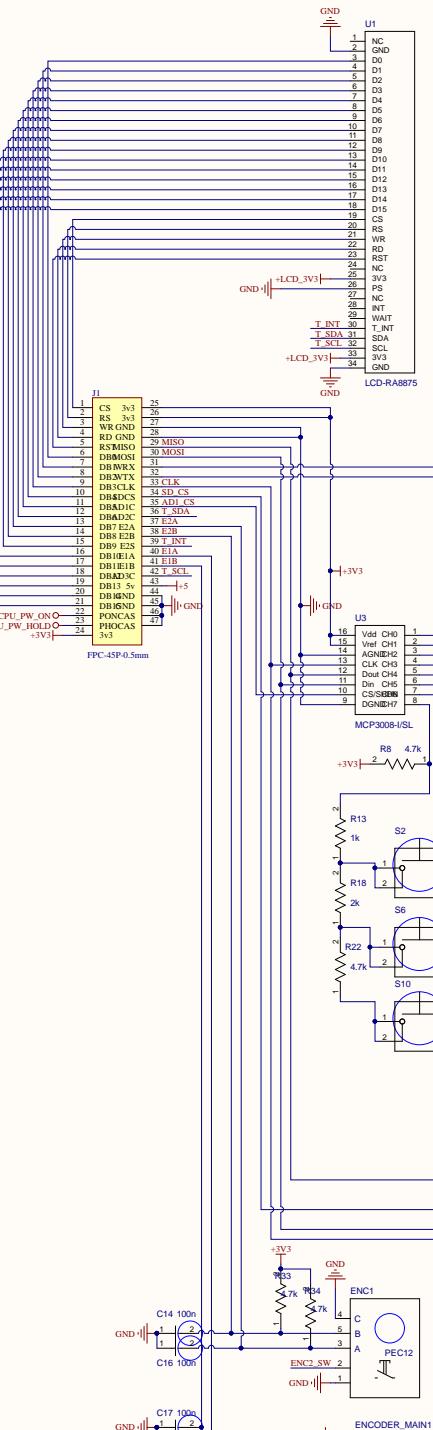


A

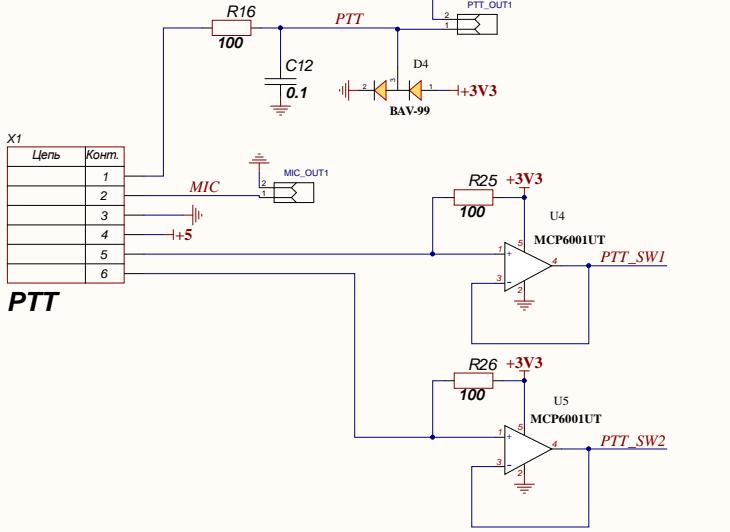
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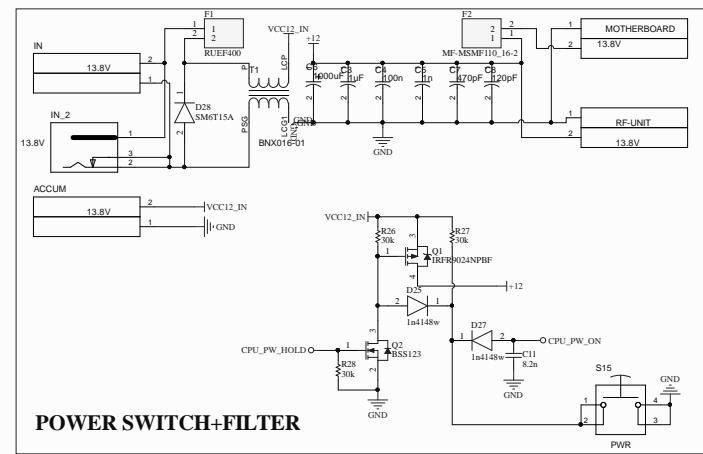
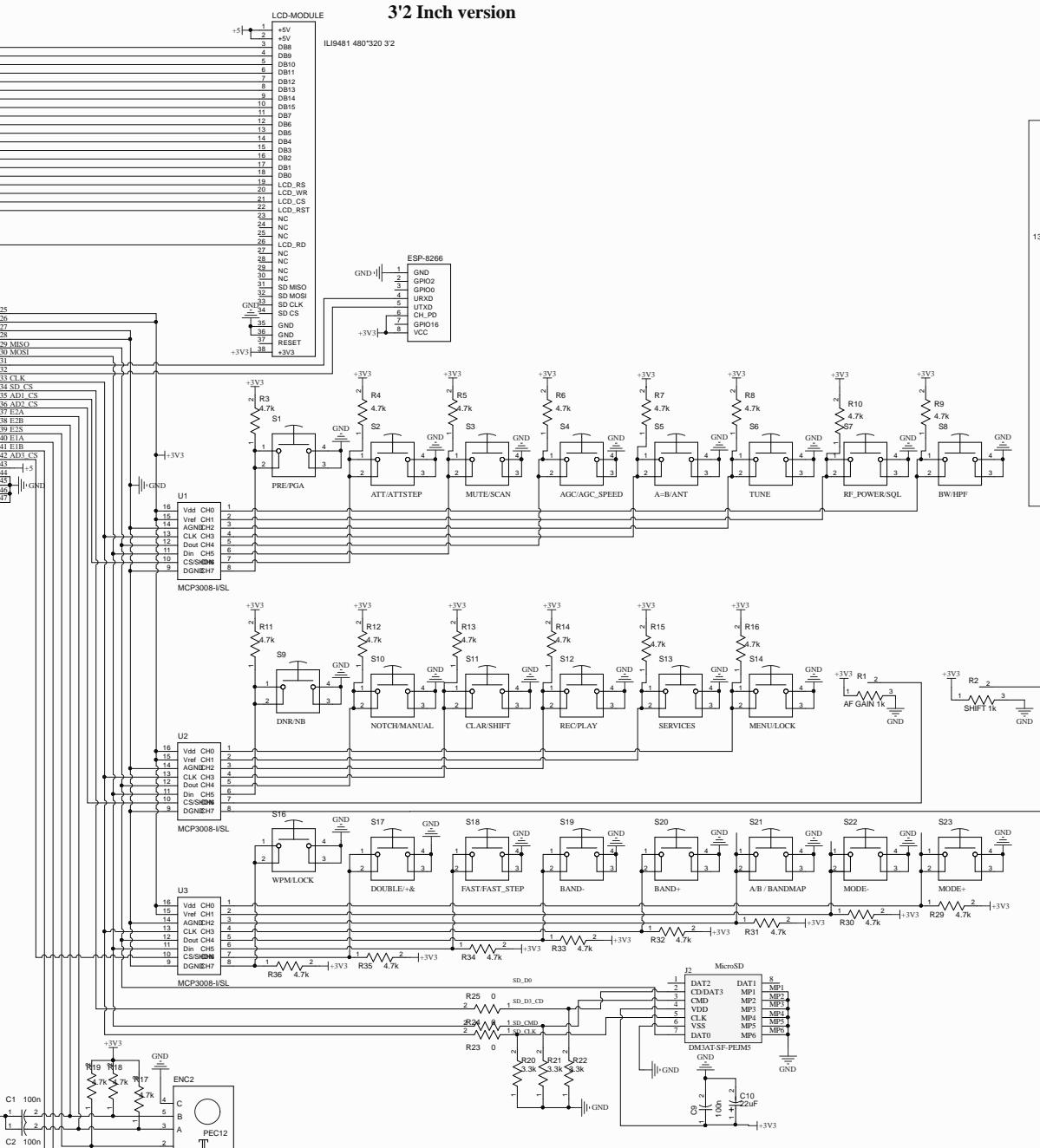
C

D



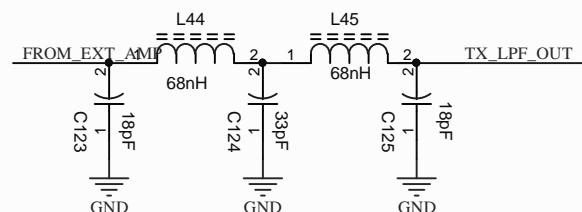
TANGENT



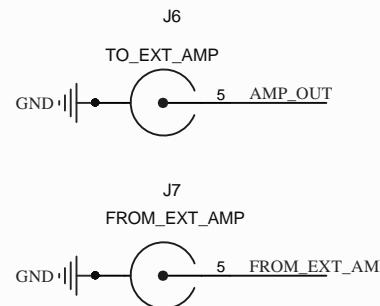
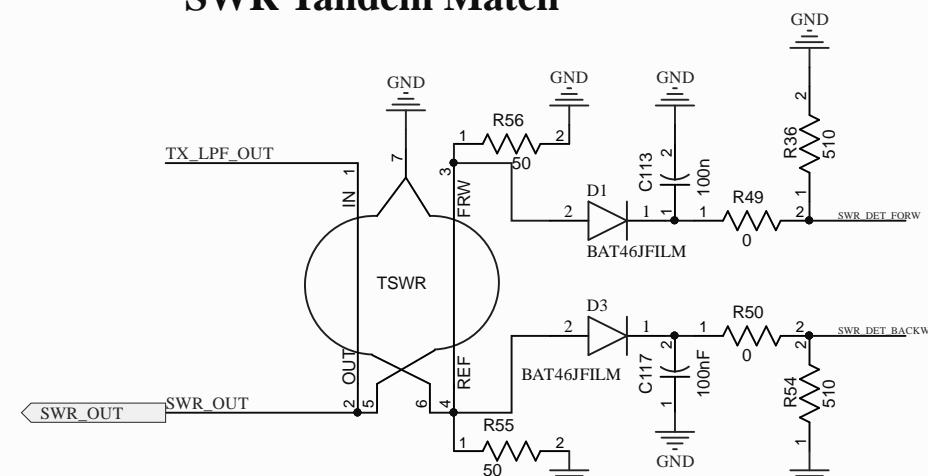


**TX\_LPF**

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**

2 провода 0.9мм пропущено через бинокль

по диагонали пропущено и намотано по 10 витков 0.5мм

Title **SWR Tandem Match**

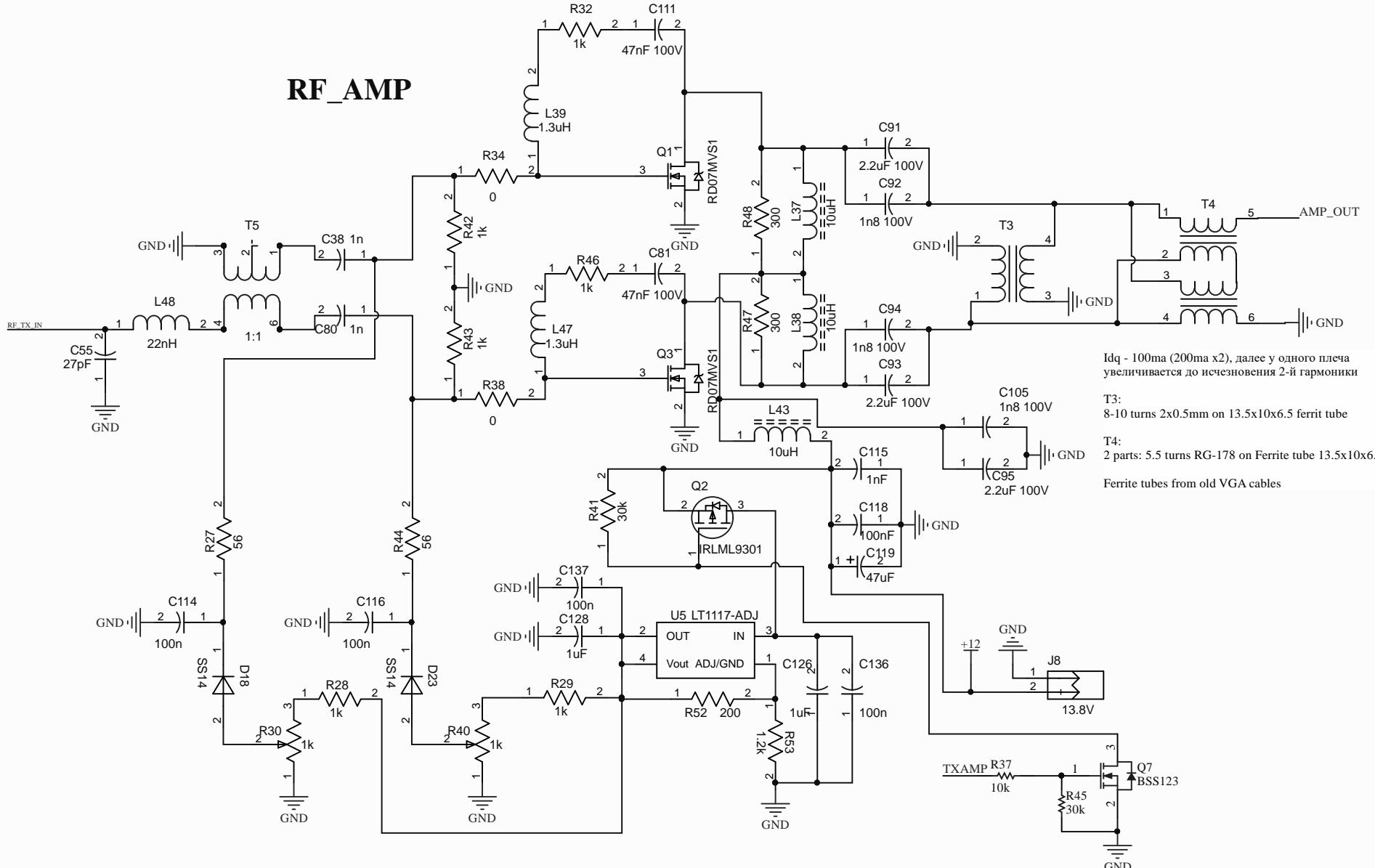
Size: A4 Number:18 Revision:2.0

Date: 08.12.2020 Time: 15:30:05 Sheet:18 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

**Altium**

A

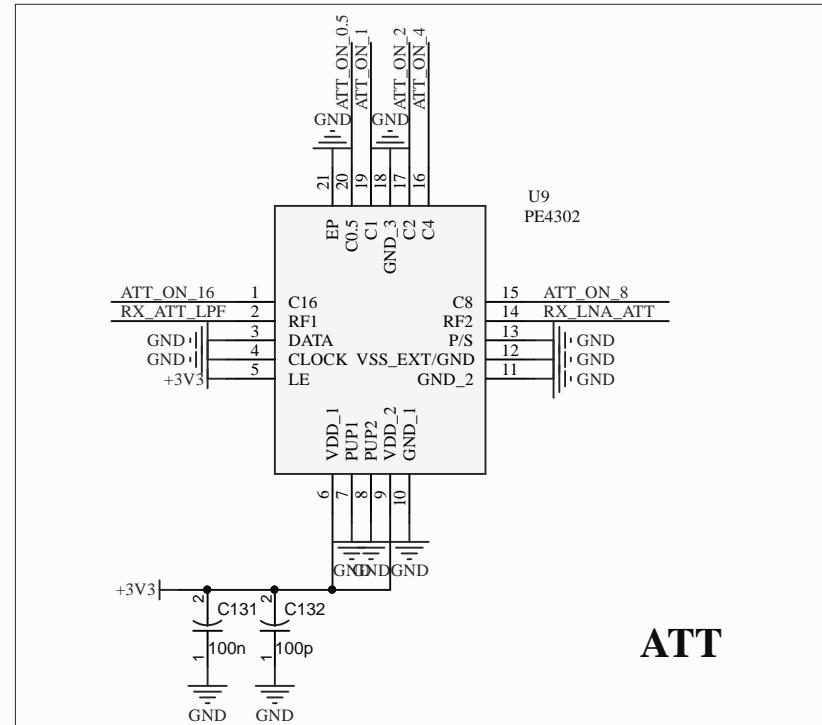
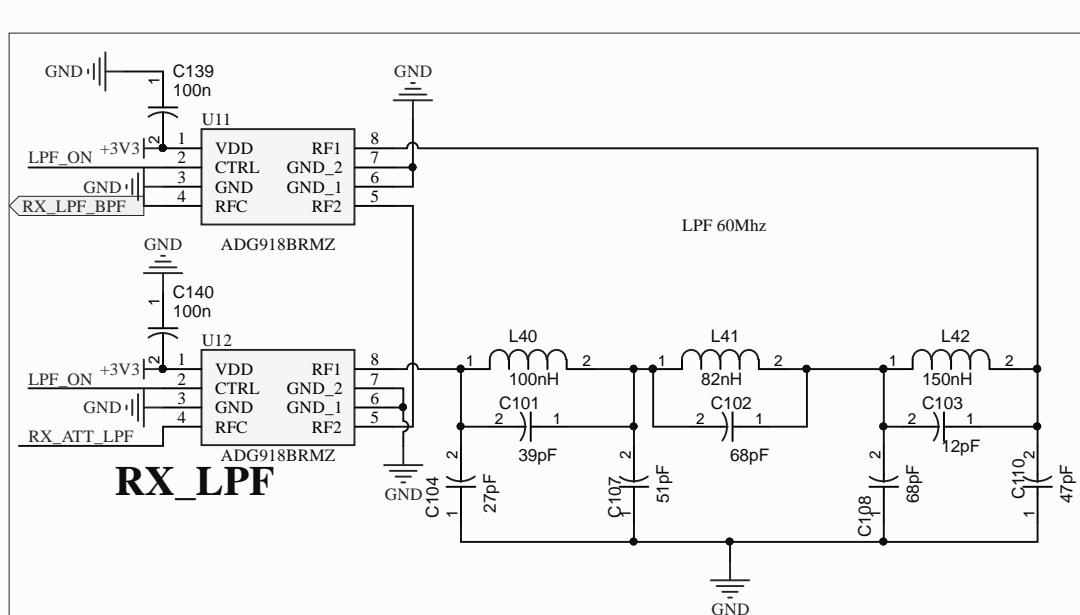
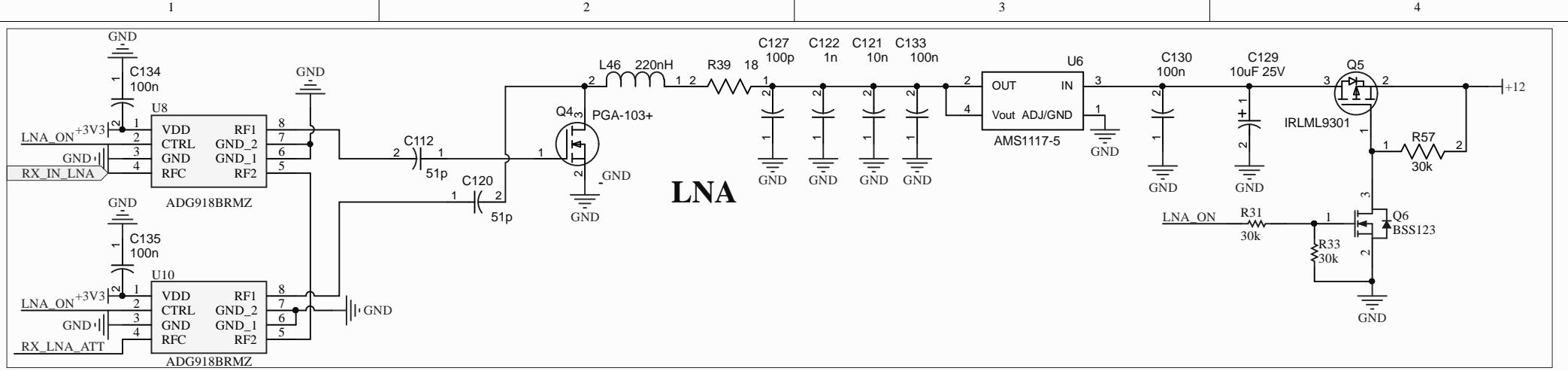
**RF\_AMP**Title **RF\_AMP**

Size: A4 Number:17 Revision:2.0

Date: 08.12.2020 Time: 15:30:06 Sheet:17 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM\_DESIGNER\RF-UNIT\RF\_AMP.SchDoc

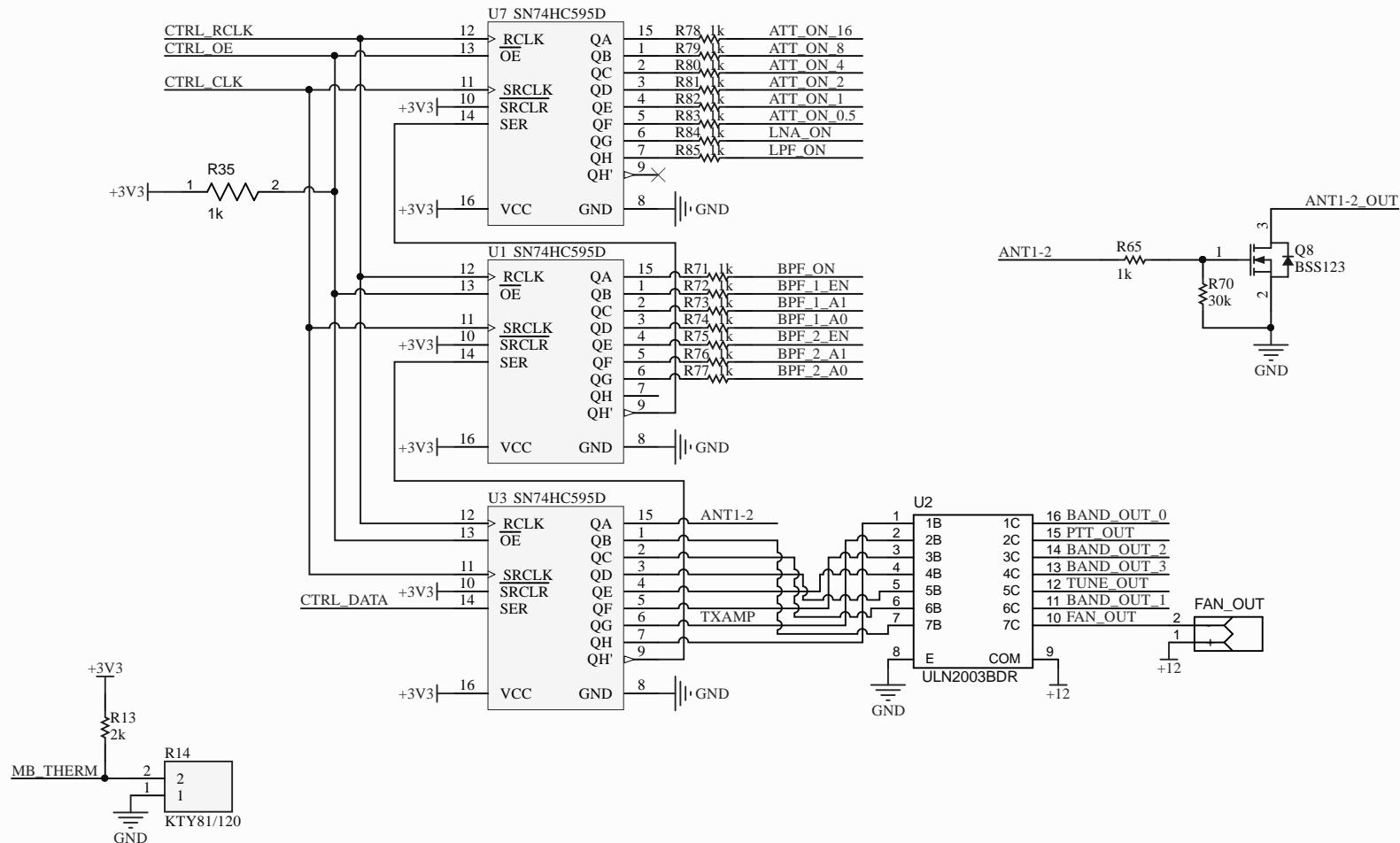
**Altium**



Title <b>LNA</b>			*
Size: A4	Number:16	Revision2.0	*
Date: 08.12.2020	Time: 15:30:07	Sheet16 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc			

**Altium**

A

Title **CONTROL**

Size: A4 Number:15 Revision:2.0

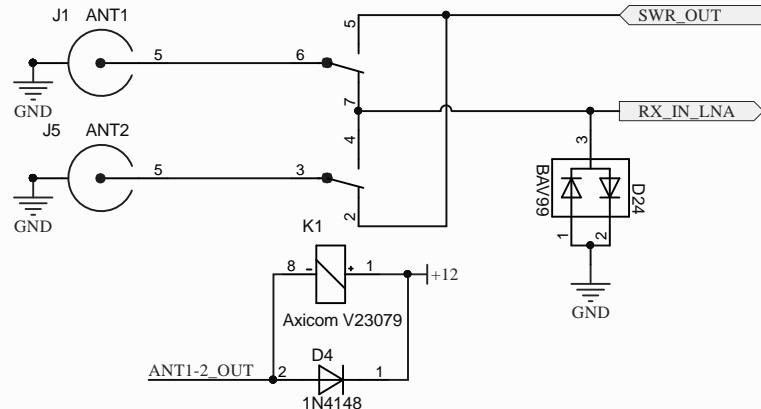
Date: 08.12.2020 Time: 15:30:09 Sheet 15 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\RF-UNIT\CONTROL.SchDoc

**Altium**

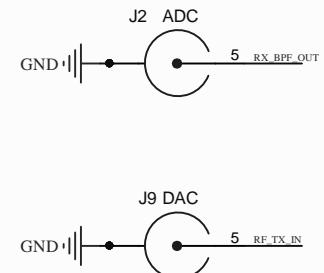
A

## **TXRX\_COMUTATOR**



B

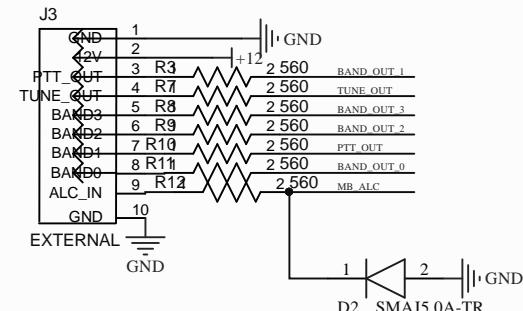
CONN



c

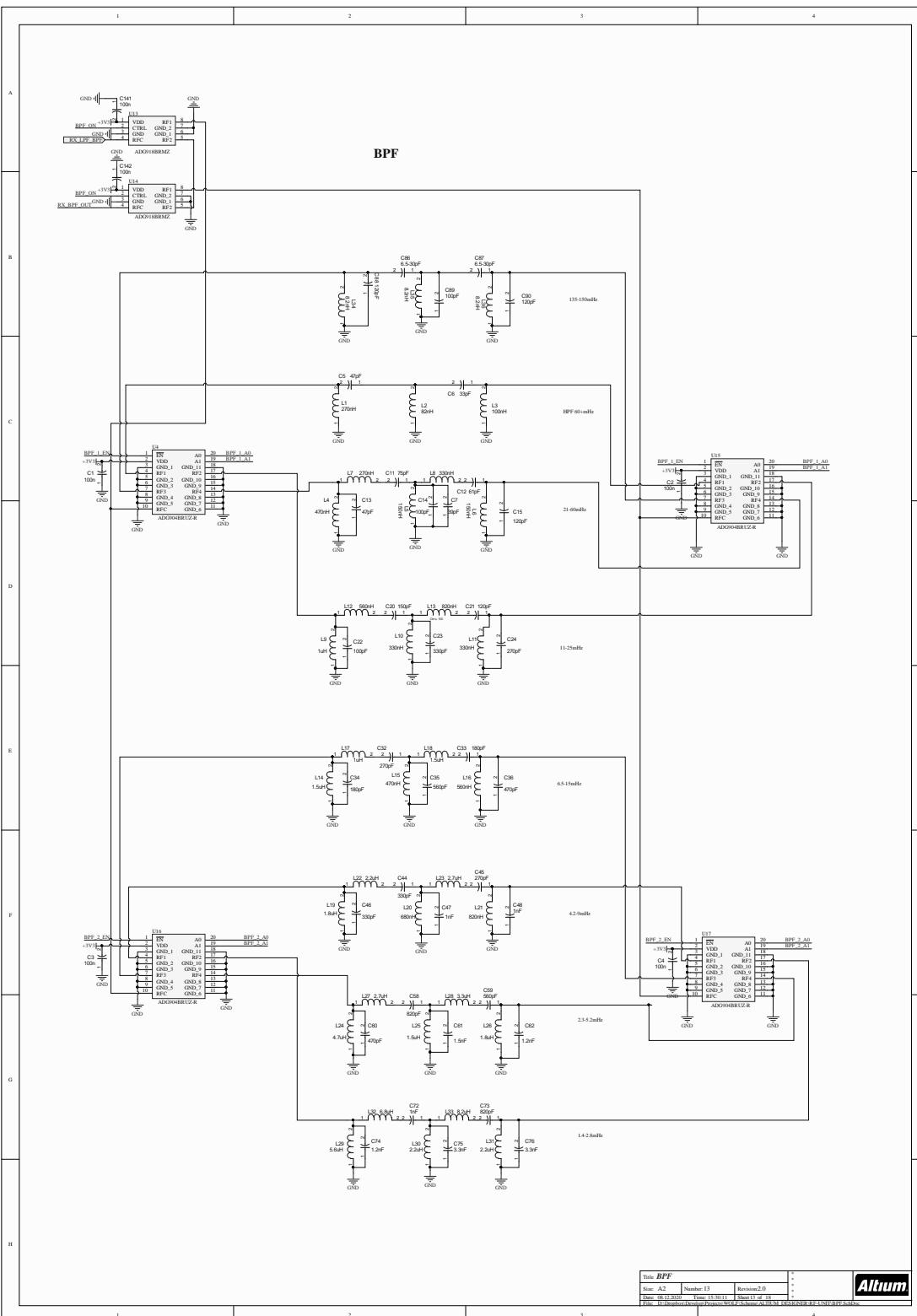
$+3V_3$	1	$+3V_3$
GND	2	GND
RCLK	3	CTRL_RCLK
CLK	4	CTRL_CLK
OE	5	CTRL_OE
DATA	6	CTRL_DATA
SWRF	7	SWR_DET_FORW
SWRB	8	SWR_DET_BACKW
THERM	9	MB_THERM
ALC	10	MB_ALC

## MOTHERBOARD

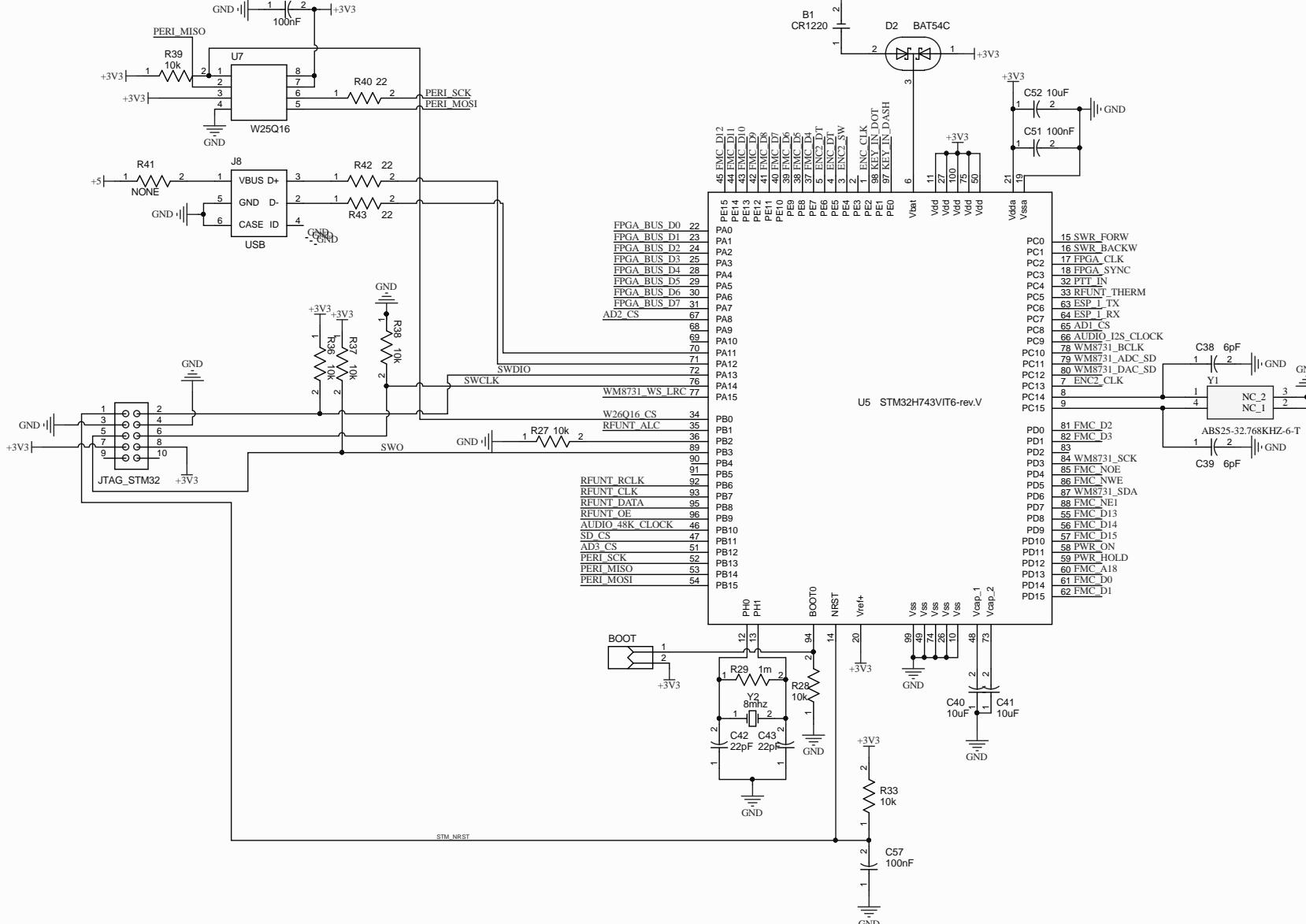


D

Title <b><i>CONN</i></b>	*		
Size: A4	Number:14		*
Revision2.0			*
Date: 08.12.2020	Time: 15:30:10		*
Sheet14 of 18			
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\RF-UNIT\CONN.SchDoc			



# STM32



Title **STM32**

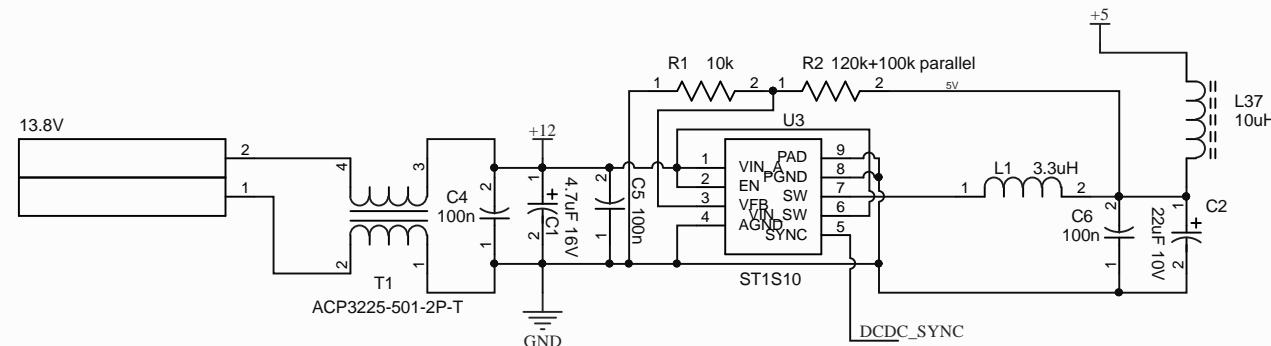
Size: A3 Number: 11 Revision: 2.0

Date: 08.12.2020 Time: 15:30:14 Sheet 11 of 18

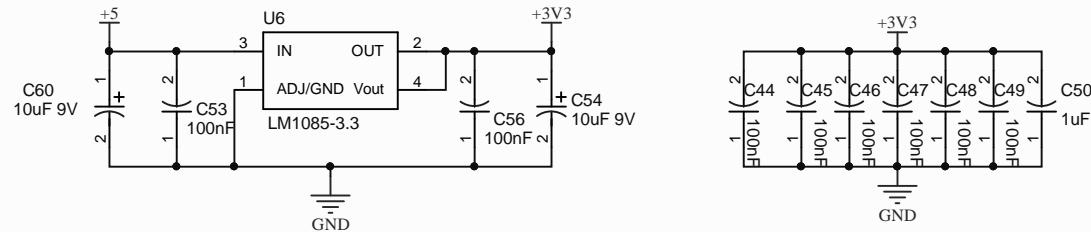
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\STM32.SchDoc



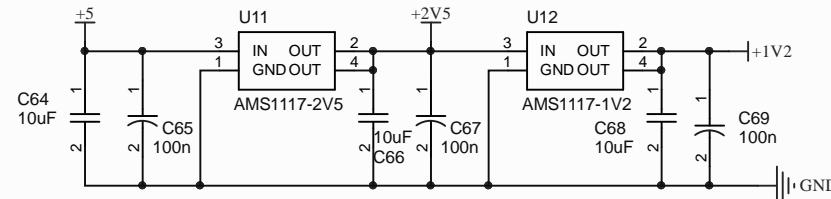
A



B

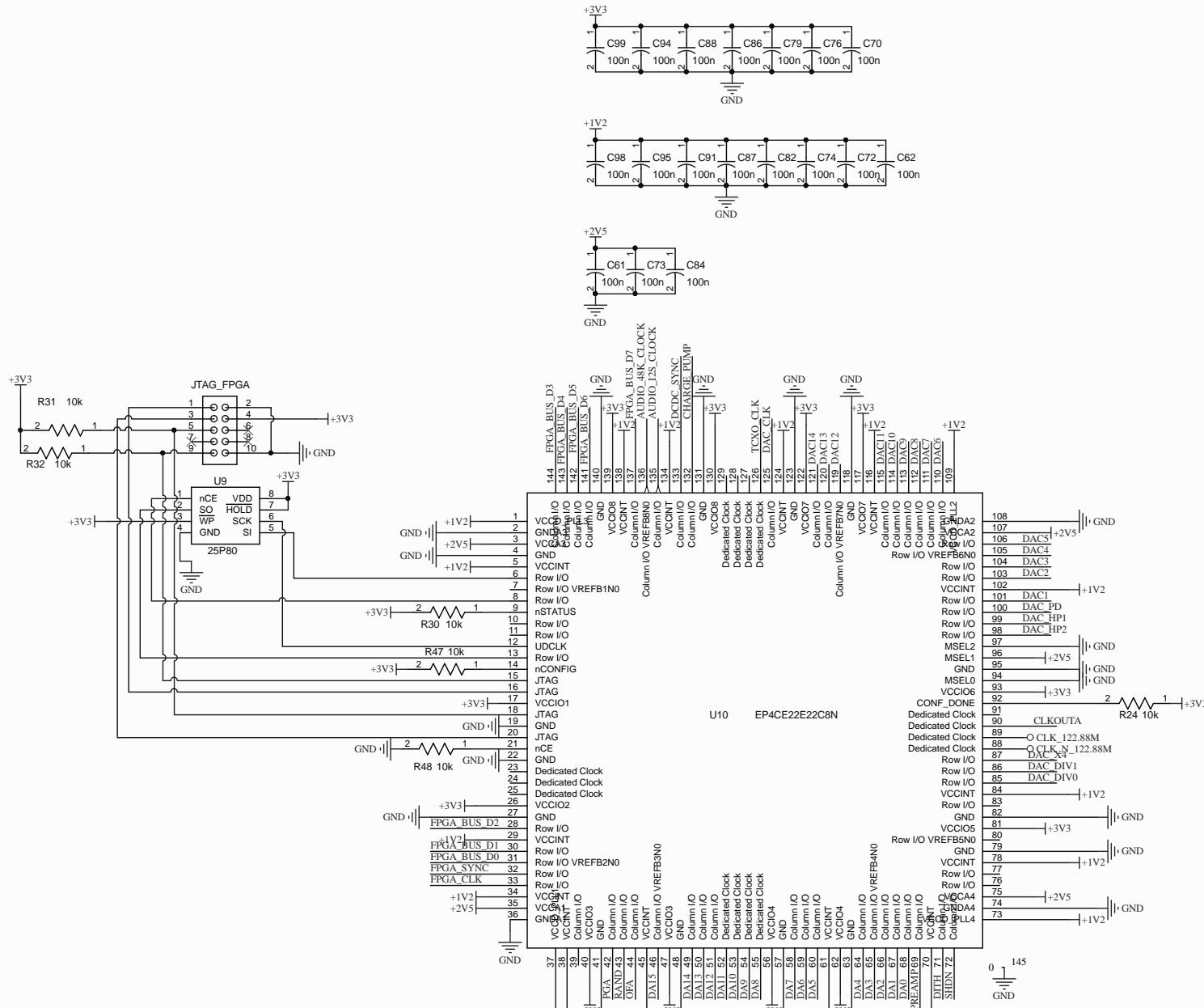


C



D

Title <b>POWER</b>			*
Size: A4	Number:10	Revision2.0	*
Date: 08.12.2020	Time: 15:30:16	Sheet10 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc			*

Title **FPGA**

Size: A3

Number: 9

Revision 2.0

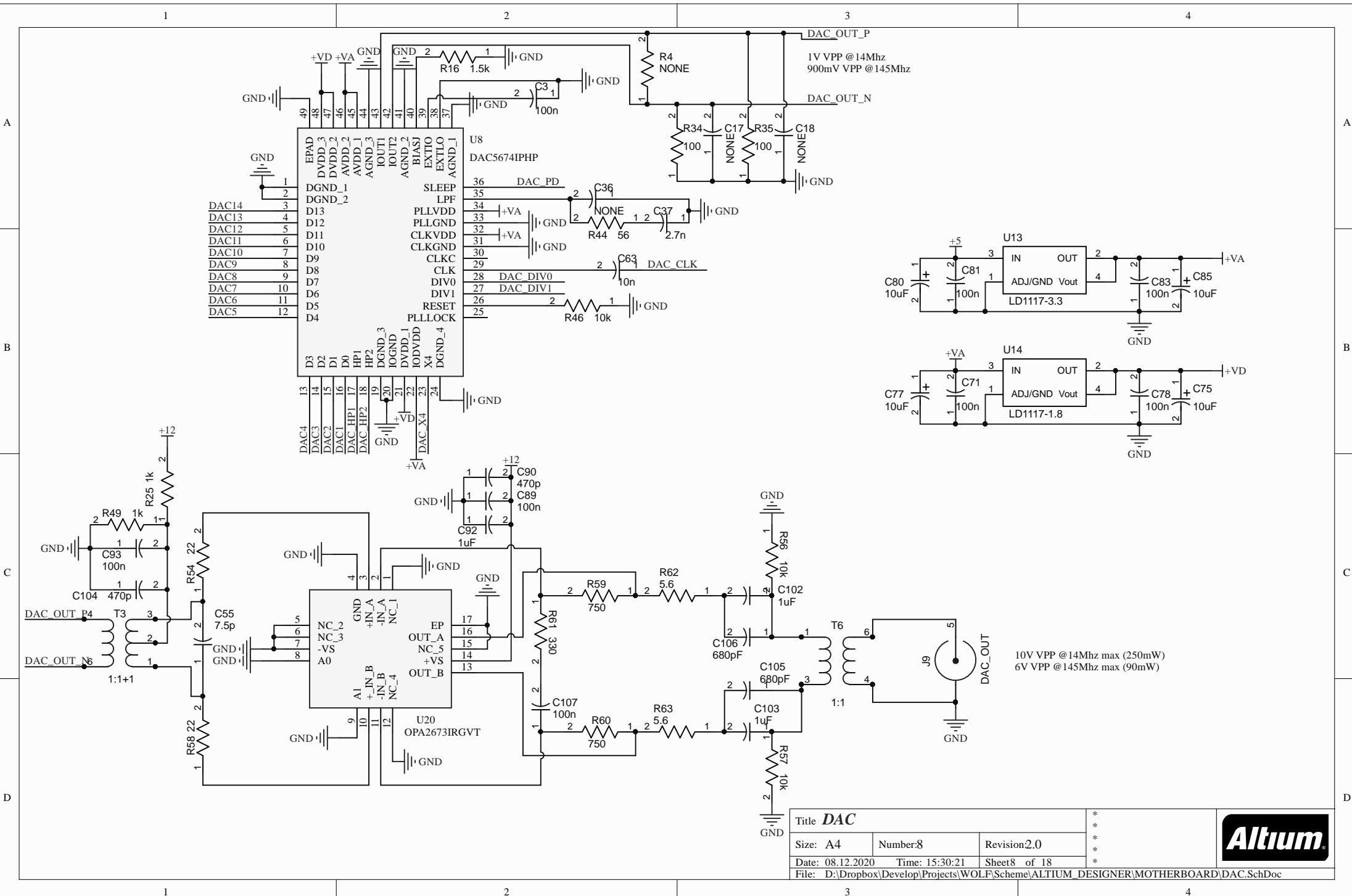
Date: 08.12.2020

Time: 15:30:19

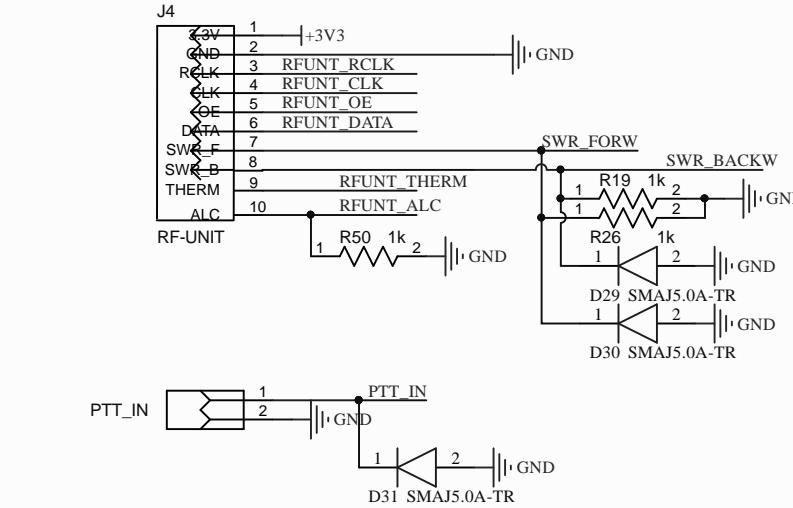
Sheet 9 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\FPGA.SchDoc

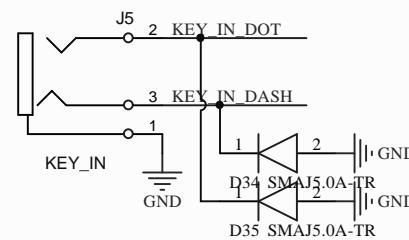




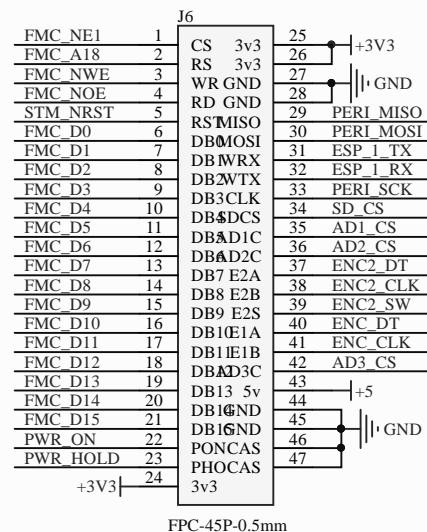
A



B



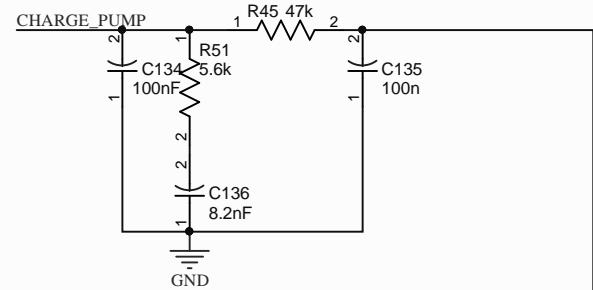
C



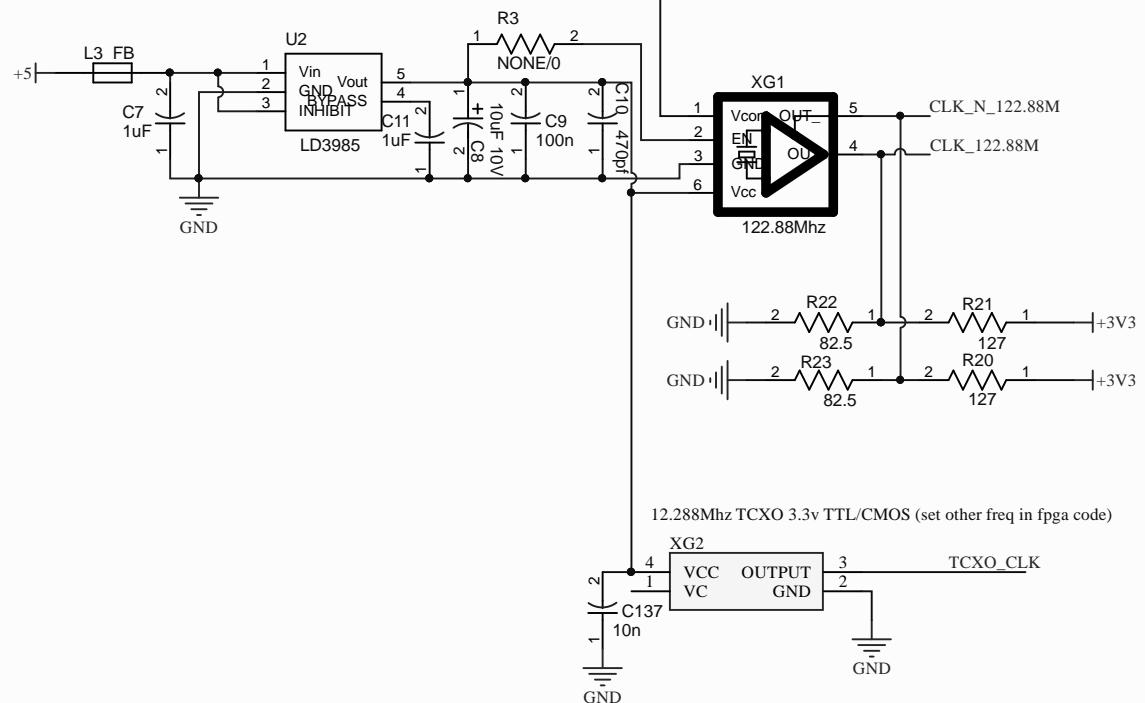
D

Title <b>CONNECTIONS</b>			*
Size: A4	Number:7	Revision2.0	*
Date: 08.12.2020	Time: 15:30:24	Sheet7 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CONNECTIONS.SchDoc			

A



B



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D

Title **CLOCK\_GENERATOR**

Size: A4 Number:6 Revision 2.0

Date: 08.12.2020 Time: 15:30:26 Sheet 6 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM\_DESIGNER\MOTHERBOARD\CLOCK\_GENERATOR.SchDoc

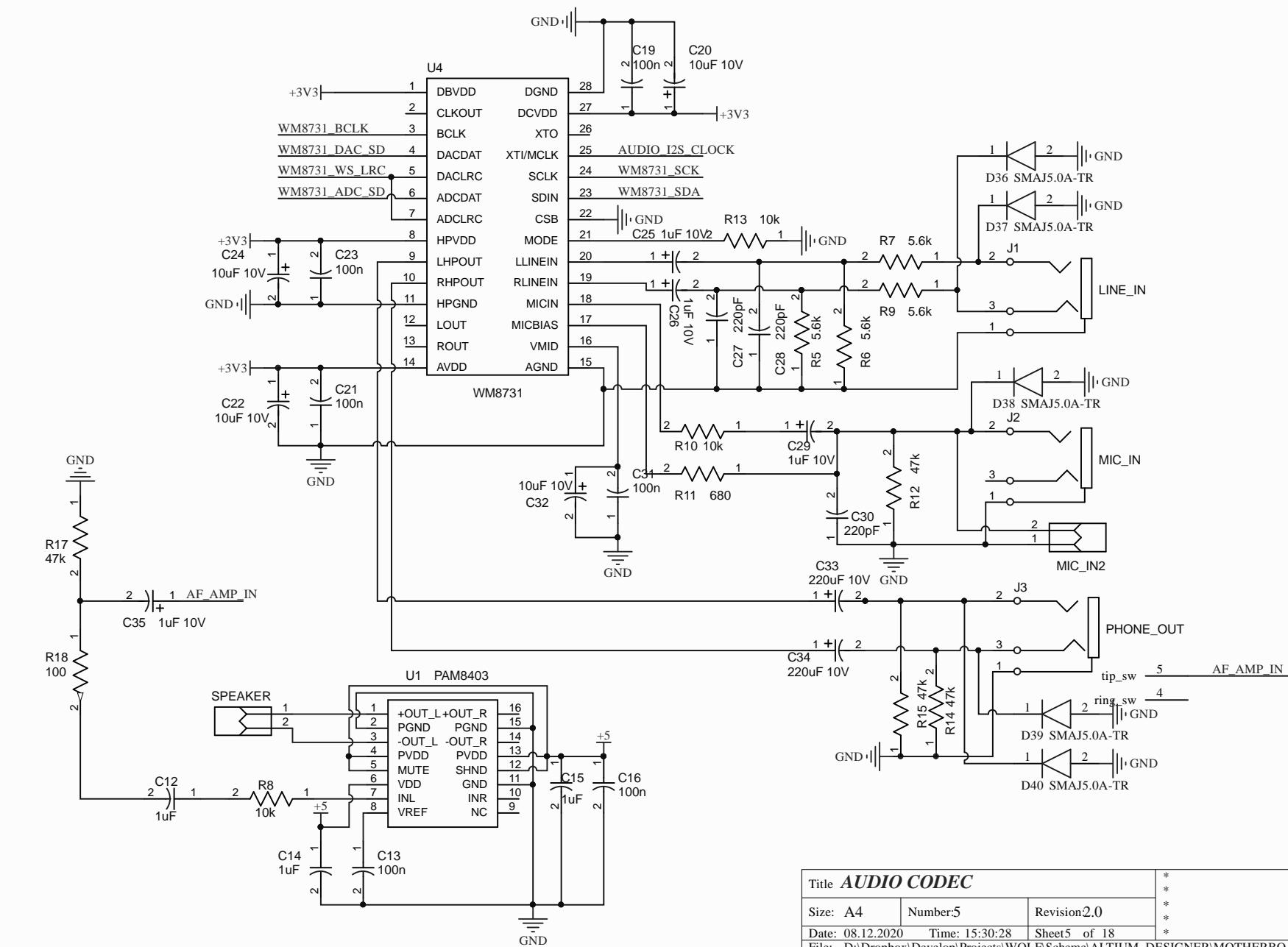
**Altium**

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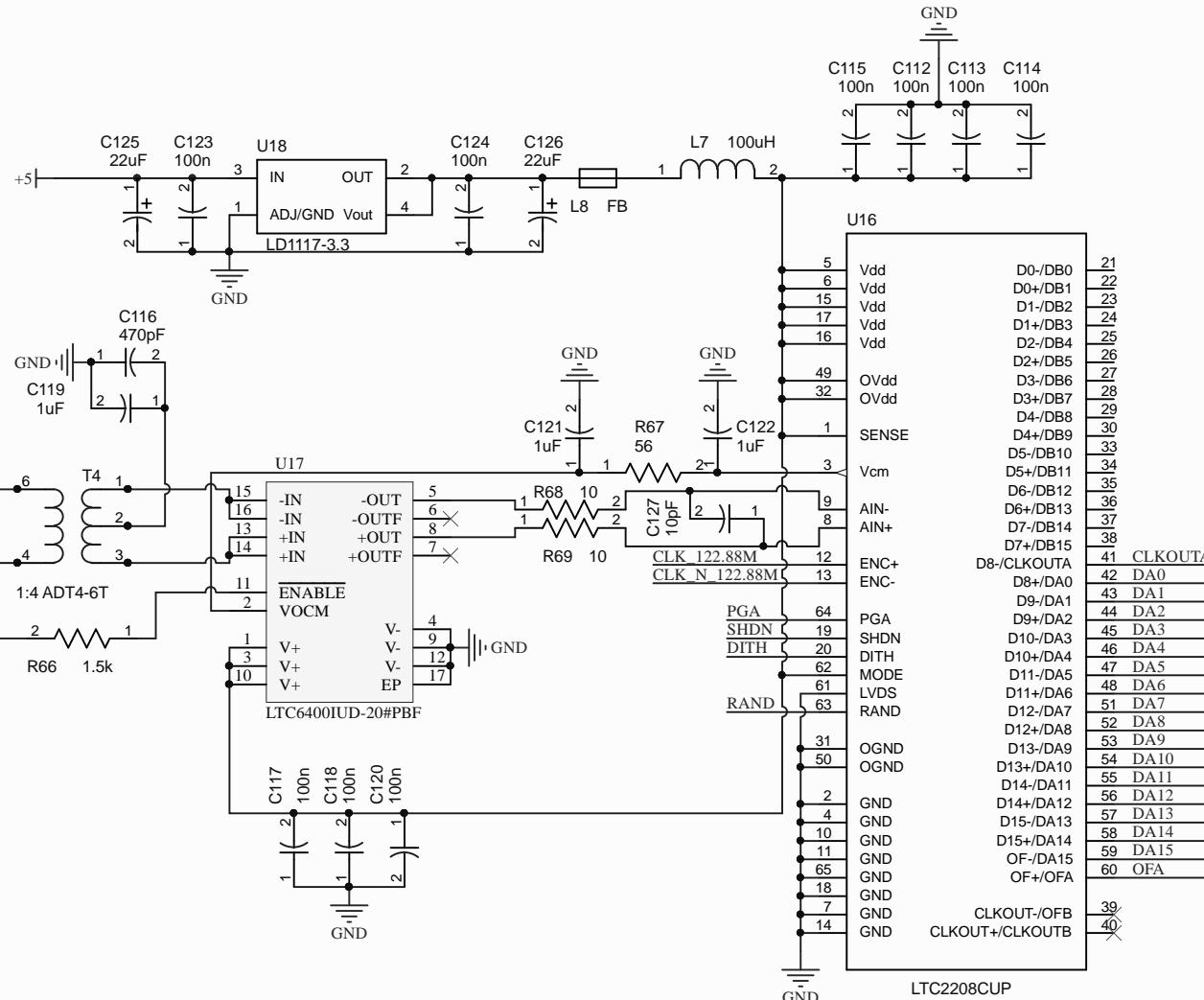
Title **AUDIO CODEC**

Size: A4 Number:5 Revision:2.0

Date: 08.12.2020 Time: 15:30:28 Sheet 5 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\MOTHERBOARD\AUDIO\_CODEC.SchDoc

**Altium**

Title **ADC**

Size: A4 Number:3 Revision 2.0

Date: 08.12.2020 Time: 15:30:30 Sheet 3 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\MOTHERBOARD\ADC.SchDoc

**Altium**