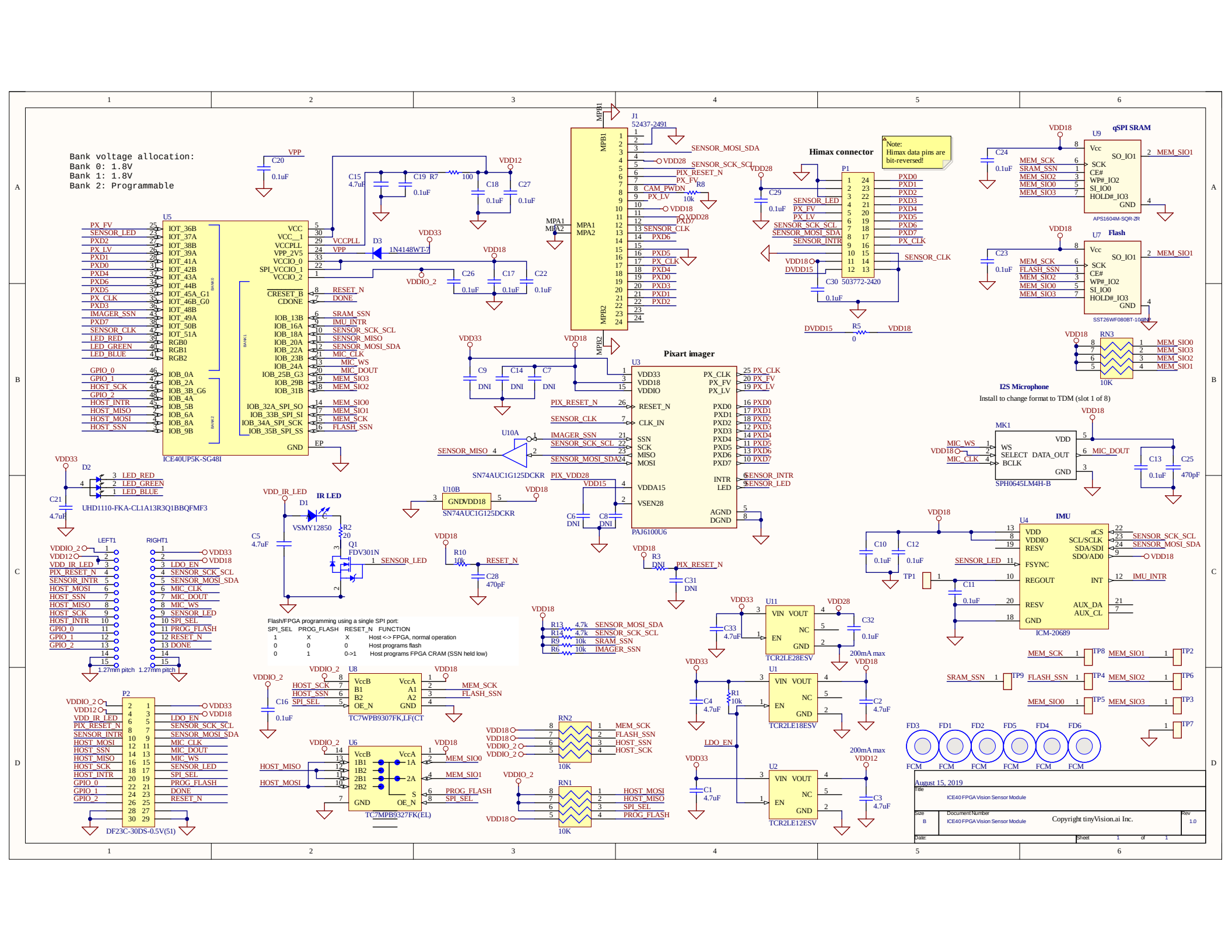
Bank voltage allocation:
Bank 0: 1.8V
Bank 1: 1.8V
Bank 2: Programmable
ICE40UP5K-SG48I
Himax connector
Note:
Himax data pins are bit-reversed!
Pixart imager
PAJ6100U6
qSPI SRAM
APS1604M-SQR-ZR
Flash
SST26WF080BT-104I/MF
I2S Microphone
Install to change format to TDM (slot 1 of 8)
SPH0645LM4H-B
IMU
ICM-20689
IR LED
VSMY12850
UHD1110-FKA-CL1A13R3Q1BBQFMF3
SN74AUC1G125DCKR
TC7WPB9307FK,LF(CT
TC7MPB9327FK(EL)
TCR2LE28ESV
TCR2LE18ESV
TCR2LE12ESV
DF23C-30DS-0.5V(51)
Flash/FPGA programming using a single SPI port:
SPI_SEL PROG_FLASH RESET_N FUNCTION
1 X X Host <-> FPGA, normal operation
0 0 0 Host programs flash
0 1 0->1 Host programs FPGA CRAM (SSN held low)
August 15, 2019
ICE40 FPGA Vision Sensor Module
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