

File: Inverter.sch

Sheet: Power Rails

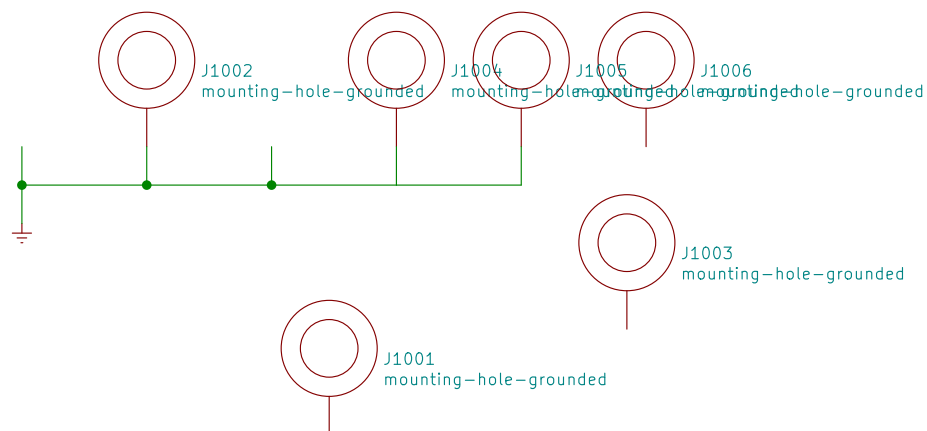
File: PowerRails.sch

Figure 1. A schematic diagram of the experimental design. The subjects were divided into two groups: the control group and the experimental group. The control group received a standard training program, while the experimental group received a modified training program. The experimental group was further divided into two subgroups: the low-intensity group and the high-intensity group. The low-intensity group received a low-intensity training program, while the high-intensity group received a high-intensity training program. The subjects were then subjected to a series of tests to measure their performance and physiological responses.

File: Control.sch

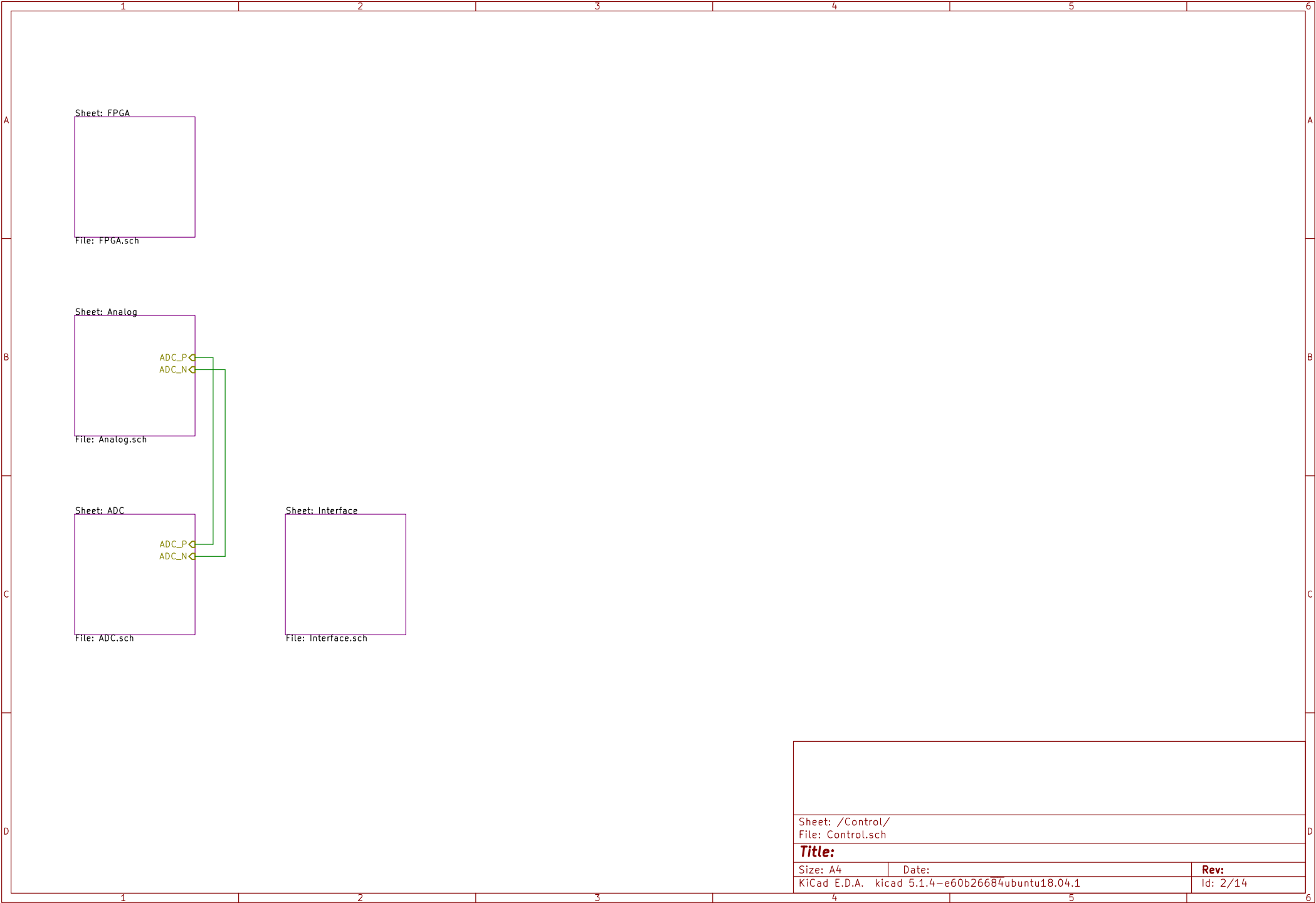
[illegible]

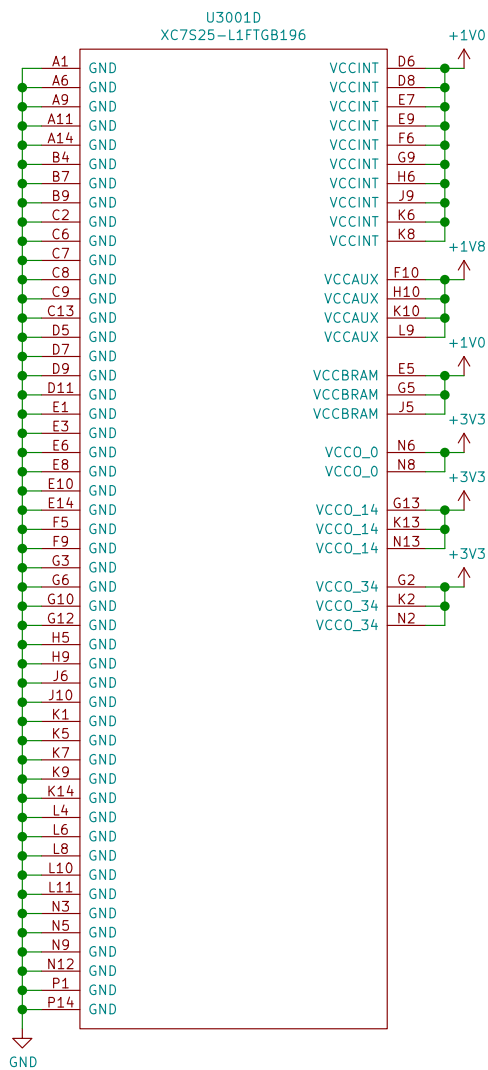
File: PowelInput.sch



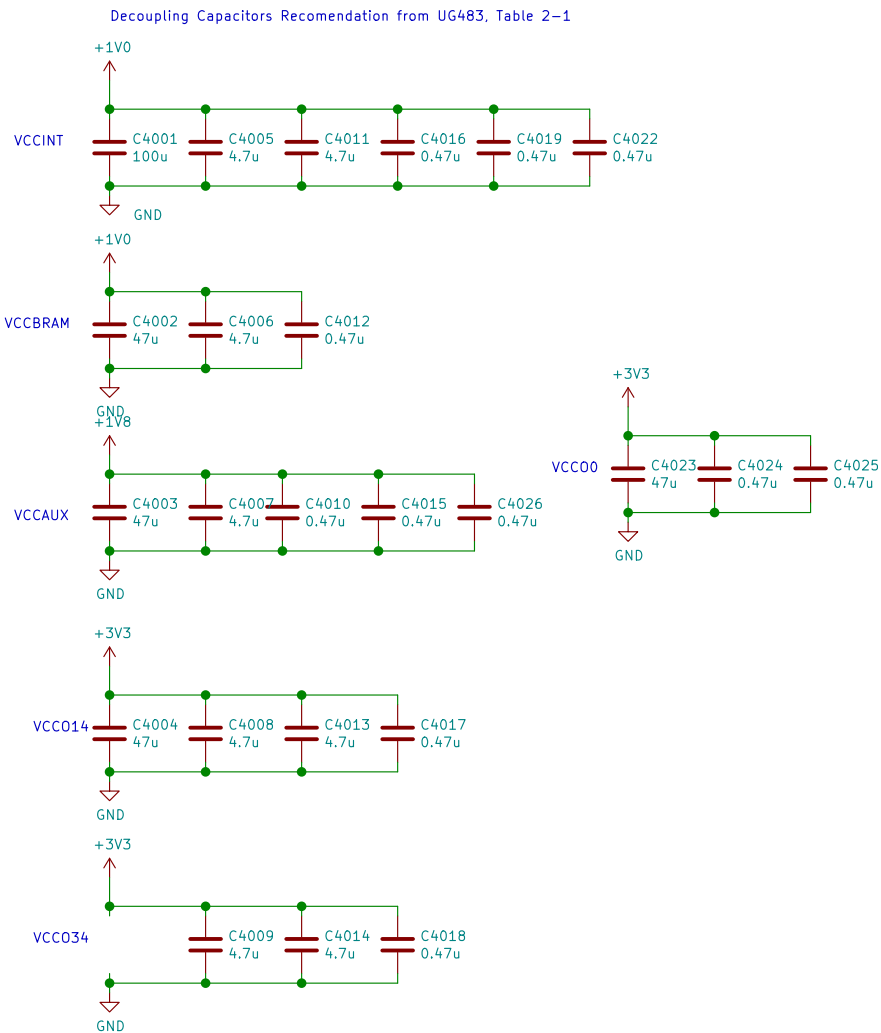
Title:

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Bank 0: 3V3 (config)
Bank 14: 3V3 (due to config)
Bank 34: 3V3 (LVDS)
VCCINT: 1V0
VCCBRAM: 1V0
VCCAUX: 1V8



Sheet: /Control/FPGA/FPGA Power/
File: FPGA_Power.sch

Title:

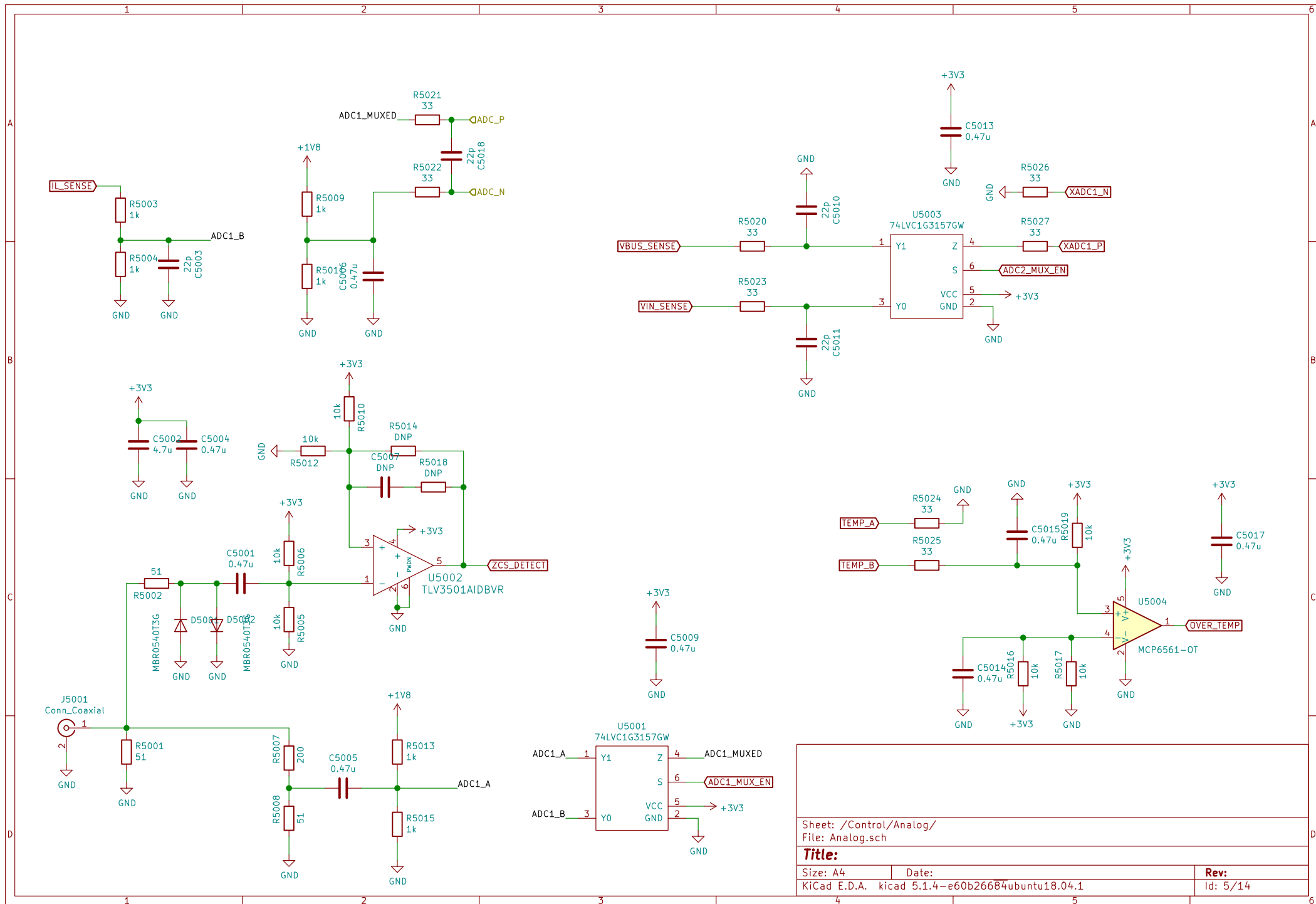
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Date:

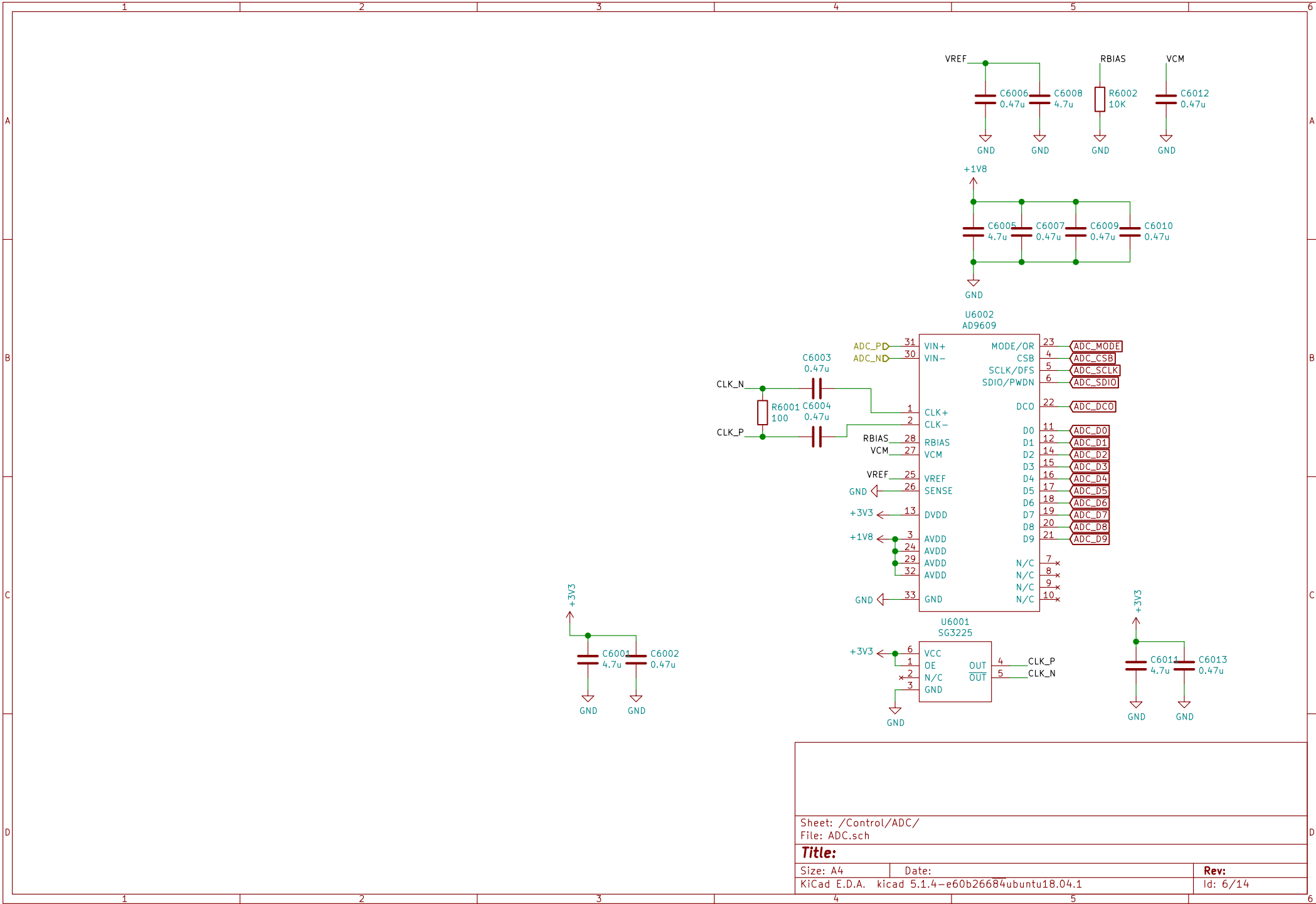
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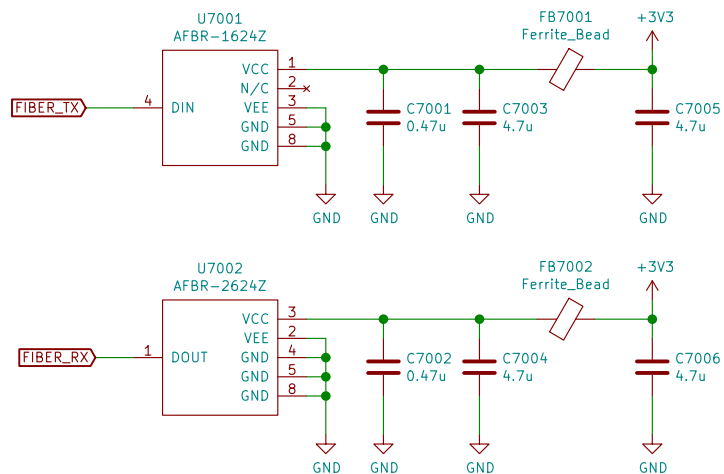
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Sheet: /Control/Analog/ File: Analog.sch		
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Sheet: /Control/Interface/
File: Interface.sch

Title:

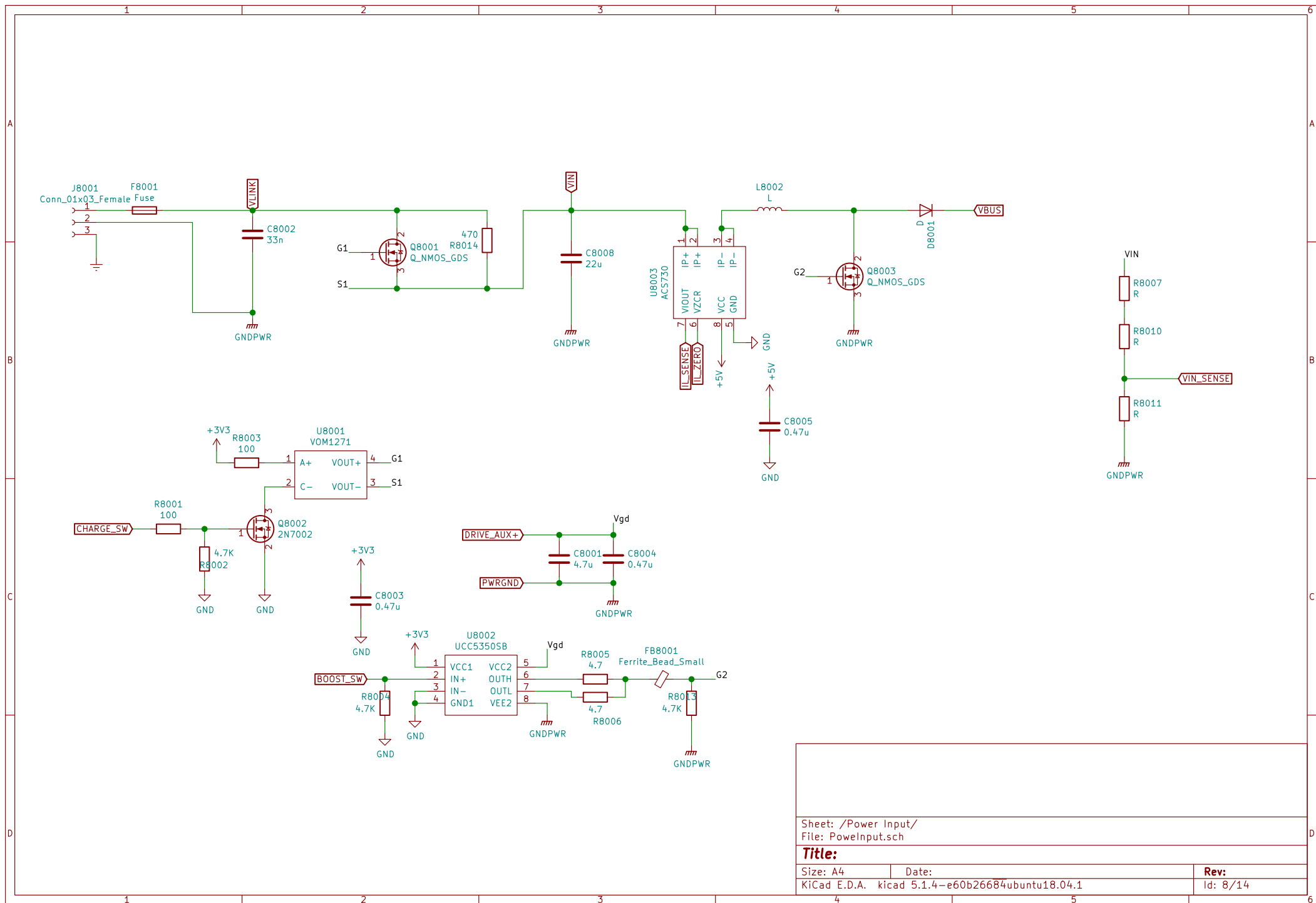
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Sheet: /Power Input/
File: PoweInput.sch

Title:

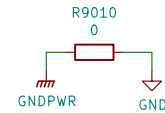
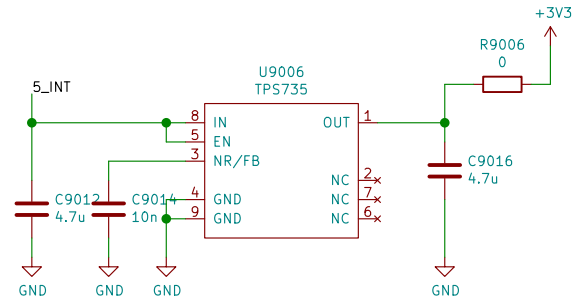
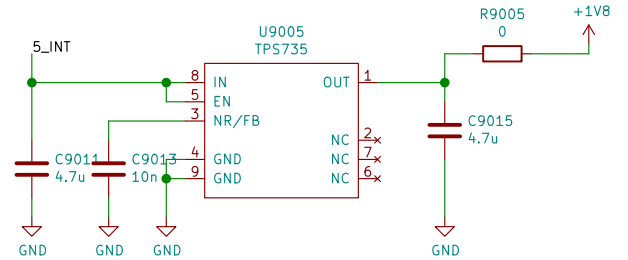
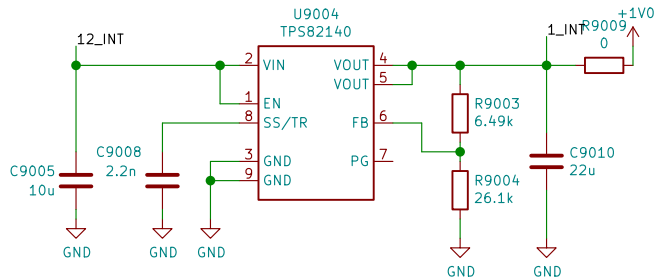
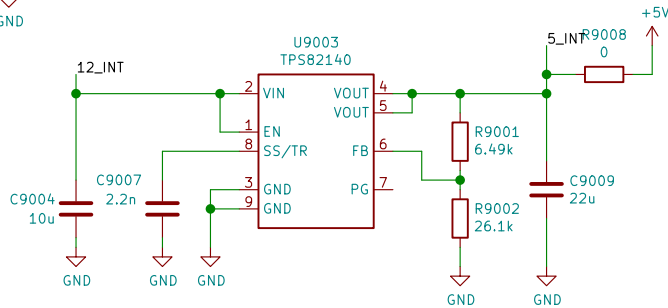
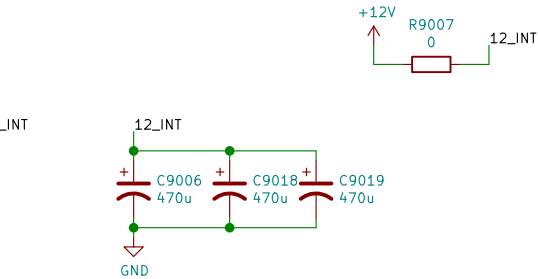
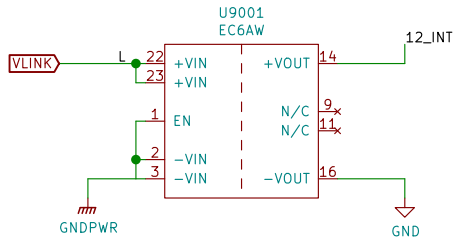
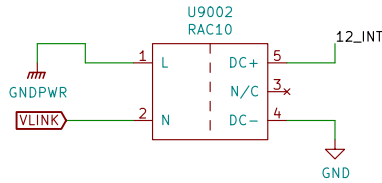
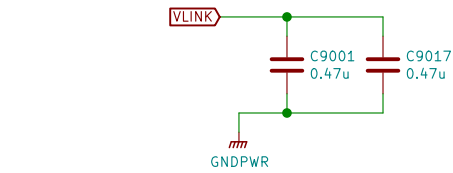
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Power Rails:
FPGA 1V: 0.8A
FPGA 1V8: 0.1A
FPGA 3V3: 0.2A
Analog 1V8 (ADC): 0.1A
Analog 3V3: 0.05
Gate Drive: 24V 1A

Sheet: /Power Rails/
File: PowerRails.sch

Title:

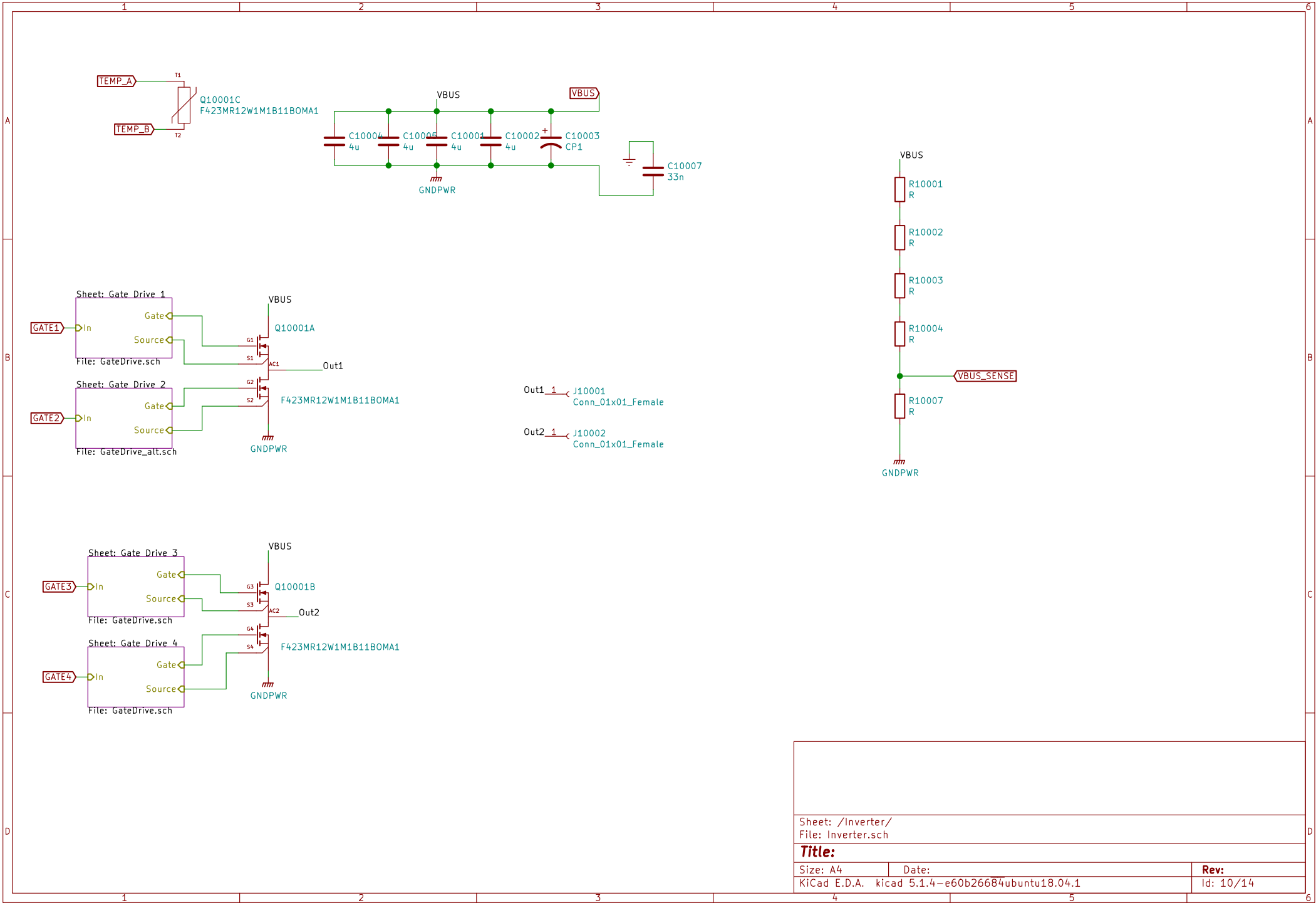
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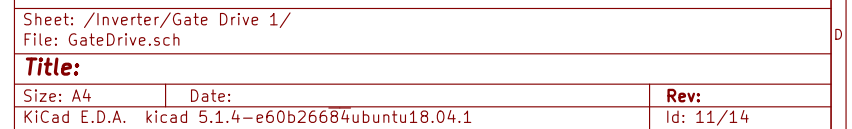
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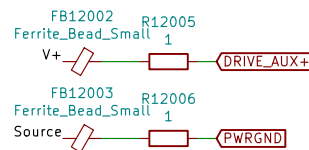
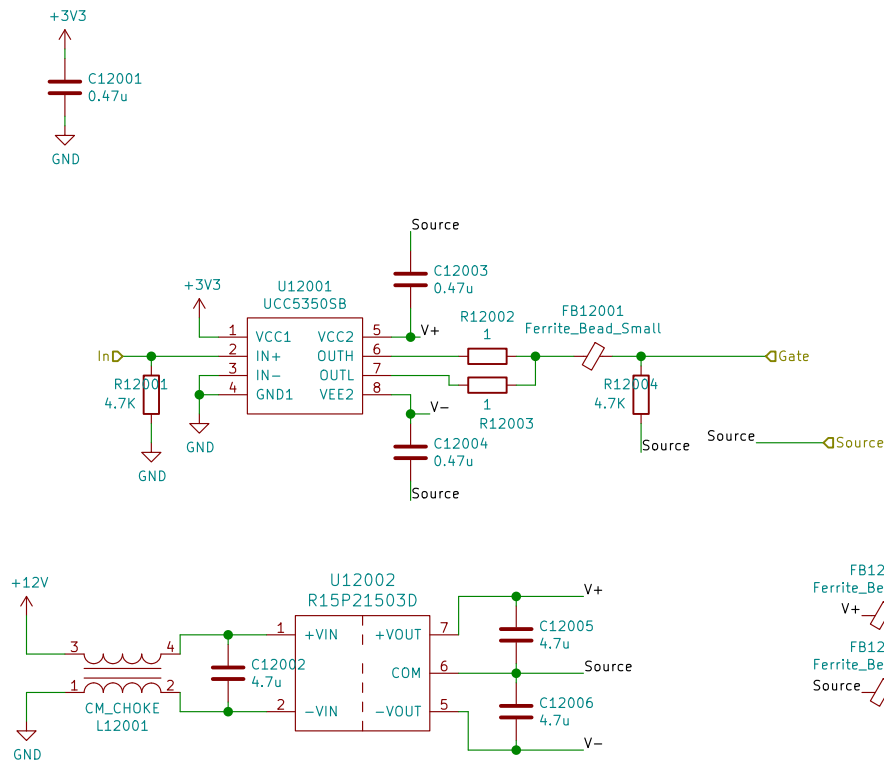
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Sheet: /Inverter/ File: Inverter.sch		
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Sheet: /Inverter/Gate Drive 2/
File: GateDrive_alt.sch

Title:

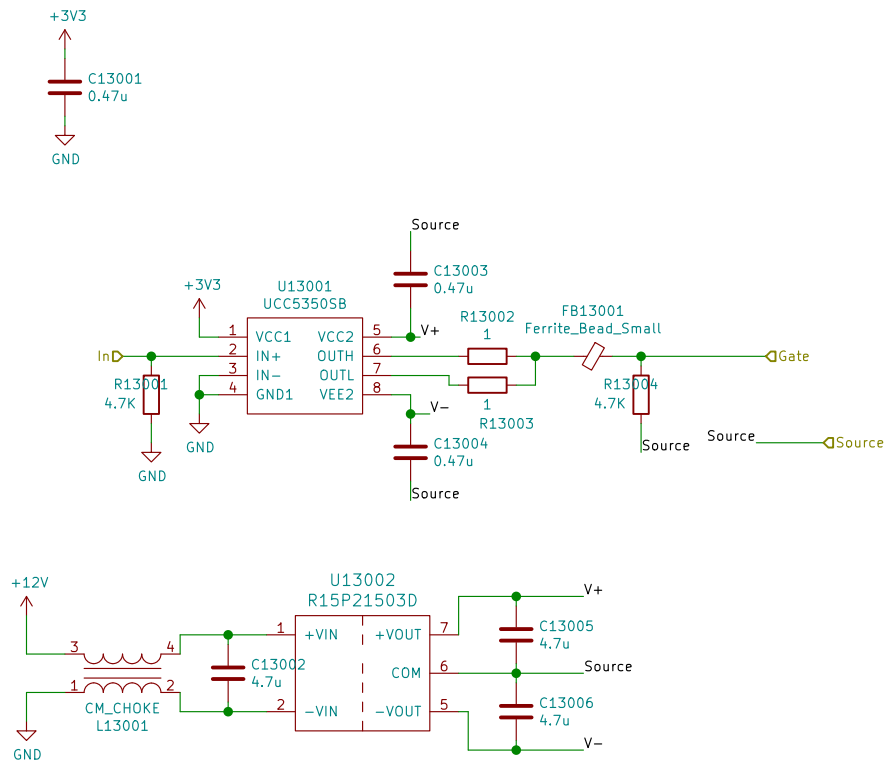
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Sheet: /Inverter/Gate Drive 3/
File: GateDrive.sch

Title:

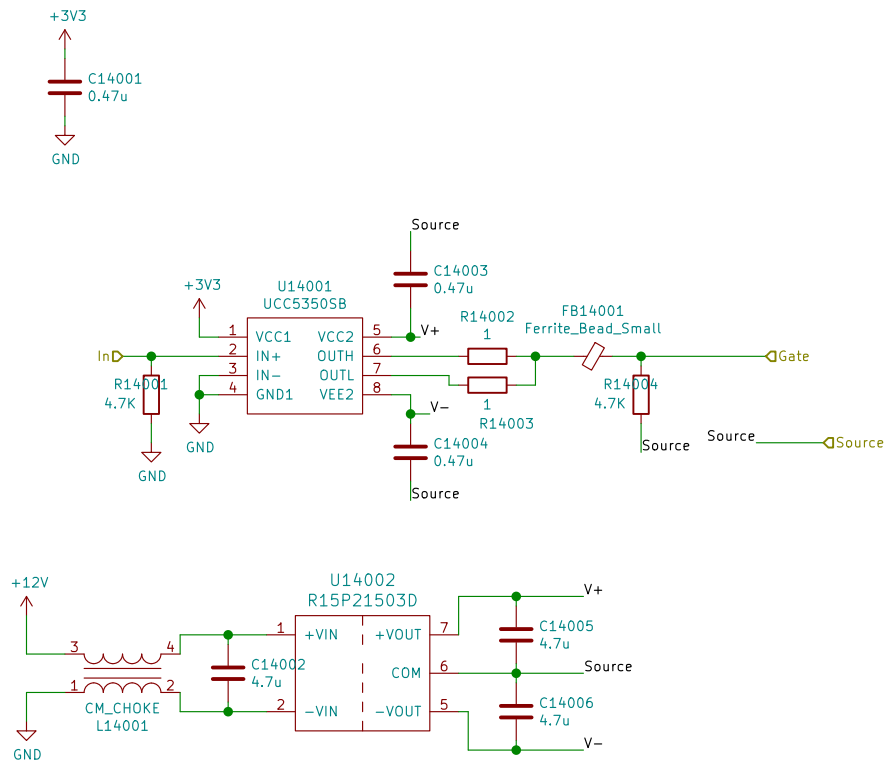
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Date:

KiCad E.D.A. kicad 5.1.4-e60b26684ubuntu18.04.1

Rev:

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Sheet: /Inverter/Gate Drive 4/
File: GateDrive.sch

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Size: A4

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