1. Description

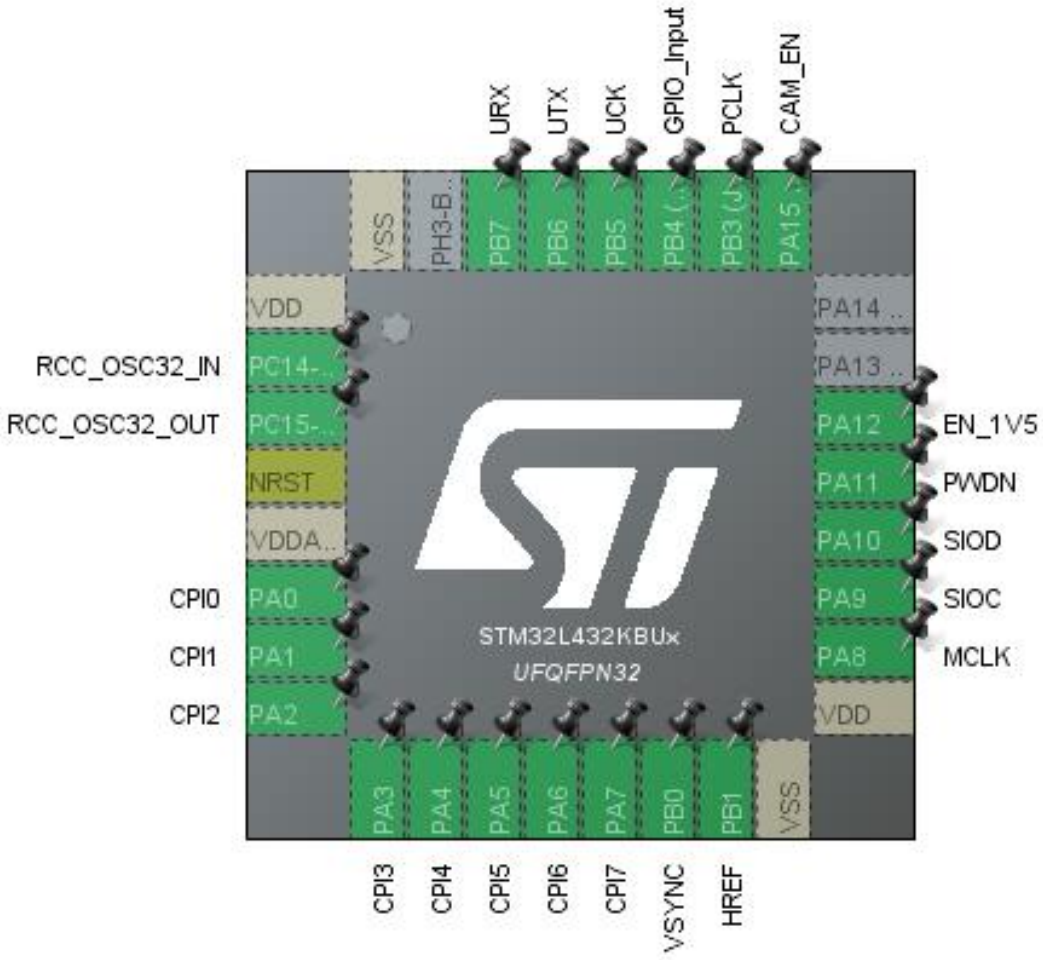
1.1. Project

Project Name	rho_mod_v5
Board Name	rho_mod_v4
Generated with:	STM32CubeMX 5.2.0
Date	05/20/2019

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x2
MCU name	STM32L432KBUx
MCU Package	UFQFPN32
MCU Pin number	32

2. Pinout Configuration

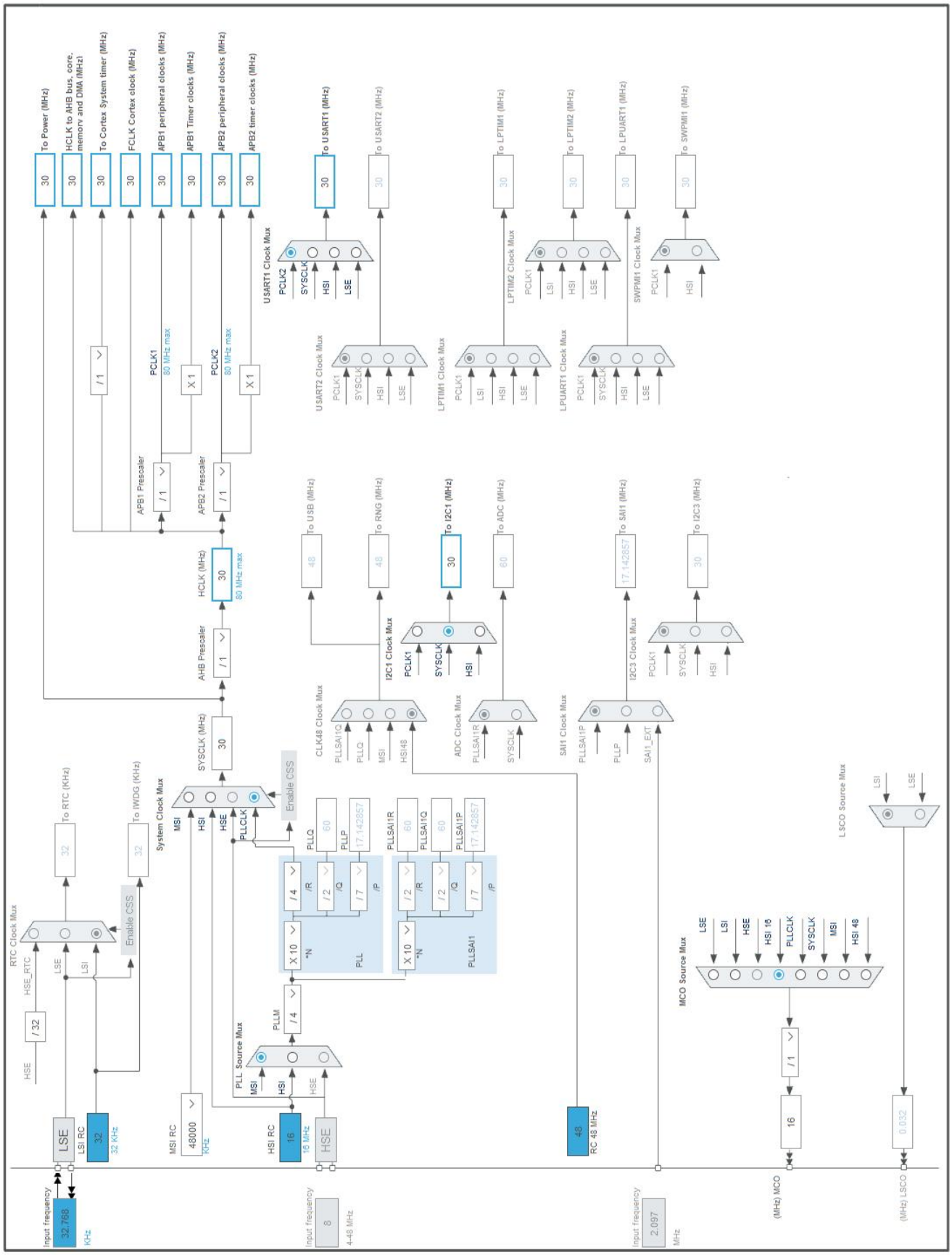


3. Pins Configuration

Pin Number UFQFPN32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
3	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
4	NRST	Reset		
5	VDDA/VREF+	Power		
6	PA0 *	I/O	GPIO_Input	CPI0
7	PA1 *	I/O	GPIO_Input	CPI1
8	PA2 *	I/O	GPIO_Input	CPI2
9	PA3 *	I/O	GPIO_Input	CPI3
10	PA4 *	I/O	GPIO_Input	CPI4
11	PA5 *	I/O	GPIO_Input	CPI5
12	PA6 *	I/O	GPIO_Input	CPI6
13	PA7 *	I/O	GPIO_Input	CPI7
14	PB0	I/O	GPIO_EXTI0	VSYNC
15	PB1	I/O	GPIO_EXTI1	HREF
16	VSS	Power		
17	VDD	Power		
18	PA8	I/O	RCC_MCO	MCLK
19	PA9	I/O	I2C1_SCL	SIOC
20	PA10	I/O	I2C1_SDA	SIOD
21	PA11 *	I/O	GPIO_Output	PWDN
22	PA12 *	I/O	GPIO_Output	EN_1V5
25	PA15 (JTDI) *	I/O	GPIO_Output	CAM_EN
26	PB3 (JTDO-TRACESWO)	I/O	TIM2_CH2	PCLK
27	PB4 (NJTRST) *	I/O	GPIO_Input	
28	PB5	I/O	USART1_CK	UCK
29	PB6	I/O	USART1_TX	UTX
30	PB7	I/O	USART1_RX	URX
32	VSS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	rho_mod_v5
Project Folder	C:\Users\Matthew
Toolchain / IDE	EWARM V7
Firmware Package Name and Version	STM32Cube FW_L4 V1.14.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x2
MCU	STM32L432KBUx
Datasheet	028798_Rev2

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. I2C1

I2C: I2C

7.1.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x007074AF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	**0x60 ***

7.2. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

mode: Master Clock Output

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Enabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.3. SYS

Timebase Source: SysTick

7.4. TIM2

Slave Mode: Combined Reset Trigger Mode

Trigger Source: TI2FP2

Channel2: Input Capture direct mode

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	**Center Aligned mode1 ***
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***
Slave Mode Controller	Combined Reset Trigger mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**1 ***

7.5. USART1

Mode: Synchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	**921600 ***

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	**Transmit Only ***

Clock Parameters:

Clock Polarity	Low
Clock Phase	One Edge
Clock Last Bit	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PA9	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	SIOC
	PA10	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	SIOD
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PA8	RCC_MCO	Alternate Function Push Pull	No pull-up and no pull-down	Low	MCLK
TIM2	PB3 (JTDO-TRACESWO)	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	PCLK
USART1	PB5	USART1_CK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	UCK
	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	UTX
	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	URX
GPIO	PA0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CPI0
	PA1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CPI1
	PA2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CPI2
	PA3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CPI3
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CPI4
	PA5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CPI5
	PA6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CPI6
	PA7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CPI7
	PB0	GPIO_EXTI0	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	VSYNC
	PB1	GPIO_EXTI1	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	HREF
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PWDN
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EN_1V5

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA15 (JTDI)	GPIO_Output	Output Push Pull	**Pull-up ***	Low	CAM_EN
	PB4 (NJTRST)	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM2_CH2/CH4	DMA1_Channel7	Peripheral To Memory	**Very High ***
USART1_TX	DMA2_Channel6	Memory To Peripheral	Low

TIM2_CH2/CH4: DMA1_Channel7 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Byte ***
Memory Data Width:	**Byte ***

USART1_TX: DMA2_Channel6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	1
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line0 interrupt	true	1	1
EXTI line1 interrupt	true	1	1
DMA1 channel7 global interrupt	true	0	0
USART1 global interrupt	true	0	0
DMA2 channel6 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM2 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report