OV9650FSL Color CMOS SXGA (1.3 MegaPixel) Concept Camera Module with OmniPixel® Technology

General Description

The OV9650FSL is a sensor on-board camera and lens module designed for mobile applications where low power consumption and small size are of utmost importance.

Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. All required camera functions are programmable through the serial SCCB interface.

The device can be programmed to provide image output in various fully processed and encoded formats.

The OV9650FSL features the OV9650 CAMERACHIP™. Refer to the *OV9650 Datasheet* for chip-specific information.

Caution: READ THIS FIRST!
Prior to finalizing any mechanical or electrical design for production, consult with OmniVision to confirm any final dimensional or electrical pinout data.

Features

- 1,310,720 pixels, SXGA/VGA format, 1/4" lens
- 8mm x 8mm x 7.22mm module size, flex cable
- Flex cable connector
- 2.5V operation, low power dissipation
- Serial Camera Control Bus (SCCB) interface
- Function controls:
  - Exposure control
  - Gamma
  - Gain
  - White balance
  - Color matrix
  - Color saturation
  - Hue control
  - Windowing

Ordering Information

Product	Package
OV09650-FSL0	8mm x 8mm x 7.22mm Flex Cable

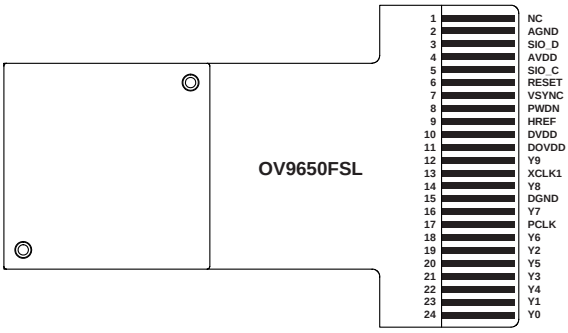
Applications

- Cellular and Picture Phones
- Toys
- PC Multimedia
- Digital Still Cameras

Key Specifications

Array Size		1280 x 1024 (SXGA)
Power Supply	**Core**	1.8VDC ± 10%
	Analog	2.45 to 2.8 VDC
	I/O	2.5V to (V_{DD-A}+0.3V)
Power Requirements	**Active**	50 mW (15 fps, no I/O power)
	Standby	30 µW
Temperature Range	**Operation**	-10°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • GRB 4:2:2 • Raw RGB Data
Lens Size		1/4"
Maximum Image Transfer Rate	**SXGA**	15 fps
	VGA	30 fps
	QVGA, QQVGA, CIF	60 fps
	QCIF, QQCIF	120 fps
Sensitivity		0.9 V/Lux-sec
S/N Ratio		40 dB
Dynamic Range		62 dB
Scan Mode		Progressive
Max. Exposure Interval		1050 x t_{ROW}
Gamma Correction		Programmable
Pixel Size		3.18 µm x 3.18 µm
Dark Current		30 mV/s at 60°C
Well Capacity		28 Ke
Fixed Pattern Noise		<0.03% of $V_{PEAK-TO-PEAK}$
Image Area		4.13 mm x 3.28 mm
Package Dimensions		8mm x 8mm x 7.22mm

Figure 1 OV9650FSL Pin Diagram



Functional Description

Figure 2 shows the functional block diagram of the OV9650FSL Camera Module. The OV9650FSL includes:

- 1/4" lens
- OV9650 CAMERACHIP image sensor
- Flex cable

Figure 2 Functional Block Diagram

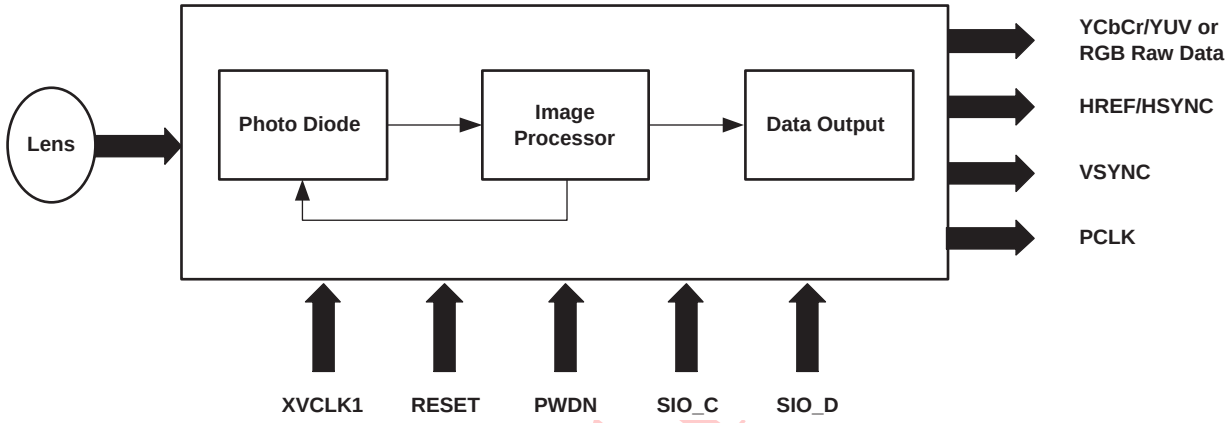
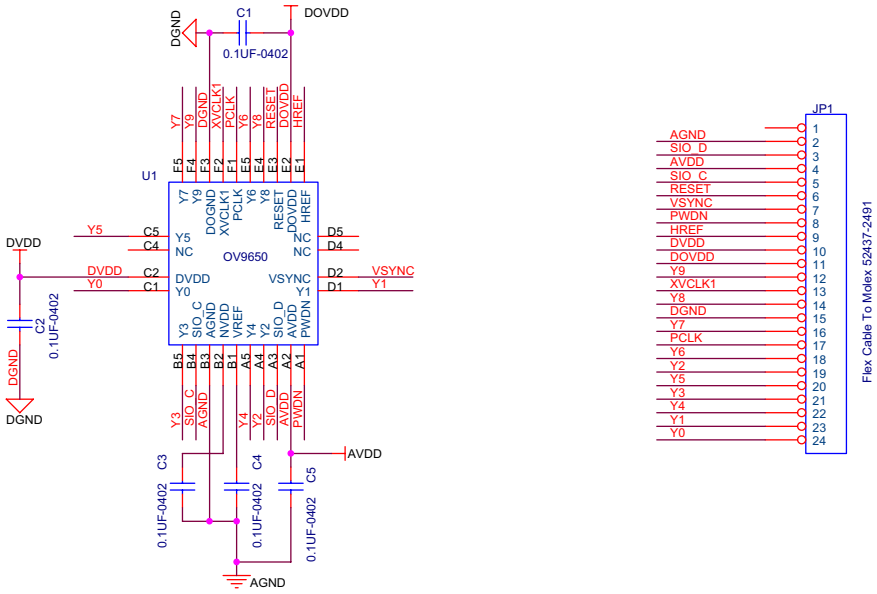


Figure 3 Module Schematic



Note:
Connector PWDN and RESET should be connected to ground il
AVDD is 2.5V sensor analog power.
DVDD is 1.8V sensor digital power.
DOVDD is 2.5V to (AVDD + 0.3V) sensor digital IO power.
Sensor AGND and DGND should be separated and connect to a single point at outside PCB (DO NOT connect inside module).
C1 should close to sensor DOVDD and DOGND.
C2 should close to sensor DVDD and DOGND.
C3 should close to sensor NVDD and AGND.
C4 should close to sensor VREF and AGND.
C5 should close to sensor AVDD and AGND.
Y[9:2] is module YUV and RGB 8bits output (Y[9]: MSB, Y[2]: LSB).
Y[9:0] is module RGB 10 bits output (Y[9]: MSB, Y[0]: LSB).

Imaging Specifications

Table 1 Sensor Image Functions

Sensor Imaging Functions	Description
Auto Exposure	Module automatically sets correct exposure time.
Auto Exposure ON/OFF	Auto exposure can be turned off so the exposure can be set manually.
Auto White Balance (AWB)	AWB without companion processor interaction.
Auto White Balance OFF	AWB can be turned off.
Color Correction	It is possible to adjust for the color filter response of the image sensor as well as for human eye sensitivity.
Bayer Pattern Interpolation	(Mosaic or equivalent) The interpolation must be done prior to downsizing the image to avoid artifacts due to incorrect interpolation.
Electrical Illumination Flicker Elimination	Interference from 50Hz or 60Hz illumination can be suppressed with manually set frame rate divider.
Gamma Correction	Built-in 0.45/1.0
Color Space Conversion	Bayer raw RGB is converted to YCbCr/YUV color space.
Image Size Decimation	Size can be altered using the windowing registers. Quarter-format sub-sampling is also provided.
Image ON/OFF	Image ON/OFF can be controlled by register settings.
RGB Output	RGB raw data output available.
AGC Gain	Automatic Gain Control (AGC)
White Balance	Automatic White Balance

NOTE: OV9650FSL features the OV9650 CAMERACHIP. Refer to the *OV9650 Datasheet* for chip-specific information.

Table 2 Output Specifications

Output Image Formats	Description
Output Formats	SXGA (1280 x 1024 pixels)
	VGA (640 x 480 pixels)
YUV Format	4:2:2 compliant with CCIR656
YUV Order	YUYV or UYVY
Embedded Sync Codes	Sync signals coded in with data output (CCIR656) or output separately.
Data Clipping	According to CCIR656 or no clipping.
Format in Decimation Mode	PCLK verifies whether or not there is data on every cycle.

Pin Description

Table 3 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	NC	–	Reserved - no connect
02	AGND	Power	Analog ground
03	SIO_D	I/O	SCCB serial interface data I/O
04	AVDD	Power	Analog power supply (V_{DD-A} = 2.45 to 2.8 VDC)
05	SIO_C	Input	SCCB serial interface clock input
06	RESET	Function (default = 0)	Clears all registers and resets them to their default values. Active high, internal pull-down resistor.
07	VSYNC	Output	Vertical sync output
08	PWDN	Function (default = 0)	Power Down Mode Selection - active high, internal pull-down resistor. 0: Normal mode 1: Power down mode
09	HREF	Output	HREF output
10	DVDD	Power	Power supply (V_{DD-C} = 1.8 VDC ± 10%) for digital core logic
11	DOVDD	Power	Digital power supply for I/O (V_{DD-IO} = 2.5 to (V_{DD-A}+0.3V))
12	Y9	Output	Output bit[9] - MSB for 10-bit RGB and 8-bit YUV
13	XVCLK1	Input	Crystal clock input
14	Y8	Output	Output bit[8]
15	DGND	Power	Digital ground
16	Y7	Output	Output bit[7]
17	PCLK	Output	Pixel clock output
18	Y6	Output	Output bit[6]
19	Y2	Output	Output bit[2] - LSB for 8-bit YUV
20	Y5	Output	Output bit[5]
21	Y3	Output	Output bit[3]
22	Y4	Output	Output bit[4]
23	Y1	Output	Output bit[1] - for 10-bit RGB only
24	Y0	Output	Output bit[0] - LSB for 10-bit RGB only

NOTE:

Y[9:2] for 8-bit YUV or RGB (Y9 MSB, Y2 LSB)

Y[9:0] for 10-bit RGB (Y9 MSB, Y0 LSB)

Electrical Characteristics

Table 4 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	4.5 V
	V_{DD-C}	3 V
	V_{DD-IO}	4.5 V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+1V
Lead-free Temperature, Surface-mount process		+245ºC
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 5 DC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – Analog	–	2.45	2.5	2.8	V
V_{DD-C}	DC supply voltage – Core	–	1.62	1.8	1.98	V
V_{DD-IO}	DC supply voltage – I/O power	–	2.5	–	V_{DD-A}+0.3V	V
I_{DDA}	Active (Operating) Current	See Note [a]		20		mA
$I_{DDS-SCCB}$	Standby Current	See Note [b]		1		mA
$I_{DDS-PWDN}$	Standby Current			10	20	µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [c]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output Leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-A} = 2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 2.5V
$I_{DDA} = \Sigma\{I_{DD-IO} + I_{DD-C} + I_{DD-A}\}$, f_{CLK} = 24MHz at 7.5 fps YUV output, no I/O loading

b. V_{DD-A} = 2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 2.5V
$I_{DDS-SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS-PWDN}$ refers to a PWDN pin-initiated Standby

c. Standard Output Loading = 25pF, 1.2KΩ

Table 6 Functional and AC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			18	dB
	Red/Blue Adjustment Range		12		dB
Inputs (PWDN, CLK, RESET)					
f_{CLK}	Input Clock Frequency	10	24	48	MHz
t_{CLK}	Input Clock Period	21	42	100	ns
$t_{CLK:DC}$	Clock Duty Cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB Timing (see Figure 4)					
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and Y[9:0] (see Figure 5, Figure 6, Figure 7, Figure 8, Figure 10, and Figure 11)					
t_{PDV}	PCLK[↓] to Data-out Valid			5	ns
t_{SU}	Y[9:0] Setup time	15			ns
t_{HD}	Y[9:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	• V_{DD}: V_{DD-C} = 1.8V, V_{DD-A} = 2.5V, V_{DD-IO} = 2.5V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 2.5V • f_{CLK}: 24MHz				

Timing Specifications

Figure 4 SCCB Timing Diagram

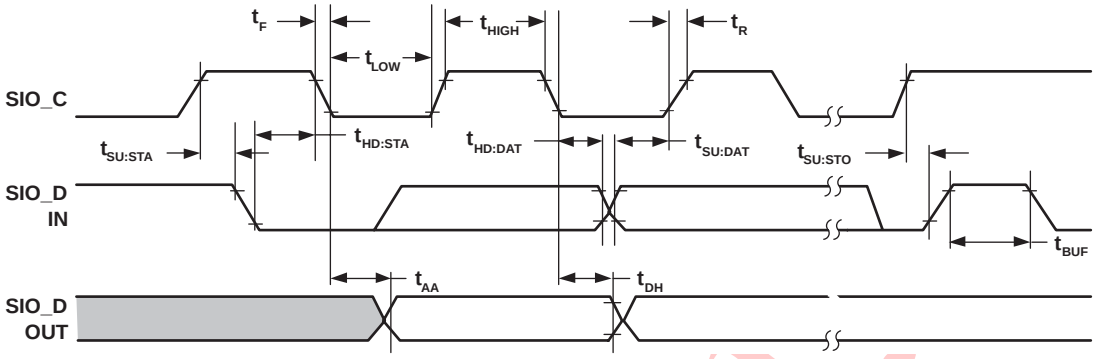


Figure 5 Horizontal Timing

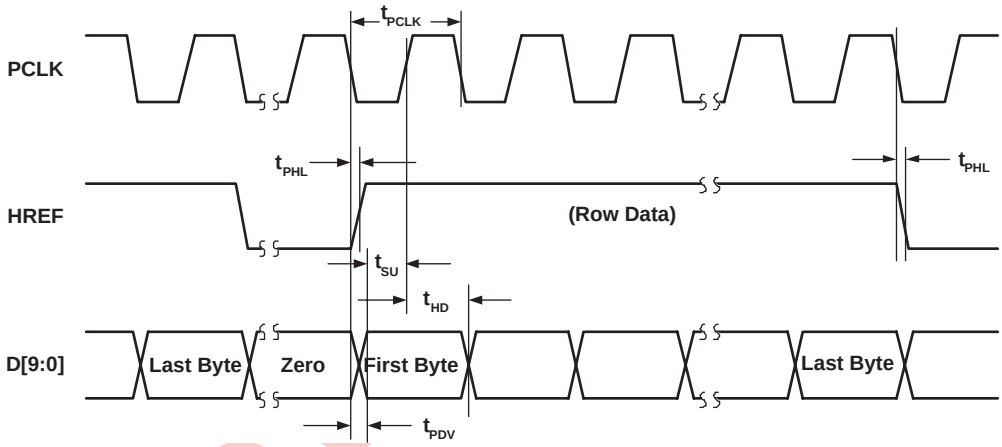
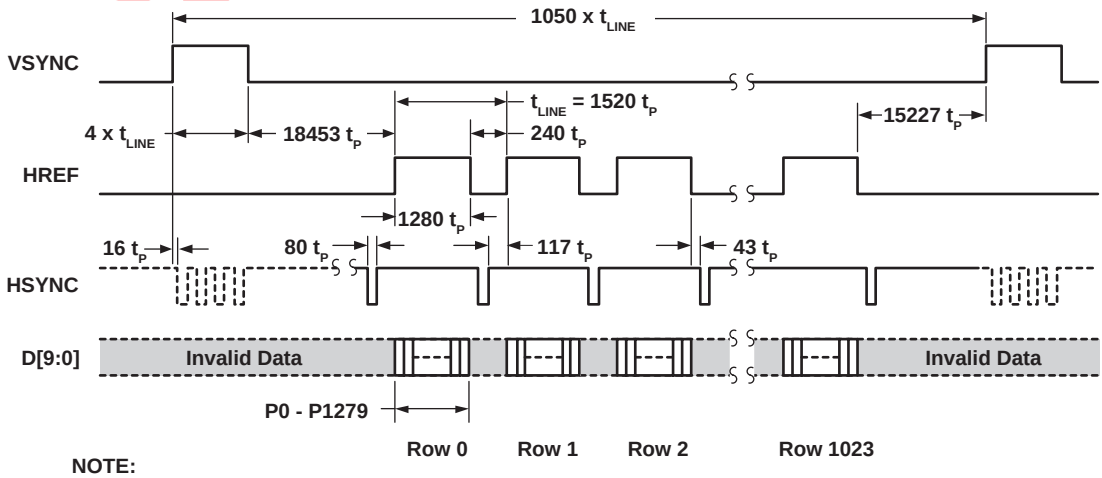
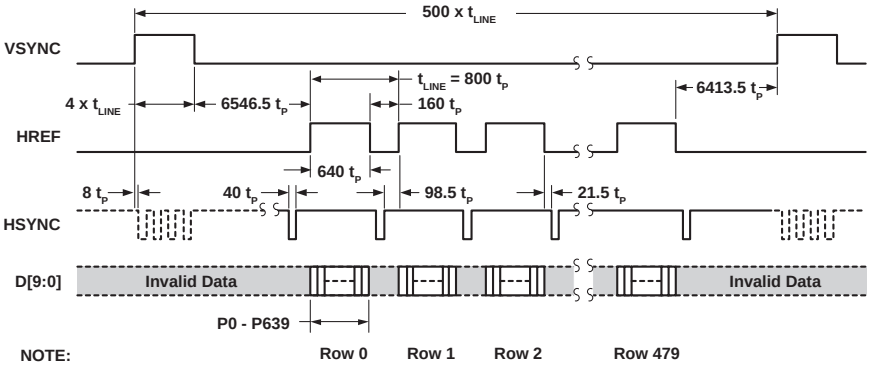


Figure 6 SXGA Frame Timing



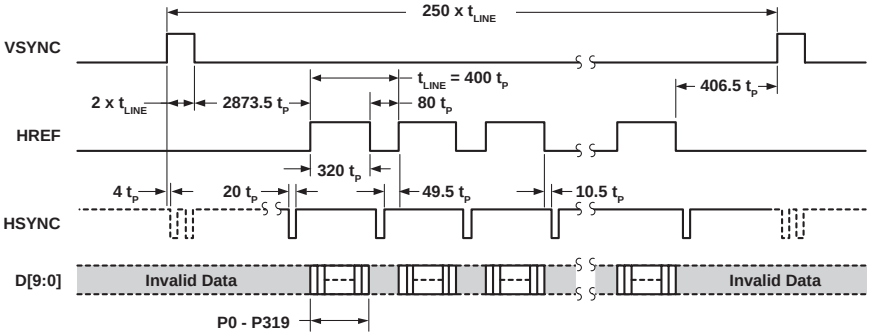
NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x internal pixel clock

Figure 7 VGA Frame Timing



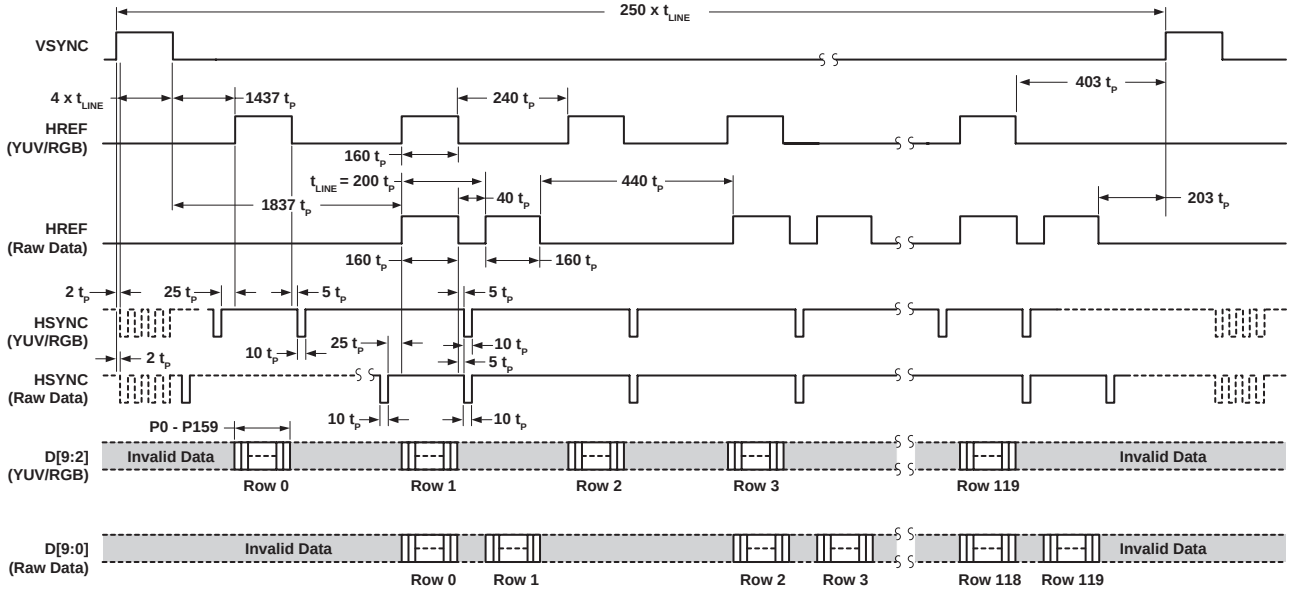
NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x internal pixel clock

Figure 8 QVGA Frame Timing



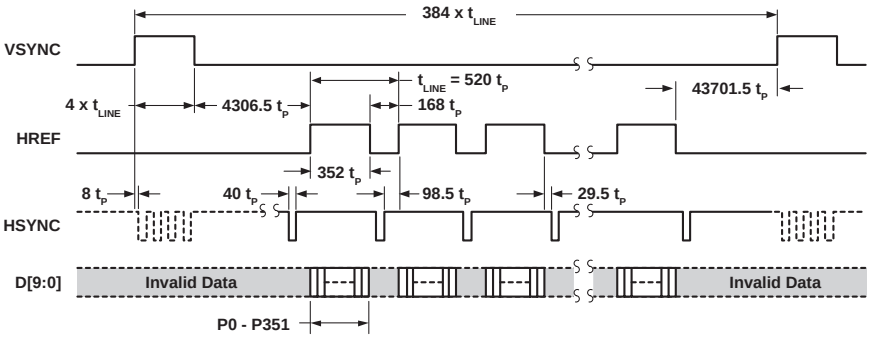
NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x internal pixel clock

Figure 9 QQVGA Frame Timing



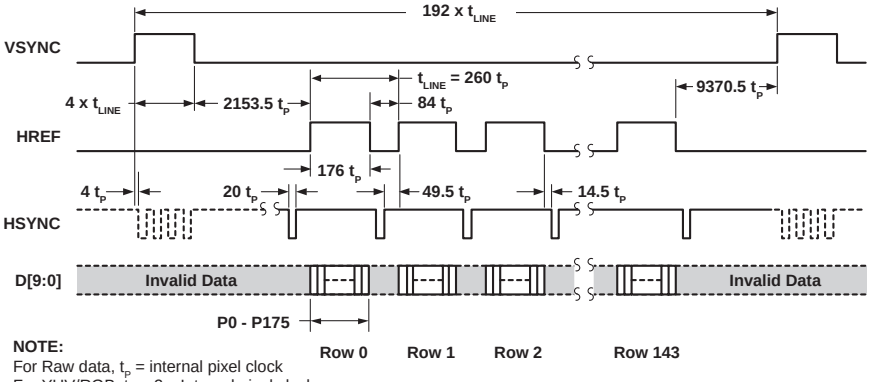
NOTE:
For YUV/RGB, $t_P = 2 \times t_{PCLK}$
For Raw data, $t_P = t_{PCLK}$

Figure 10 CIF Frame Timing



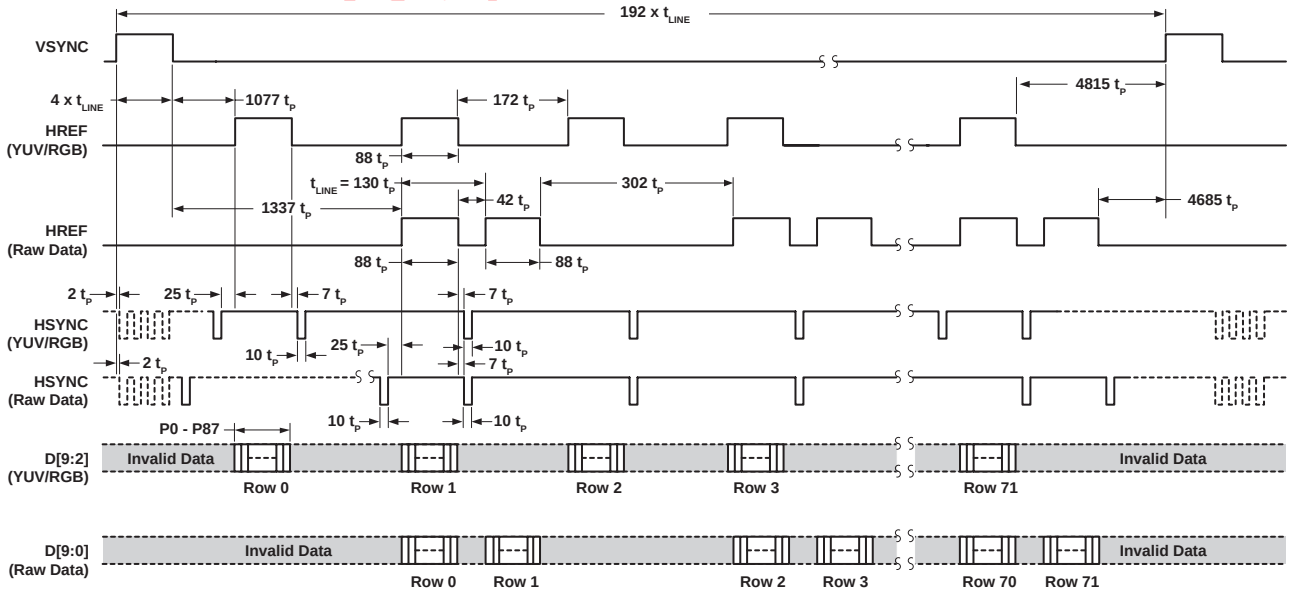
NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x internal pixel clock

Figure 11 QCIF Frame Timing



NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x Internal pixel clock

Figure 12 QQCIF Frame Timing



NOTE:
For YUV/RGB, $t_P = 2 \times t_{PCLK}$
For Raw data, $t_P = t_{PCLK}$

Figure 13 RGB 565 Output Timing Diagram

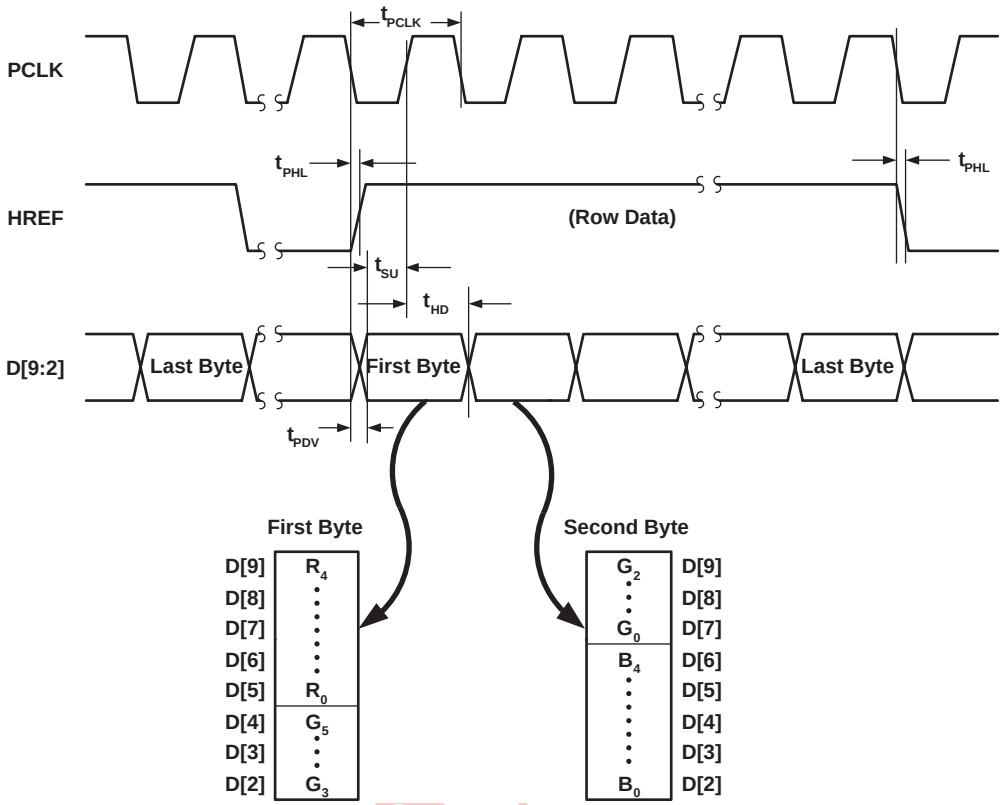
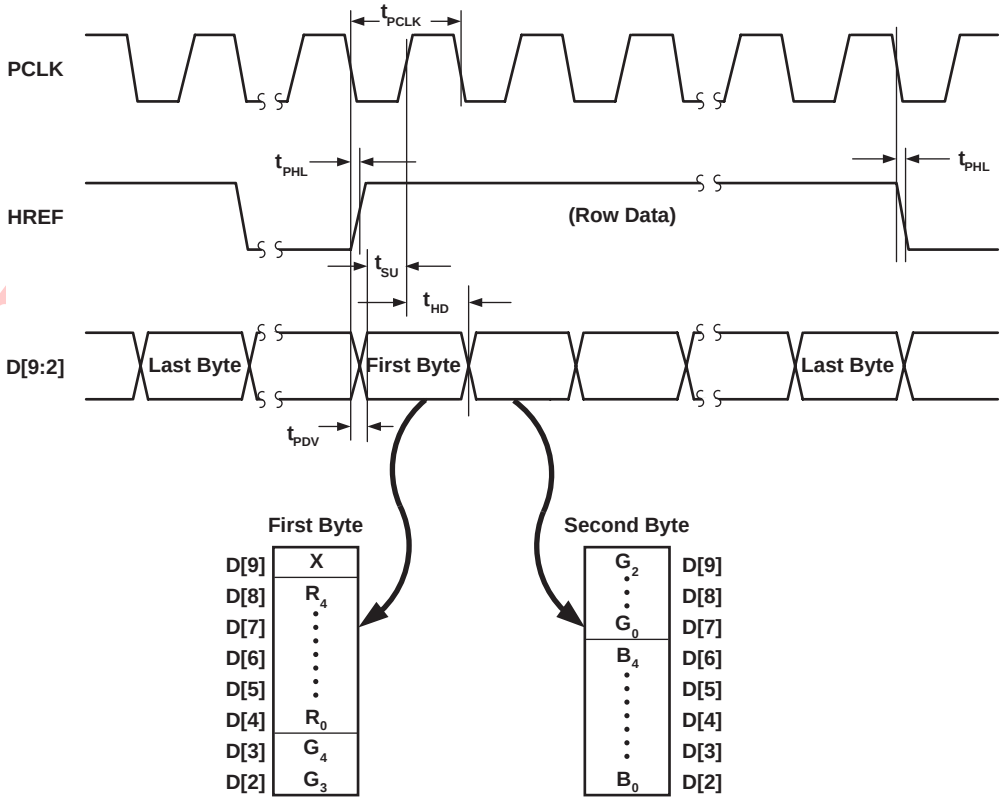


Figure 14 RGB 555 Output Timing Diagram



Register Set

Table 7 provides a list and description of the Device Control registers. The device slave addresses for the OV9650FSL are 60 for write and 61 for read.

Table 7 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC[7:0] – Gain control gain setting • Range: [00] to [FF]
01	BLUE	80	RW	AWB – Blue channel gain setting • Range: [00] to [FF]
02	RED	80	RW	AWB – Red channel gain setting • Range: [00] to [FF]
03	VREF	12	RW	Vertical Frame Control Bit[7:6]: AGC[9:8] (see register GAIN for AGC[7:0]) Bit[5:3]: VREF end low 3 bits (high 8 bits at VSTOP[7:0] Bit[2:0]: VREF start low 3 bits (high 8 bits at VSTRT[7:0]
04	COM1	00	RW	Common Control 1 Bit[7]: Reserved Bit[6]: CCIR656 format Bit[5]: QQVGA or QQCIF format. Effective only when QVGA (register bit COM7[4]) or QCIF (register bit COM7[3]) output is selected and related HREF skip option based on format is selected (register COM1[3:2]) Bit[4]: Reserved Bit[3:2]: HREF skip option 00: No skip 01: YUV/RGB skip every other row for YUV/RGB, skip 2 rows for every 4 rows for Raw data 1x: Skip 3 rows for every 4 rows for YUV/RGB, skip 6 rows for every 8 rows for Raw data Bit[1:0]: AEC low 2 LSB (see registers AECHM for AEC[15:10] and AECH for AEC[9:2])
05	BAVE	00	RW	U/B Average Level Automatically updated based on chip output format
06	GEAVE	00	RW	Y/Ge Average Level Automatically updated based on chip output format
07	RSVD	00	–	Reserved
08	RAVE	00	RW	V/R Average Level Automatically updated based on chip output format

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
09	COM2	01	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Soft sleep mode Bit[3:2]: Reserved Bit[1:0]: Output drive capability 00: 1x 01: 2x 10: 2x 11: 4x
0A	PID	96	R	Product ID Number MSB (Read only)
0B	VER	52	R	Product ID Number LSB (Read only)
0C	COM3	00	RW	Common Control 3 Bit[7]: Reserved Bit[6]: Output data MSB and LSB swap Bit[5:4]: Reserved Bit[3]: Pin selection 1: Change RESET pin to EXPST_B (frame exposure mode timing) and change PWDN pin to FREX (frame exposure enable) Bit[2]: VarioPixel® for VGA, CIF, QVGA, QCIF, QQVGA, and QQCIF Bit[1]: Reserved Bit[0]: Single frame output (used for Frame Exposure mode only)
0D	COM4	00	RW	Common Control 4 Bit[7]: VarioPixel® for QVGA, QCIF, QQVGA, and QQCIF Bit[6:3]: Reserved Bit[2]: Tri-state option for output clock at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[1]: Tri-state option for output data at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[0]: Reserved
0E	COM5	01	RW	Common Control 5 Bit[7]: System clock selection. If the system clock is 48 MHz, this bit should be set to high to get 15 fps for YUV or RGB Bit[6:5]: Reserved Bit[4]: Slam mode enable 0: Master mode 1: Slam mode (used for slave mode) Bit[3:0]: Reserved

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0F	COM6	43	RW	Common Control 6 Bit[7]: Output of optical black line option 0: Disable HREF at optical black 1: Enable HREF at optical black Bit[6:4]: Reserved Bit[3]: Enable bias for ADBLC Bit[2]: ADBLC offset 0: Use 4-channel ADBLC 1: Use 2-channel ADBLC Bit[1]: Reset all timing when format changes Bit[0]: Enable ADBLC option
10	AECH	40	RW	Exposure Value Bit[7:0]: AEC[9:2] (see registers AECHM for AEC[15:10] and COM1 for AEC[1:0])
11	CLKRC	00	RW	Data Format and Internal Clock Bit[7]: Digital PLL option 0: Disable double clock option, meaning the maximum PCLK can be as high as half input clock 1: Enable double clock option, meaning the maximum PCLK can be as high as input clock Bit[6]: Use input clock directly (no clock pre-scale available) Bit[5:0]: Internal clock pre-scalar F(internal clock) = F(input clock)/(Bit[5:0]+1) • Range: [0 0000] to [1 1111]
12	COM7	00	RW	Common Control 7 Bit[7]: SCCB Register Reset 0: No change 1: Resets all registers to default values Bit[6]: Output format - VGA selection Bit[5]: Output format - CIF selection Bit[4]: Output format - QVGA selection Bit[3]: Output format - QCIF selection Bit[2]: Output format - RGB selection Bit[1]: Reserved Bit[0]: Output format - Raw RGB (COM7[2] must be set high)
13	COM8	8F	RW	Common Control 8 Bit[7]: Enable fast AGC/AEC algorithm Bit[6]: AEC - Step size limit 0: Fast condition change maximum step is VSYNC 1: Unlimited step size Bit[5]: Banding filter ON/OFF Bit[4:3]: Reserved Bit[2]: AGC Enable Bit[1]: AWB Enable Bit[0]: AEC Enable

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
14	COM9	4A	RW	Common Control 9 Bit[7]: Reserved Bit[6:4]: Automatic Gain Ceiling - maximum AGC value 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x Bit[3]: Exposure timing can be less than limit of banding filter when light is too strong Bit[2]: Data format - VSYNC drop option 0: VSYNC always exists 1: VSYNC will drop when frame data drops Bit[1]: Enable drop frame when AEC step is larger than the Exposure Gap Bit[0]: Freeze AGC/AEC
15	COM10	00	RW	Common Control 10 Bit[7]: Set pin definition 1: Set RESET to SLHS (slave mode horizontal sync) and set PWDN to SLVS (slave mode vertical sync) Bit[6]: HREF changes to HSYNC Bit[5]: PCLK output option 0: PCLK always output 1: No PCLK output when HREF is low Bit[4]: PCLK reverse Bit[3]: HREF reverse Bit[2]: Reset signal end point option Bit[1]: VSYNC negative Bit[0]: HSYNC negative
16	RSVD	00	–	Reserved
17	HSTART	1A	RW	Output Format - Horizontal Frame (HREF column) start high 8-bit (low 3 bits are at HREF[2:0])
18	HSTOP	BA	RW	Output Format - Horizontal Frame (HREF column) end high 8-bit (low 3 bits are at HREF[5:3])
19	VSTRT	01	RW	Output Format - Vertical Frame (row) start high 8-bit (low 3 bits are at VREF[2:0])
1A	VSTOP	81	RW	Output Format - Vertical Frame (row) end high 8-bit (low 3 bits are at VREF[5:3])
1B	PSHFT	00	RW	Data Format - Pixel Delay Select (delays timing of the Y[9:0] data relative to HREF in pixel units) • Range: [00] (no delay) to [FF] (256 pixel delay which accounts for whole array)
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	MVFP	00	RW	Mirror/VFlip Enable Bit[7:6]: Reserved Bit[5]: Mirror 0: Normal image 1: Mirror image Bit[4]: VFlip enable 0: VFlip disable 1: VFlip enable Bit[3:0]: Reserved
1F	LAEC	00	RW	Reserved
20	BOS	80	RW	B Channel ADBLC Result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
21	GBOS	80	RW	Gb channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
22	GROS	80	RW	Gr channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
23	ROS	80	RW	R channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
24	AEW	78	RW	AGC/AEC - Stable Operating Region (Upper Limit)
25	AEB	68	RW	AGC/AEC - Stable Operating Region (Lower Limit)
26	VPT	D4	RW	AGC/AEC Fast Mode Operating Region Bit[7:4]: High nibble of upper limit Bit[3:0]: High nibble of lower limit
27	BBIAS	80	RW	B Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
28	GbBIAS	80	RW	Gb Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
29	Gr_COM	00	RW	Analog BLC and Regulator Control Bit[7:6]: Reserved Bit[5]: Bypass Analog BLC Bit[4]: Bypass regulator Bit[3:0]: Reserved
2A	EXHCH	00	RW	Dummy Pixel Insert MSB Bit[7]: Reserved Bit[6:4]: 3 MSB for dummy pixel insert in horizontal direction Bit[3:2]: HSYNC falling edge delay 2 MSB Bit[1:0]: HSYNC rising edge delay 2 MSB
2B	EXHCL	00	RW	Dummy Pixel Insert LSB 8 LSB for dummy pixel insert in horizontal direction
2C	RBIAS	80	RW	R Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
2D	ADVFL	00	RW	LSB of insert dummy lines in vertical direction (1 bit equals 1 line)
2E	ADVFH	00	RW	MSB of insert dummy lines in vertical direction
2F	YAVE	00	RW	Y/G Channel Average Value
30	HSYST	08	RW	HSYNC Rising Edge Delay (low 8 bits)
31	HSYEN	30	RW	HSYNC Falling Edge Delay (low 8 bits)
32	HREF	A4	RW	HREF Control Bit[7:6]: HREF edge offset to data output Bit[5:3]: HREF end 3 LSB (high 8 MSB at register HSTOP) Bit[2:0]: HREF start 3 LSB (high 8 MSB at register HSTART)
33	CHLF	00	RW	Bit[7:0]: Reserved
34	ARBLM	03	RW	Bit[7:0]: Reserved
35-36	RSVD	XX	–	Reserved
37	ADC	04	RW	Bit[7:0]: Reserved
38	ACOM	12	RW	Bit[7:0]: Reserved
39	OFON	00	RW	Bit[7:4]: Reserved Bit[3]: Line buffer power down - must be set to "1" before chip power down Bit[2:0]: Reserved

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3A	TSLB	0C	RW	Line Buffer Test Option Bit[7:6]: Reserved Bit[5]: Bit-wise reverse Bit[4]: UV output value 0: Use normal UV output 1: Use fixed UV value set in registers MANU and MANV as UV output instead of chip output Bit[3:2]: Output sequence is Y U Y V instead of U Y V Y 00: Y U Y V 01: Y V Y U 10: V Y U Y 11: U Y V Y Bit[1]: Reserved Bit[0]: Digital BLC enable 0: Disable 1: Enable
3B	COM11	00	RW	Common Control 11 Bit[7]: Night mode 0: Night mode disable 1: Night mode enable - If the AGC gain goes over 2, then AGC gain drops to 0 and frame rate changes by half. COM11[6:5] limits the minimum frame rate. Also, ADVFH and ADVFL will be automatically updated. Bit[6:5]: Night mode insert frame option 00: Normal frame rate 01: 1/2 frame rate 10: 1/4 frame rate 11: 1/8 frame rate Bit[4:3]: Average calculation window option 00: Use full frame 01: Use half frame 10: Use quarter frame 11: Not allowed Bit[2:1]: Reserved Bit[0]: Manual banding filter mode
3C	COM12	40	RW	Common Control 12 Bit[7]: HREF option 0: No HREF when VREF is low 1: Always has HREF Bit[6:3]: Reserved Bit[2]: Enable UV average Bit[1:0]: Reserved

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3D	COM13	99	RW	Common Control 13 Bit[7:6]: Gamma selection for signal 00: No gamma function 01: Gamma used for Y channel only 10: Gamma used for Raw data before interpolation 11: Not allowed Bit[5]: Reserved Bit[4]: Enable color matrix for RGB or YUV Bit[3]: Enable Y channel delay option 0: Delay UV channel 1: Delay Y channel Bit[2:0]: Output Y/UV delay
3E	COM14	0E	RW	Common Control 14 Bit[7:2]: Reserved Bit[1]: Enable edge enhancement for YUV output (effective only for YUV/RGB, no use for Raw data) Bit[0]: Edge enhancement option 0: Edge enhancement factor = EDGE[3:0] 1: Edge enhancement factor = 2 x EDGE[3:0]
3F	EDGE	88	RW	Edge Enhancement Adjustment Bit[7:4]: Edge enhancement threshold[3:0] (see register COM22[7:6} for Edge threshold[5:4]) Bit[3:0]: Edge enhancement factor
40	COM15	C0	RW	Common Control 15 Bit[7:6]: Data format - output full range enable 0x: Output range: [10] to [F0] 10: Output range: [01] to [FE] 11: Output range: [00] to [FF] Bit[5:4]: RGB 555/565 option (must set COM7[2] high) x0: Normal RGB output 01: RGB 565 11: RGB 555 Bit[3]: Swap R/B in RGB565/RGB555 format Bit[2:0]: Reserved
41	COM16	10	RW	Common Control 16 Bit[7:2]: Reserved Bit[1]: Color matrix coefficient double option Bit[0]: Reserved
42	COM17	08	RW	Common Control 17 Bit[7:5]: Reserved Bit[4]: Edge enhancement option Bit[3]: Reserved Bit[2]: Select single frame out Bit[1]: Tri-state output after single frame out Bit[0]: Reserved

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
43-4E	RSVD	XX	–	Reserved
4F	MTX1	58	RW	Matrix Coefficient 1
50	MTX2	48	RW	Matrix Coefficient 2
51	MTX3	10	RW	Matrix Coefficient 3
52	MTX4	28	RW	Matrix Coefficient 4
53	MTX5	48	RW	Matrix Coefficient 5
54	MTX6	70	RW	Matrix Coefficient 6
55	MTX7	40	RW	Matrix Coefficient 7
56	MTX8	40	RW	Matrix Coefficient 8
57	MTX9	40	RW	Matrix Coefficient 9
58	MTXS	0F	RW	Matrix Coefficient Sign for coefficient 9 to 2 0: Plus 1: Minus
59-61	RSVD	XX	–	Reserved
62	LCC1	00	RW	Lens Correction Option 1
63	LCC2	00	RW	Lens Correction Option 2
64	LCC3	10	RW	Lens Correction Option 3
65	LCC4	80	RW	Lens Correction Option 4
66	LCC5	00	RW	Lens Correction Control
67	MANU	80	RW	Manual U Value (effective only when register TSLB[4] is high)
68	MANV	80	RW	Manual V Value (effective only when register TSLB[4] is high)
69	HV	00	RW	Manual Banding Filter MSB Bit[7:1]: Reserved Bit[0]: Matrix coefficient 1 sign
6A	MBD	00	RW	Manual Banding Filter Value (effective only when COM11[0] is high).
6B	DBLV	0A	RW	Bit[7:0]: Reserved
6C-7B	GSP	XX	RW	Gamma curve
7C-8A	GST	XX	RW	Gamma curve
8B	COM21	04	RW	Common Control 21 Bit[7:0]: Reserved

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
8C	COM22	00	RW	Common Control 22 Bit[7:6]: Edge enhancement threshold[5:4] (see register EDGE[7:4} for Edge threshold[3:0]) Bit[5]: De-noise enable Bit[4:2]: Reserved Bit[1]: White-pixel erase enable Bit[0]: White-pixel erase option
8D	COM23	00	RW	Common Control 23 Bit[7:5]: Reserved Bit[4]: Color bar test mode Bit[3:2]: Reserved Bit[1]: Color gain option 0: Analog 1: Digital Bit[0]: Reserved
8E	COM24	00	RW	Common Control 24 Bit[7:0]: Reserved
8F	DBLC1	0F	RW	Digital BLC Offset Sign Bit[7:4]: Reserved Bit[3]: Digital BLC B offset sign Bit[2]: Digital BLC R offset sign Bit[1]: Digital BLC Gb offset sign Bit[0]: Digital BLC Gr offset sign
90	DBLC_B	00	RW	Digital BLC B Channel Offset Value Bit[7:0]: Digital BLC B channel offset value
91	DBLC_R	00	RW	Digital BLC R Channel Offset Value Bit[7:0]: Digital BLC R channel offset value
92	DM_LNL	00	RW	Dummy Line low 8 bits Bit[7:0]: Control insert Dummy line[7:0]
93	DM_LNH	00	RW	Dummy Line high 8 bits Bit[7:0]: Control insert Dummy line[15:8]
94-9C	RSVD	XX	–	Reserved
9D	LCCFB	00	RW	Lens Correction B Channel Control
9E	LCCFR	00	RW	Lens Correction R Channel Control
9F	DBLC_Gb	00	RW	Digital BLC Gb Channel Offset Value Bit[7:0]: Digital BLC Gb channel offset value
A0	DBLC_Gr	00	RW	Digital BLC Gr Channel Offset Value Bit[7:0]: Digital BLC Gr channel offset value

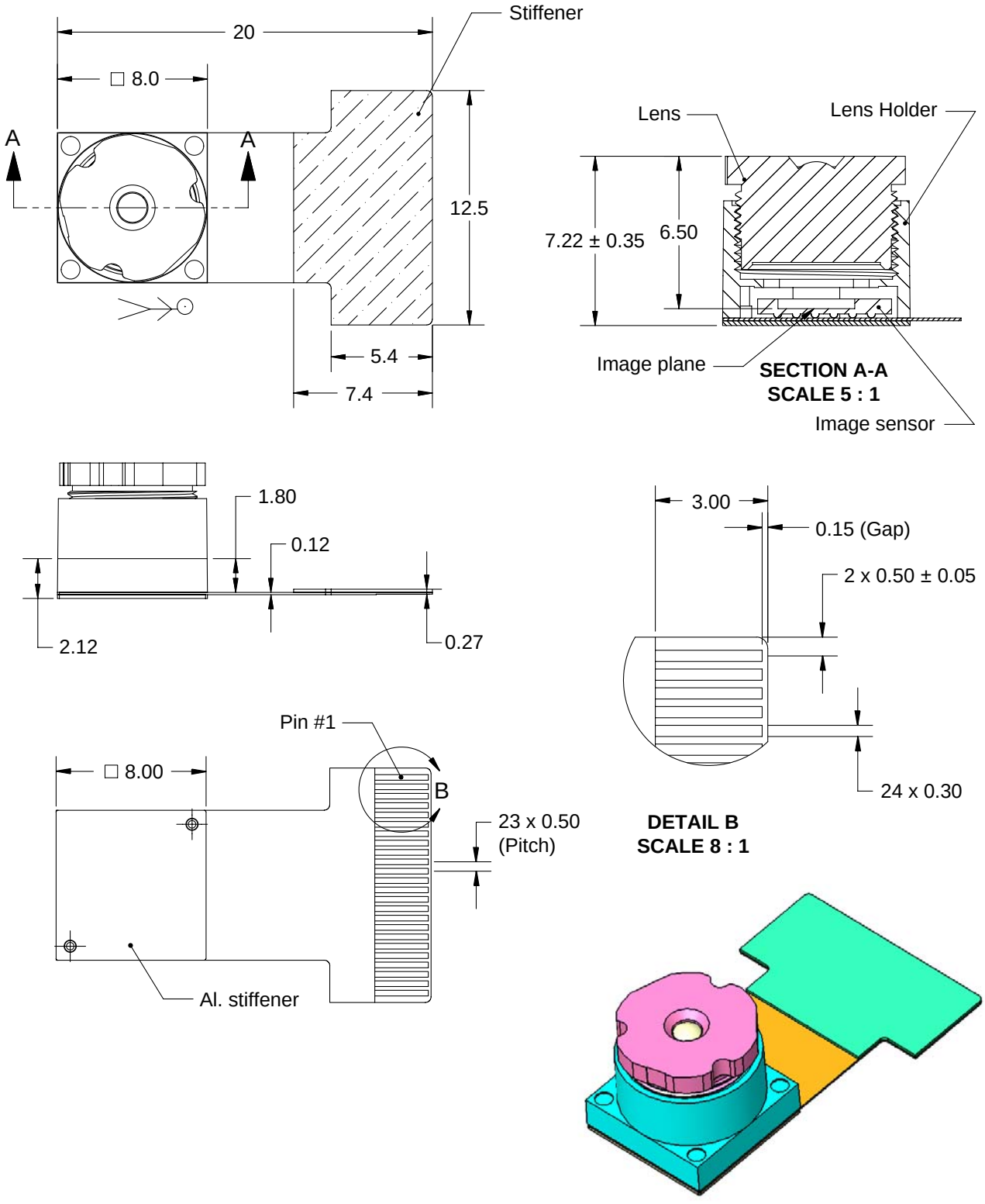
Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
A1	AECHM	40	RW	Exposure Value - AEC MSB 5 bits Bit[7:6]: Reserved Bit[5:0]: AEC[15:10] (see registers AECH for AEC[9:2] and COM1 for AEC[1:0])
A2-A3	RSVD	XX	–	Reserved
A4	COM25	00	RW	Common Control 25 Bit[7:0]: Reserved
A5	COM26	00	RW	Common Control 26 Bit[7:0]: Reserved
A6	G_GAIN	80	RW	Reserved
A7	VGA_ST	14	RW	Reserved
A8-AA	ACOM	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

Refer to Figure 15 for package information on the OV9650FSL module.

Figure 15 OV9650FSL Package Specifications



Mechanical Specifications

Table 8 Mechanical Dimensions

Parameter	Specification	Comments
Sensor	5.1 mm x 5.72 mm	CMOS in housing
Lens	Glass/Plastic	
Connection Type	24 x 0.5 mm	Flex cable
Housing	8 mm x 8 mm x 7.22 mm	Excluding mushroom

Connector Information

The OV9650FSL uses a 24-pin, 0.5 mm pitch flex cable connector. Table 9 shows a listing of some recommended connectors.

Table 9 Recommended Connectors

Manufacturer	Part No.	Description
Molex	52437-2427 (Bulk) 52437-2491 (Tape reel)	0.5 FPC connector, ZIF for SMT, R/A (bottom contact)

Optical Specifications

Table 10 Lens Specifications

Parameter	Specification	Comments
Lens Elements	Plastic	3-element
Viewing Angle	55.74° diagonal	
Focal Length	4.85 mm	
F Number	2.8	
Focus Range	40 cm → ∞	
Filter	IR cut	Included
Mount Description	M7 x 0.35P	
TV Distortion	<1%	
Focus Adjustment	Fixed	at 80 cm

Handling Precautions

WARNING: READ THIS FIRST!
Prior to handling any OmniVision flex camera module, read the following precautions.

- DO NOT try to open the unit enclosure as there is no user-serviceable component inside.
- To prevent damage to the camera module by electrostatic discharge, handle the camera module ONLY after discharging ALL static electricity from yourself and ensuring a static-free environment for the camera module.
- DO NOT touch the top surface of the lens.
- DO NOT press down on the lens.
- DO NOT try to focus the lens.
- DO NOT put the camera module in a dusty environment.
- To reduce the risk of electrical shock and damage to the camera module, turn OFF the power before connect and disconnect the camera module.
- DO NOT bend the flex cable in a sharp angle.
- DO NOT twist the flex cable.
- DO NOT peel the flex cable when you install and uninstall the camera module.
- DO NOT drop the camera module more than 60 cm onto any hard surface.
- To prevent fire or shock hazard, DO NOT expose camera module to rain or moisture.
- DO NOT expose camera module to direct sunlight.
- DO NOT put camera module in a high temperature environment.
- DO NOT use liquid or aerosol cleaners to clean the lens.
- DO NOT make any changes or modifications to camera module.
- DO NOT subject camera module to strong electromagnetic field.
- DO NOT subject the camera module to excessive vibration or shock.

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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REVISION CHANGE LIST

Document Title: OV9650FSL Flex Module Datasheet **Version:** 1.0

DESCRIPTION OF CHANGES

- Initial Release.

REVISION CHANGE LIST

Document Title: OV9650FSL Flex Module Datasheet **Version:** 1.1

DESCRIPTION OF CHANGES

The following changes were made to version 1.0:

- Changed pixel count from 1,270,096 to 1,310,720 (1280x1024) under Features on page 1.
- In Table 2 on page 3, changed Output Format specification from “1.3 MegaPixel (1280 x 1024 pixels)” to “SXGA (1280 x 1024 pixels)”

REVISION CHANGE LIST

Document Title: OV9650FSL Flex Module Datasheet **Version:** 1.2

DESCRIPTION OF CHANGES

The following changes were made to version 1.1:

- In the Key Specifications table on page 1, changed the I/O Power Supply specification from “2.5V to 3.3V“ to “2.5V to (V_{DD-A}+0.3V)”
- In Table 3 on page 4, changed Function/Description of pin 11 (DOVDD) from “Digital power supply (V_{DD-IO} = 2.5 to 3.3 VDC) for I/O’ to “Digital power supply for I/O (V_{DD-IO} = 2.5 to (V_{DD-A}+0.3V))”
- In Table 5 on page 5, changed Min parameter for DC supply voltage - I/O power (V_{DD-IO}) from “2.25V” to “2.5V”
- In Table 5 on page 5, changed Max parameter for DC supply voltage - I/O power (V_{DD-IO}) from “3.6V” to “V_{DD-A}+0.3V”
- In Table 5 on page 5, for Standby Current ($I_{DDS-PWDN}$), added Max parameter “20µA”
- In Table 5 on page 5, changed table footnote a from “...V_{DD-IO} = 3.0V” to “...V_{DD-IO} = 2.5V”
- In Table 5 on page 5, changed table footnote b from “...V_{DD-IO} = 3.0V” to “...V_{DD-IO} = 2.5V”
- In Table 6 on page 6, changed AC Conditions from “...V_{DD-IO} = 3.0V” to “...V_{DD-IO} = 2.5V” and from “Output Loading: 25pF, 1.2KΩ to 3V” to “Output Loading: 25pF, 1.2KΩ to 2.5V”
- In Figures 6-12, added timing relationship between HSYNC and rising edge of VSYNC
- In Figure 9, defined t_{LINE} = 200 t_P
- In Figure 12, defined t_{LINE} = 130 t_P
- In Figure 12, corrected changed 5 t_P to 7 t_P in three places
- In Figure 3 on page 2, changed line under Note from “DOVDD is 2.5V to 3.3V sensor digital IO power” to “DOVDD is 2.5V to (AVDD + 0.3V) sensor digital IO power”
- Replaced Table 7 with the register table in the most current OV9650 Datasheet (Table 5)

DESCRIPTION OF CHANGES (CONTINUED)

- Updated Figure 15 on page 22 including the following dimension changes:
  - Module height changed from 6.20±0.30 to 7.22±0.35
  - In Section A-A, dimension 5.48±0.22 changed to 6.50
  - In Side View, deleted dimension 4.67
  - In Side View, deleted (Gold Fingers) callout
- Under Features on page 1, changed bulleted item “8mm x 8mm x 6.20mm module size, flex cable” to “8mm x 8mm x 7.22mm module size, flex cable”
- Under Ordering Information on page 1, changed Package description from “8mm x 8mm x 6.20mm Flex Cable” to “8mm x 8mm x 7.22mm Flex Cable”
- Under Key Specifications on page 1, changed Package Dimensions specification from “8mm x 8mm x 6.20mm” to “8mm x 8mm x 7.22mm
- In Table 8 on page 23, changed Housing specification from “8 mm x 8 mm x 6.20 mm” to “8 mm x 8 mm x 7.22 mm”
- In Table 10 on page 23, changed Viewing Angle specification from “61.52° diagonal” to “55.74° diagonal”
- In Table 10 on page 23, changed Focal Length specification from “4.18” to “4.85”
- Under Key Specifications on page 1, changed Max. Exposure Interval specification from “1000 x t_{ROW}” to “1050 x t_{ROW}” as per current OV9650 Sensor Datasheet ver. 1.91
- Under Key Specifications on page 1, changed Dark Current specification from “30 mV/s” to “30 mV/s at 60°C” as per current OV9650 Sensor Datasheet ver. 1.91
- Under Functional Description, changed callout “XCLK” to “XVCLK1” in Figure 2 on page 3.

REVISION CHANGE LIST

Document Title: OV9650FSL Flex Module Datasheet **Version:** 1.3

DESCRIPTION OF CHANGES

The following changes were made to version 1.2:

- In Figure 15 on page 22, replaced ME drawing.
- In Figure 1 on page 1, corrected the shape of the flex module shown in the pinout drawing