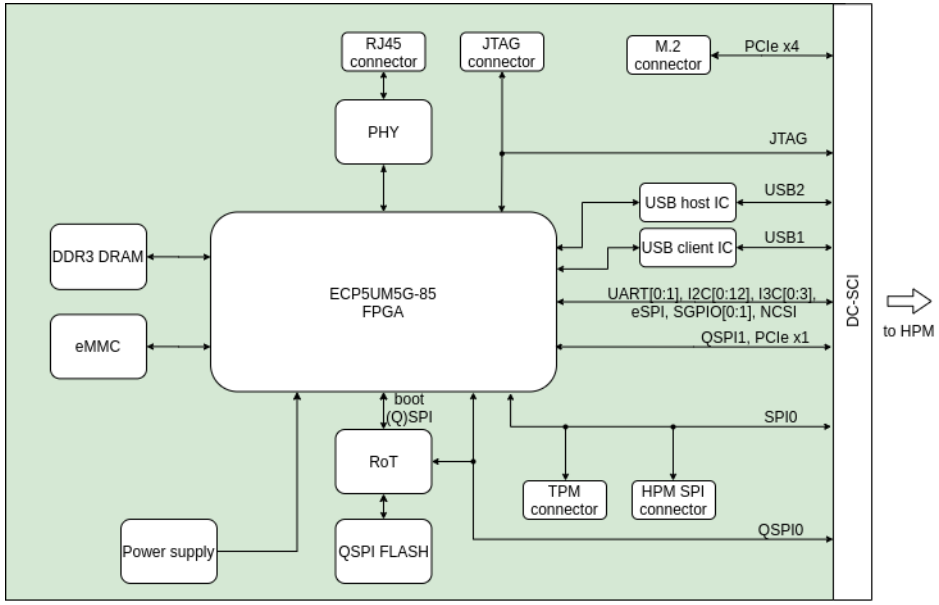
ECP5– Datacenter Secure Control Module (DC–SCM)



Sheet: Ethernet
File: ethernet.sch

Sheet: PCIe–connector
File: pcie–conn.sch

Sheet: RoT
File: rot.sch

Sheet: Edge connector
File: edge–connector.sch

Sheet: Interfaces
File: interfaces.sch

Sheet: DDR3
File: ddr3.sch

Sheet: Power supply
File: power–supply.sch

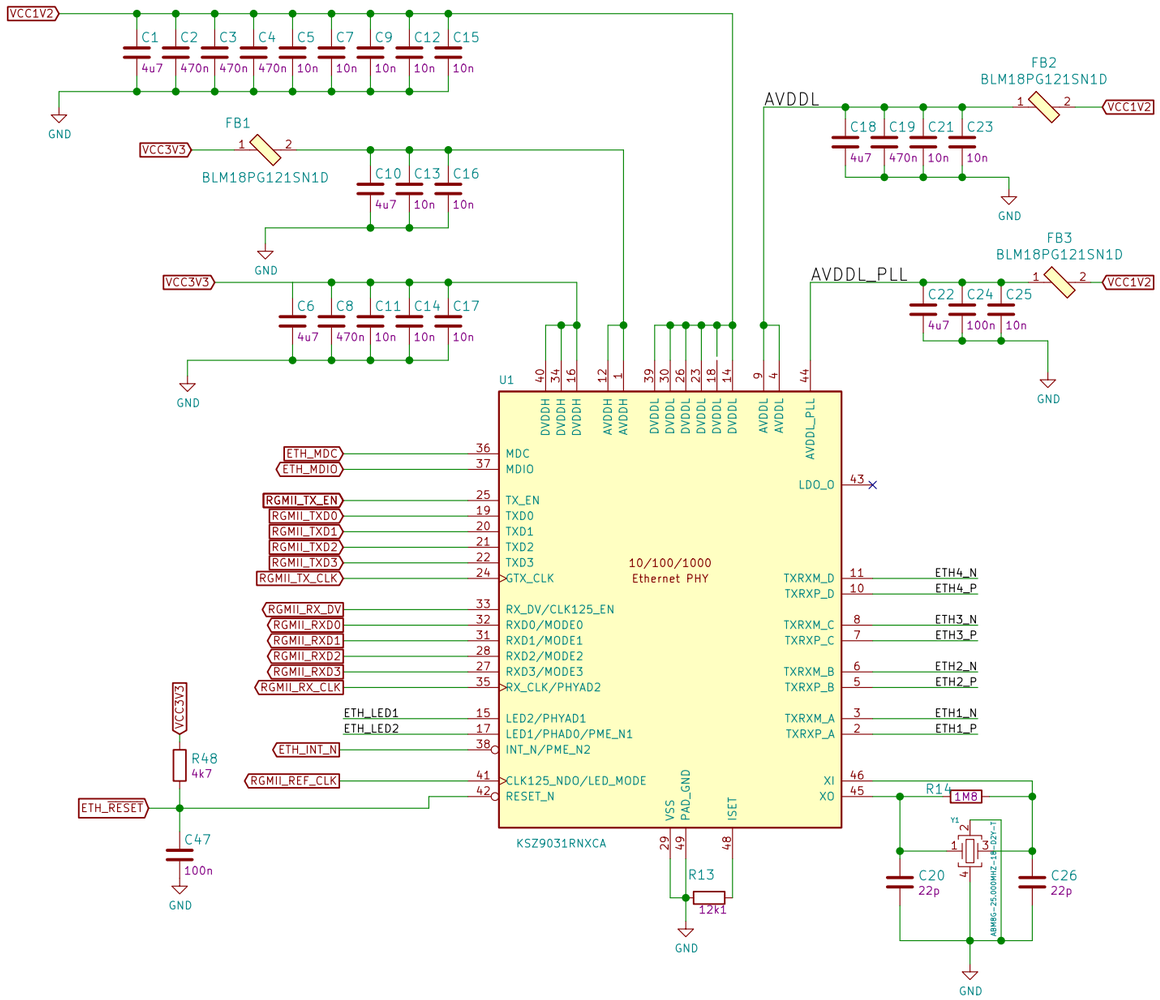
Sheet: FPGA power supply
File: fpga–power–supply.sch

Sheet: FPGA banks
File: fpga–banks.sch

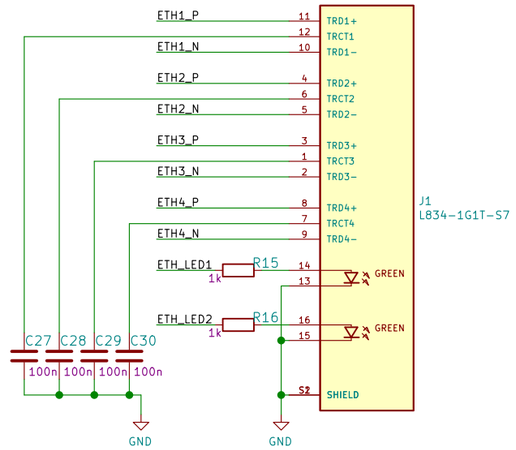
Sheet: /
File: ecp5–dc–scm.sch

Title: ECP5 – Datacenter Secure Control Module (DC–SCM)

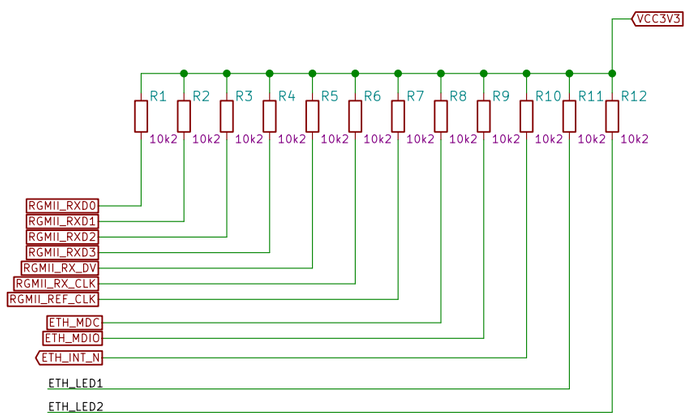
Size: A4	Date:	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1–2bpo10+1		Id: 1/10



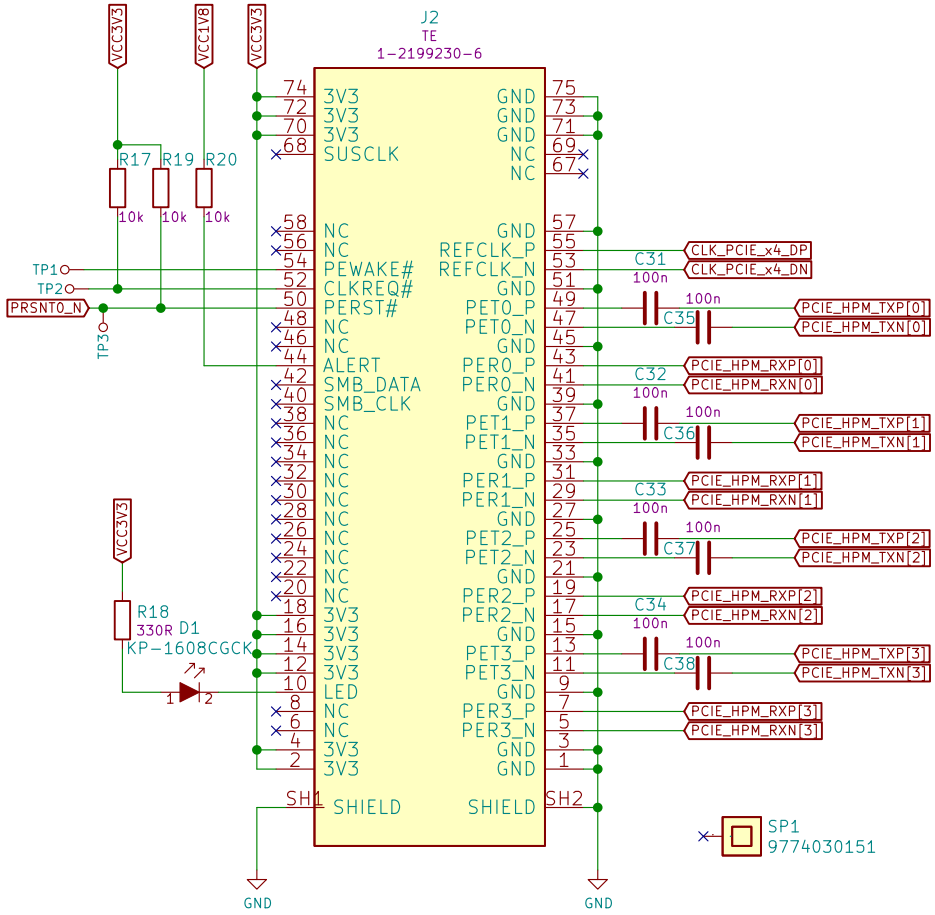
RJ45 connector



Pull up resistors



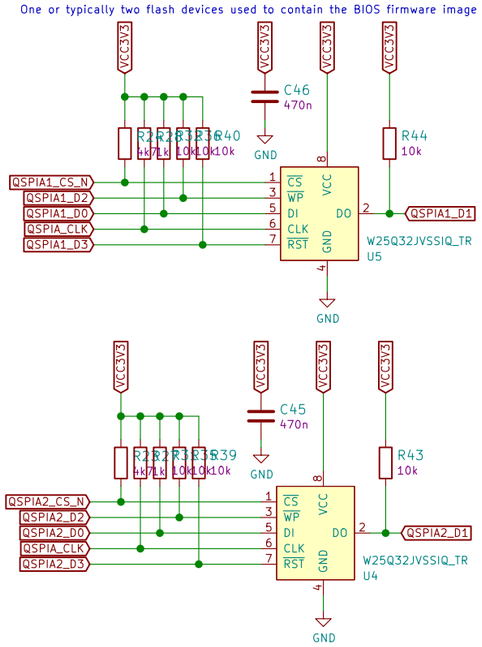
Sheet: /Ethernet/		
File: ethernet.sch		
Title: ECP5 – Datacenter Secure Control Module (DC-SCM)		
Size: A3	Date:	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 2/10



Sheet: /PCIe-connector/		
File: pcie-conn.sch		
Title: ECP5 – Datacenter Secure Control Module (DC-SCM)		
Size: A4	Date:	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 3/10

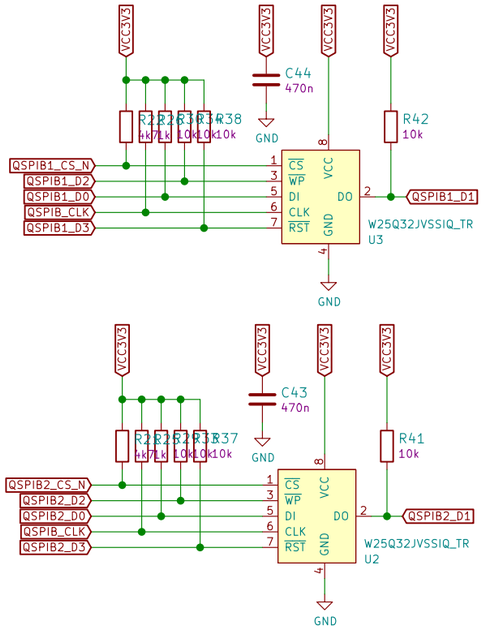
BIOS flash

One or typically two flash devices used to contain the BIOS firmware image

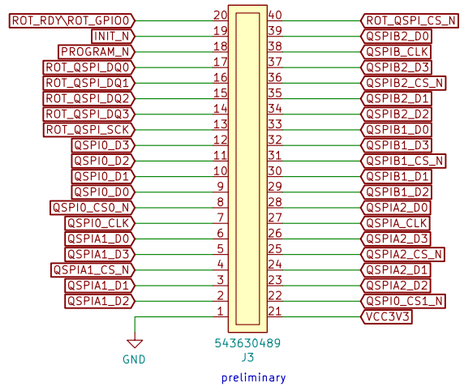


BMC flash

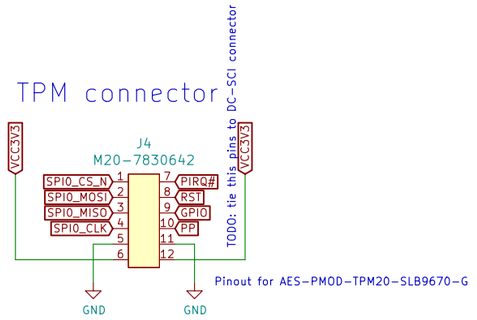
One or typically two flash devices used to contain the BMC firmware image



RoT connector

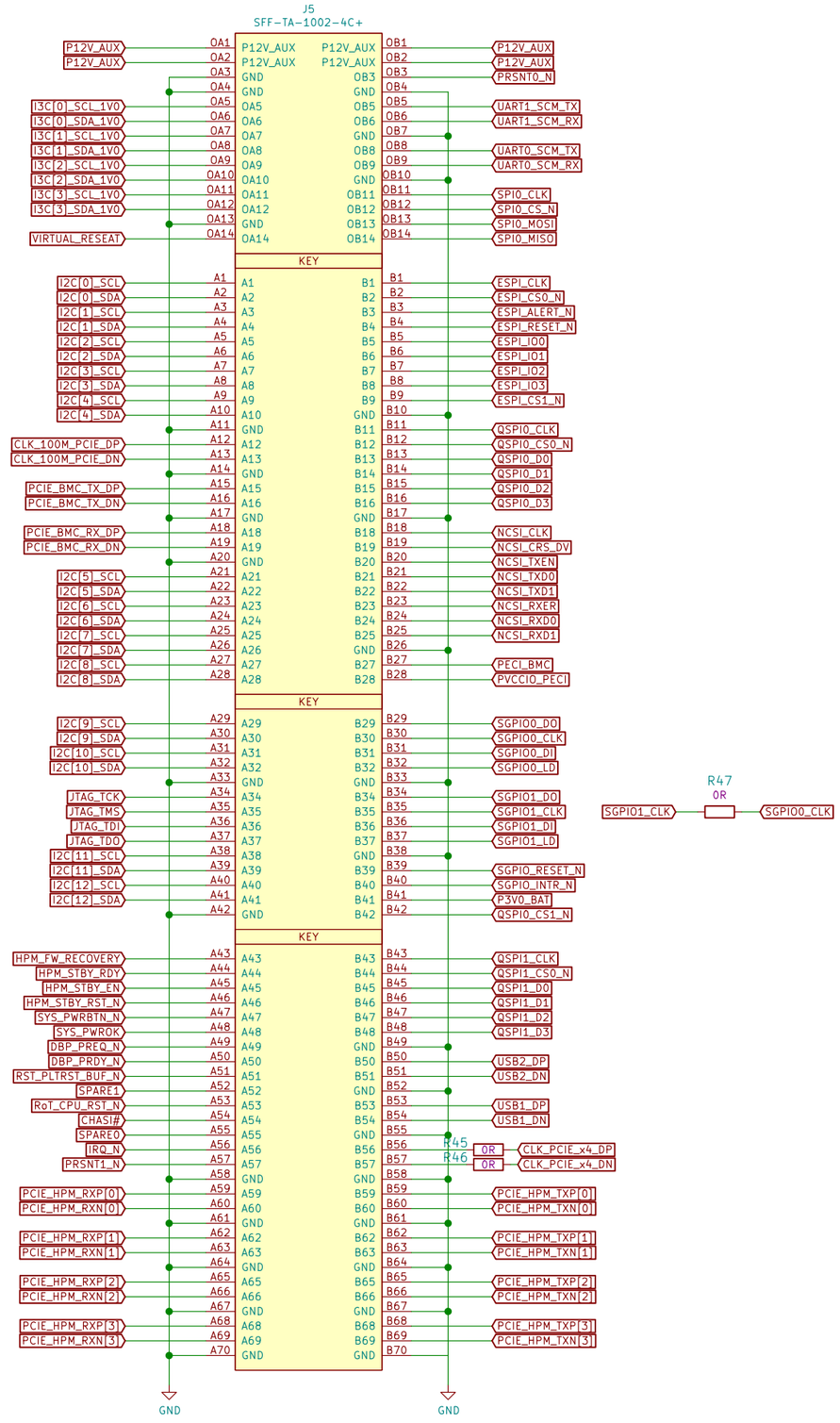


TPM connector



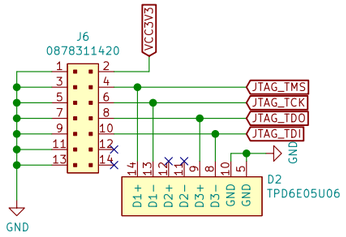
Sheet: /RoT/		
File: rot.sch		
Title: ECP5 – Datacenter Secure Control Module (DC-SCM)		
Size: A3	Date:	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 4/10

Edge connector



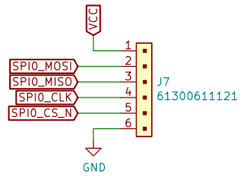
Sheet: /Edge connector/	
File: edge-connector.sch	
Title: ECP5 – Datacenter Secure Control Module (DC-SCM)	
Size: A3	Date:
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1	Id: 5/10
	Rev: 1.0.0

JTAG

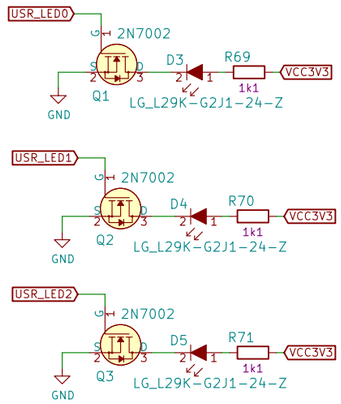


HPM SPI

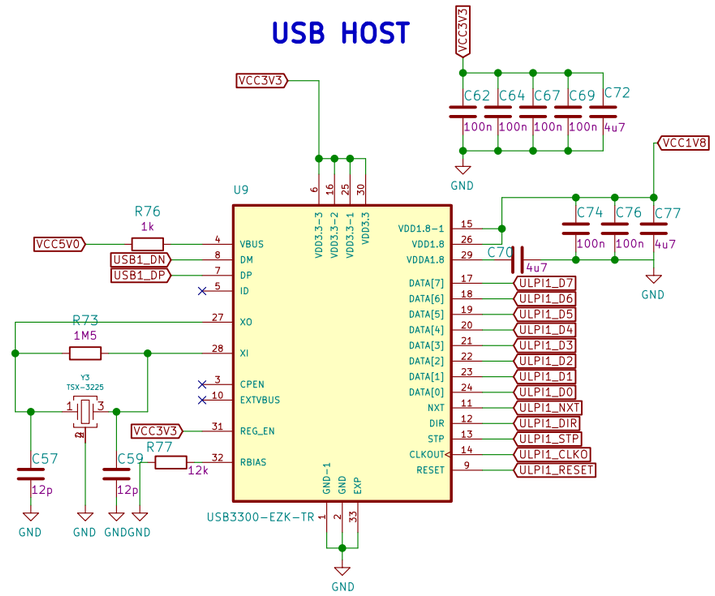
reserved for future use (as of DC-SCI OPC specification)



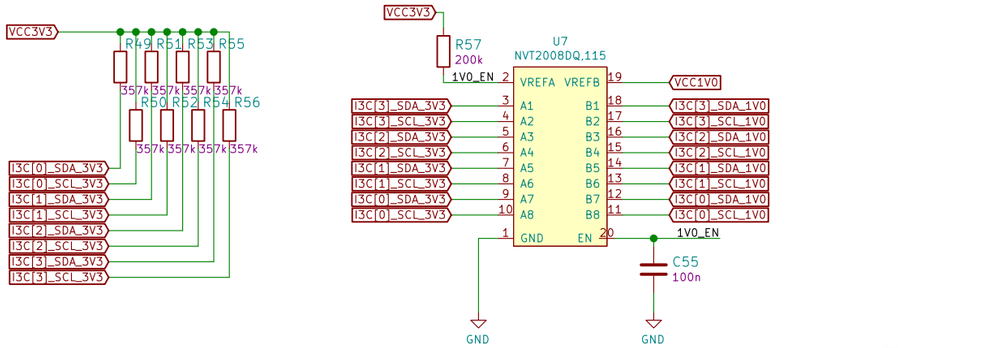
USER LEDs

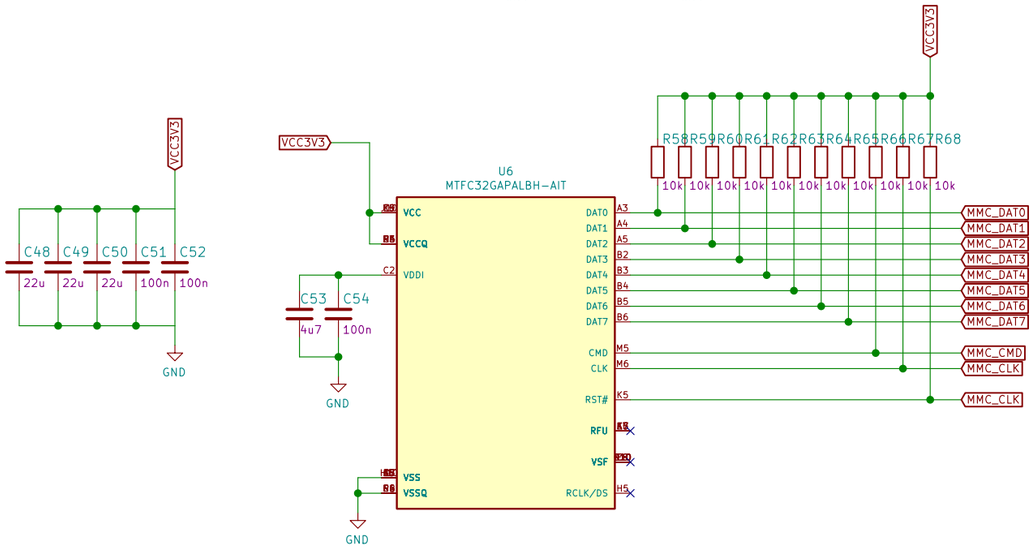


USB HOST

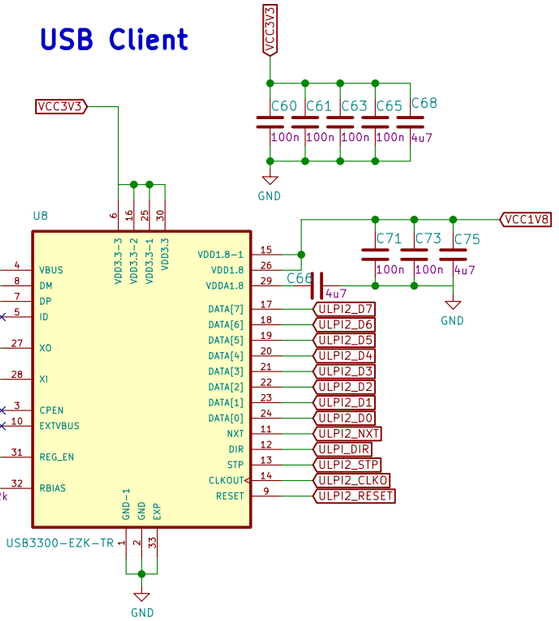


I3C voltage level translation





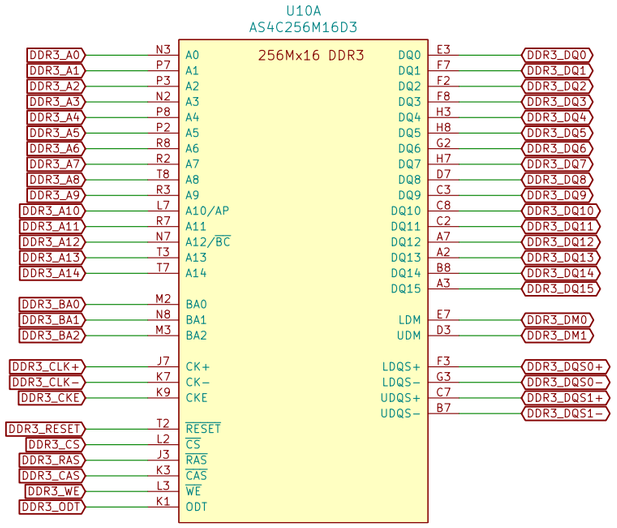
USB Client

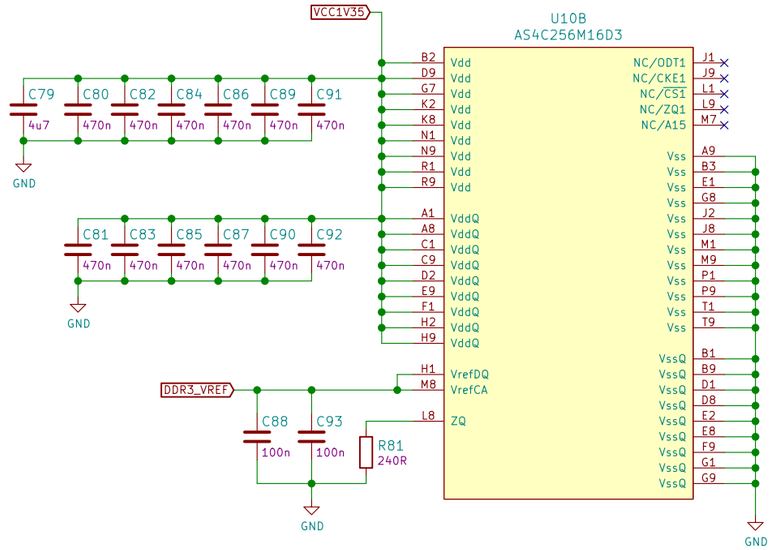


Sheet: /Interfaces/
File: interfaces.sch

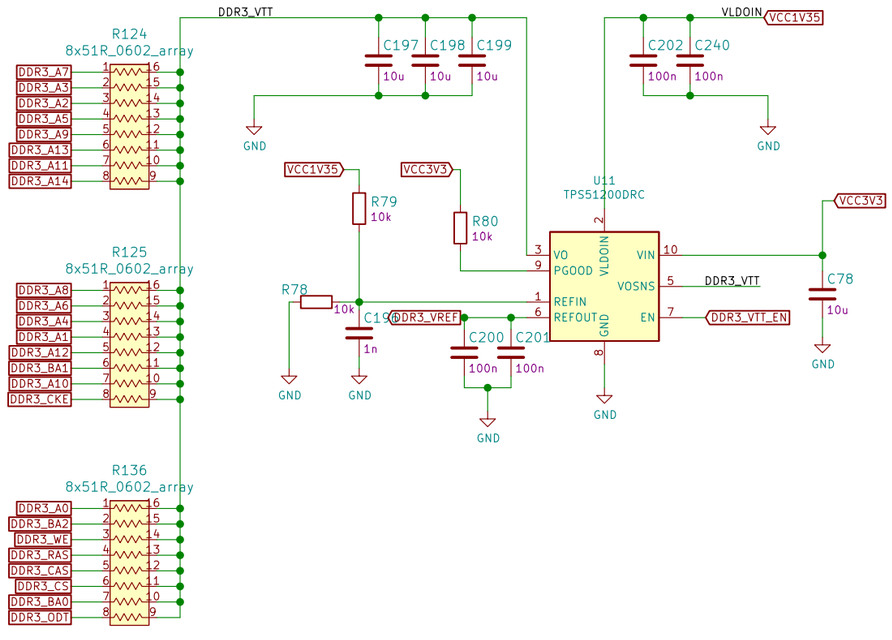
Title: ECP5 – Datacenter Secure Control Module (DC-SCM)

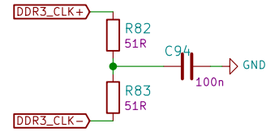
Size: A3	Date:	Rev: 1.0.0
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 6/10





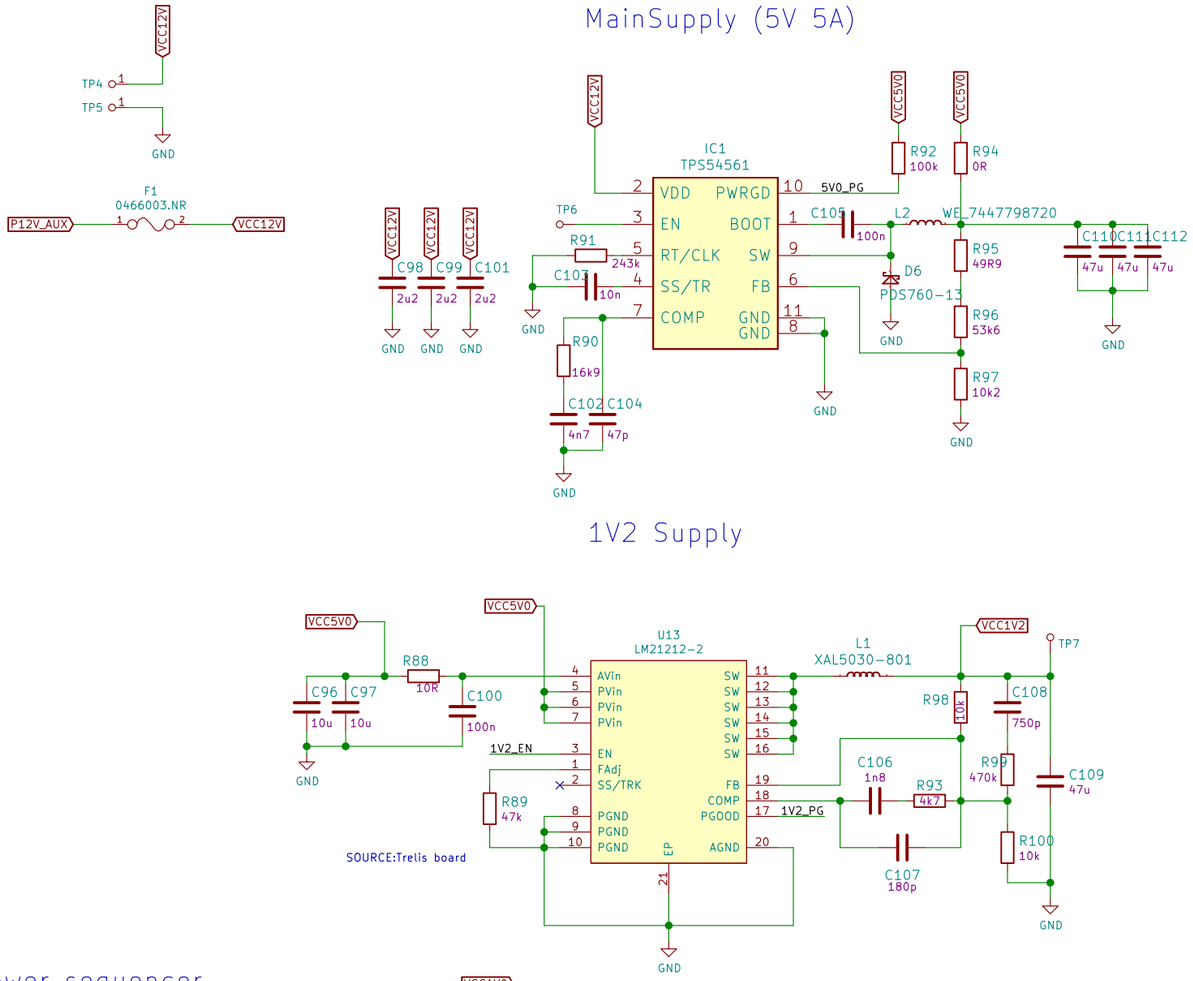
Source:Trellis board



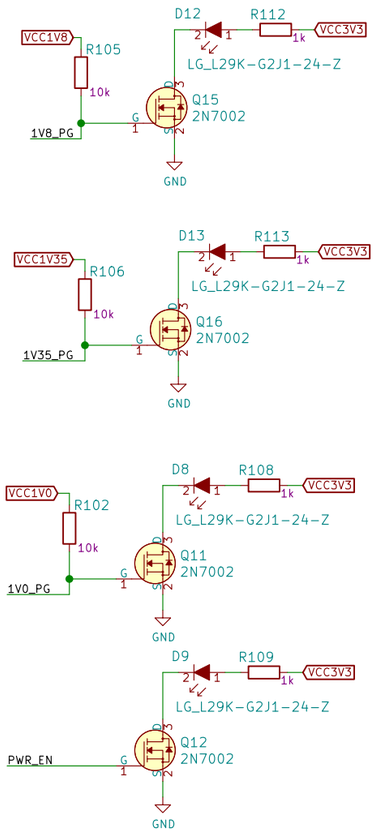


Sheet: /DDR3/		
File: ddr3.sch		
Title: ECP5 – Datacenter Secure Control Module (DC-SCM)		
Size: A3	Date:	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 7/10

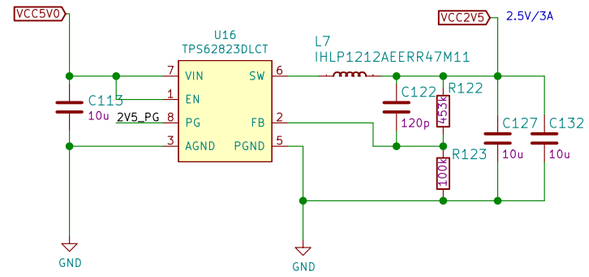
MainSupply (5V 5A)



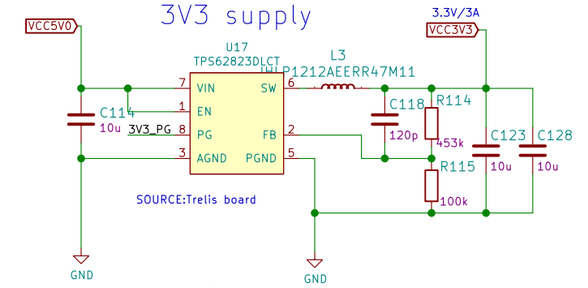
PWR_LED Indicators



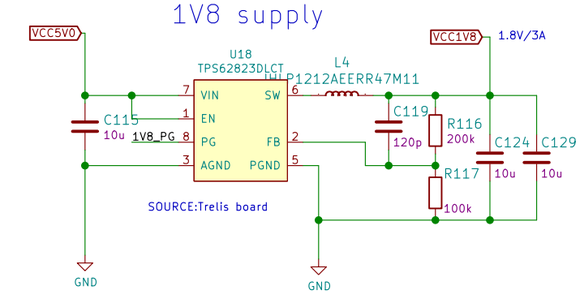
2V5 Supply



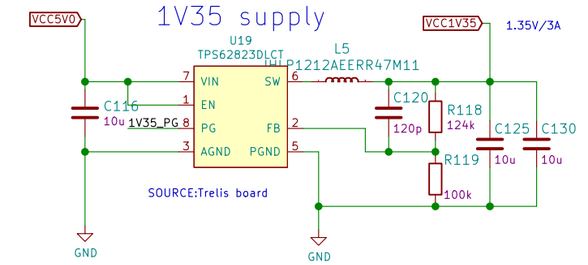
3V3 supply



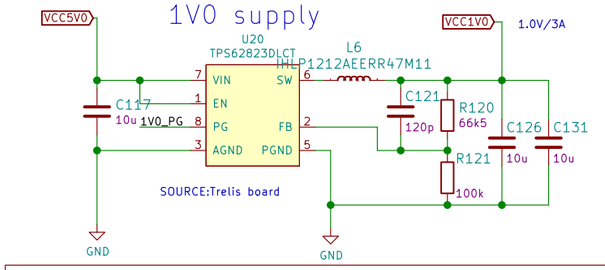
1V8 supply



1V35 supply

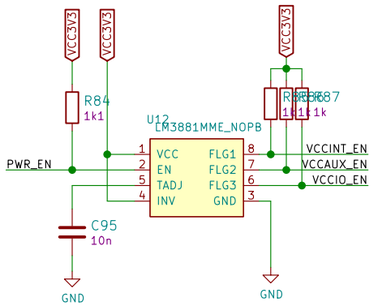


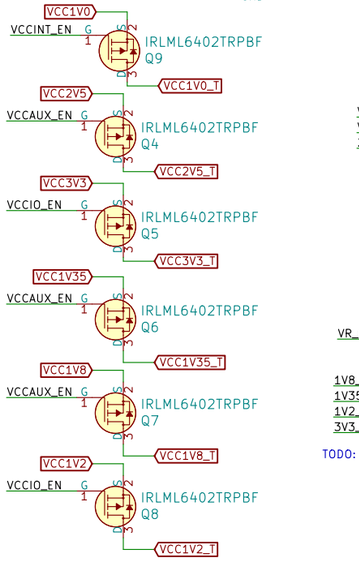
1V0 supply

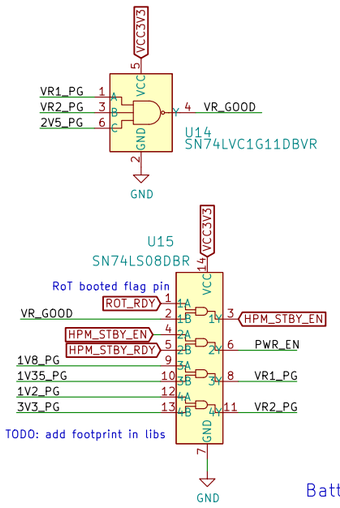


1V2 Supply

Power sequencer





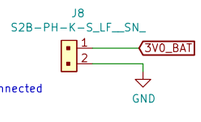


STEP1: VRs start and RoT boots (HPM_STBY_EN when both are done)
STEP2: HPM starts its VRs and sets HPM_STBY_RDY when done
STEP3: FPGA VCCINT (1.0V)
STEP4: FPGA VCCAUX + DDR3 (1.8V, 1.35V)
STEP5: FPGA VCCIO + DDR3 (3.3V, DDRVTT), HPM reset is de-asserted
STEP6: HPM boots

^ TODO: decide which DC-SCI pin connected to FPGA does this

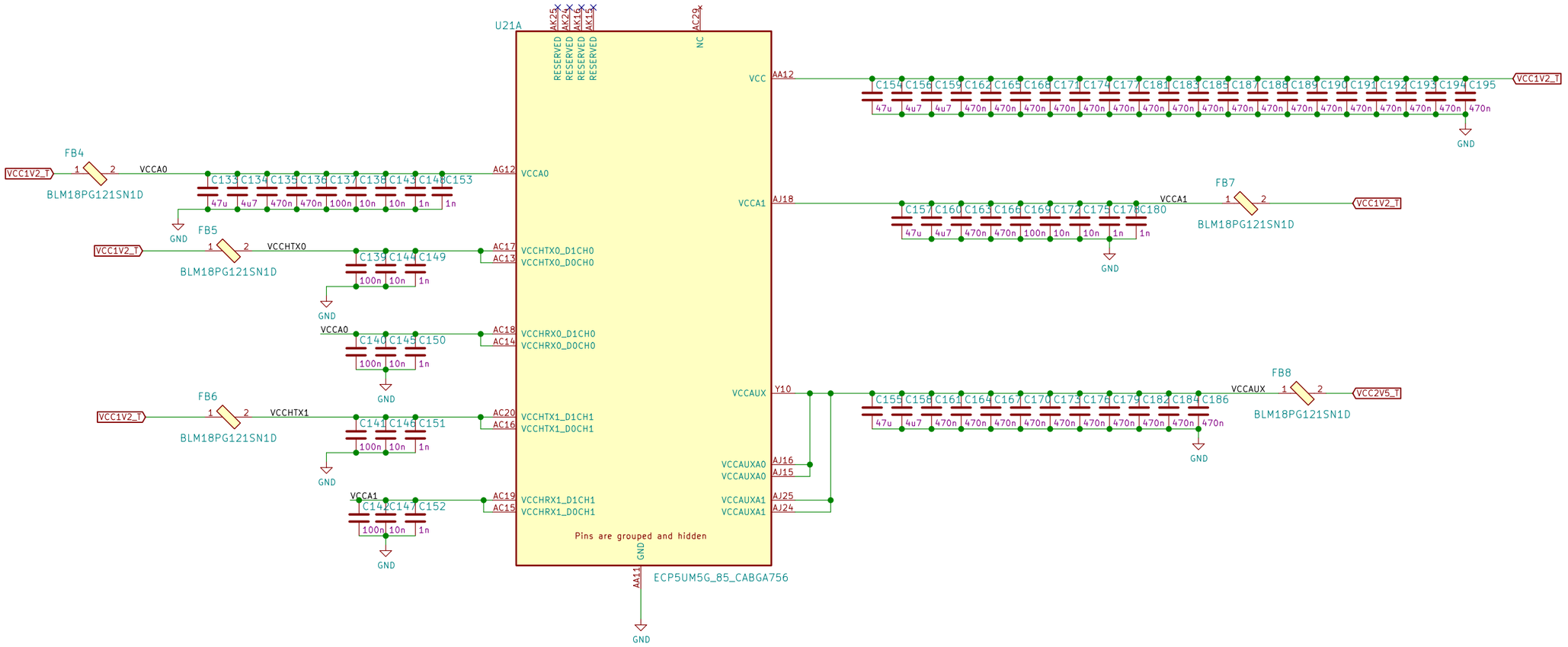
HPM_STBY_RST_N

Battery connector



Sheet: /Power supply/		
File: power-supply.sch		
Title: ECP5 – Datacenter Secure Control Module (DC-SCM)		
Size: A3	Date:	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 8/10

Power supply



Sheet: /FPGA power supply/		
File: fpga-power-supply.sch		
Title: ECP5 – Datacenter Secure Control Module (DC-SCM)		
Size: A3	Date:	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 9/10

FPGA connections to be established while preparing layout

DDR3

RGMII_REFCLK is movable:
not used in Ref

USB1 between HPM and BMC
USB2 between BMC and HPM expansion

ethernet.sch

1V8

DDR3_CS and DDR3_RESET
not used in Ref

ROT_SPI

JTAG

PCIe x1

TBD: should additional GPIO pin be considered as BootStrap pin (OCP mentions 50k pulldown)

ECP5UM5G_85_CABGA756

Sheet: /FPGA banks/	
File: fpga-banks.sch	
Title: ECP5 – Datacenter Secure Control Module (DC-SCM)	
Size: A3	Date:
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1	Id: 10/10