txpll.pll analysed at 10/10/20 18:30:37

PLL Chip is ADF4351
Notes:
VCO is ADF4351
Reference is custom

Advanced Design - VCO Divider is Outside loop and set as follows:

Start Freq	Stop Freq	VCO Divider	Channel Spacing
150MHz	275MHz	16	31.25 Hz
275MHz	550MHz	8	62.5 Hz
550MHz	1.10GHz	4	125 Hz
1.10GHz	2.20GHz	2	250 Hz
2.20GHz	4.40GHz	1	500 Hz

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 1.875GHz
VCO divider set to 2

Phase Noise Table

Freq	Total	VCO	Ref	Chip	SDM	Filter
10.0	-77.84	-81.39	--	-80.37	-228.9	-141.8
100	-77.51	-77.82	--	-89.08	-188.9	-121.9
1.00k	-74.39	-74.46	--	-93.23	-148.6	-102.1
10.0k	-79.77	-80.25	--	-93.18	-107.7	-92.19
100k	-106.8	-116.6	--	-132.7	-107.4	-127.0
1.00M	-137.3	-137.3	--	-190.3	--	-166.5

Reference Spurious
Noise and Jitter Calculations include the first 10 ref spurs
First three spurs: -300 dBc -300 dBc -300 dBc

Fractional-N Spur Estimate (worst case)
Phase Detector mode is Dither OFF

Freq (Hz)	Spur Level (dBc)
0	-51.0
0	-51.0
0	-51.0

Phase jitter using brick wall filter
from 1.00kHz to 20.0MHz
Phase Jitter **2.08ps rms**

---- End of Frequency Domain Results ----

Transient Analysis of PLL
Power up transient to frequency of 1.875GHz
Simulation run for 5.00ms Final Tuning voltage = 1.2832 V

Frequency Locking
Time to lock to 1.00kHz is 391us
Time to lock to 10.0 Hz is 557us

Phase Locking (VCO Output Phase)
Time to lock to 10.0 deg is 400us
Time to lock to 1.00 deg is 483us

Lock Detect Threshold
Time to lock detect exceeds 2.50 V is 224us

---- End of Time Domain Results ----