

8V97003

Lock Time Optimization

Contents

1. Introduction	2
2. Definition of Frequency Lock	2
3. Definition of Phase Lock.....	2
4. VCO Calibration	2
5. PLL Lock Time in VCO Auto-Calibration Mode	2
6. PLL Lock Time in VCO Manual Calibration Mode	4
7. Conclusion	7
8. Revision History	7

Figures

Figure 1. PLL Lock Time in Auto-Calibration with Instrument in Wide-Band Mode	3
Figure 2. PLL Lock Time in Auto-Calibration with Instrument in Narrow-Band Mode	4
Figure 3. PLL Lock Time, 20MHz Step, VCO Manual Mode	6
Figure 4. PLL Lock Time, 200MHz Step, VCO Manual Mode	6
Figure 5. PLL Lock Time, 600MHz Step, VCO Manual Mode	7

1. Introduction

The 8V97003 is a high-performance wideband mmWave RF Synthesizer utilizing a Phase Lock Loop (PLL) that generates output frequencies up to 18GHz from an integrated Voltage Controlled Oscillator (VCO). The excellent VCO performance supports the generation of clock signals with very low phase noise and RMS jitter. The extensive programmability on all major functional blocks allows for flexible use of the device in many applications.

This document discusses frequency lock time for applications where this parameter is critical to optimize.

2. Definition of Frequency Lock

The PLL Lock time for frequency lock is the time it takes from power-up or a configured frequency change to when the output frequency is consistently within a certain frequency tolerance from the desired frequency. In most RF synthesizer applications, the time for the PLL to get to this desired output frequency is of primary interest. For example, with the default device settings, the PLL lock time is about 1ms for achieving a target output frequency within a $\pm 100\text{kHz}$ tolerance.

The frequency lock time depends on the loop bandwidth and the duration of the device internal VCO calibration.

3. Definition of Phase Lock

The PLL phase lock time is the time from power-up or configured frequency change to when the phase difference between the input reference and the output is within the desired phase precision. The 8V97003 has an internal Lock Detection circuitry that reports the phase lock status according to the precision parameter set by the LDP[2:0] bits in the device register 0x0027[2:0]. This document does not discuss phase lock.

4. VCO Calibration

The VCO consists of multiple VCO cores where one core is used by the PLL at a time. Each core selects one of multiple VCO frequency bands for operation. The process of selecting the best core and the frequency band for a given target PLL frequency is called VCO calibration.

After power-up, the device is in auto-calibration mode – the selection of VCO and frequency band does not require the user to interact with the device as the best configuration is chosen automatically.

During operation, a change of the output frequency by configuring the frequency dividers can cause the auto-calibration to trigger and select a new VCO/band. The time for this re-calibration to the new frequency configuration is part of the PLL lock time.

If PLL lock time is too long for an application, the manual calibration mode can be chosen. Manual calibration is faster than and more predictable in time than auto-calibration.

5. PLL Lock Time in VCO Auto-Calibration Mode

For the discussion in this section, the test conditions are specified as follows:

- The loop filter and the 8V97003 charge pump current settings produce a loop bandwidth of around 350kHz.
- The register BandSelDivider is set to divide the phase-frequency detector (PFD) frequency to 78.125kHz.
For example, with an input reference frequency of 100MHz, input frequency doubler enabled (PFD frequency = 200MHz), setting BandSelDivider to a value of 2560 provides the band select clock frequency of 78.125kHz.
- BandSelAcc = 1, 2, and 3. Most focus will be on BandSelAcc = 2. To ensure reliably accurate VCO calibration, BandSelAcc = 0 and 1 are not recommended; performance with BandSelAcc = 1 is shown for comparison purposes only.

In auto-calibration mode, lock time is a function of the following VCO calibration parameters:

- Band Select Divider (BandSelDivider 13 bits in registers 0x0023[4:0] and 0x0022[7:0])
- Band Select Accuracy (BandSelAcc, 2 bits in register 0x0021[1:0])

The frequency lock time for frequency lock within $\pm 100\text{kHz}$ output frequency tolerance is as follows:

Band Select Clock Frequency	Band Select Accuracy	Lock Time ($\pm 100\text{kHz}$)
78.125 KHz	1	550 μs
78.125 KHz	2	1ms
78.125KHz	3	1.9ms

To illustrate the lock time data in the table, the transient response frequency over time is shown below for the following test conditions:

- 8V97003 device settings:
 - a Band Select Accuracy of 2
 - Input reference frequency (REFCLK) = 100MHz, f_{PFD} = 200MHz
 - Target Output Frequency = 6.2GHz
- Measurement Equipment setting:
 - Wideband mode: 256MHz to 8GHz range, VBW = 100KHz
 - Low band mode: 0Hz to 26.5GHz range, VBW = 10KHz

Trigger for the frequency-vs-time measurement in VCO auto-calibration mode is the SPI write to start VCO re-lock (register 0x21[7]). Specifically, the rising edge of the nCS signal in the SPI write operation acts as trigger for time 0 in this lock time measurement.

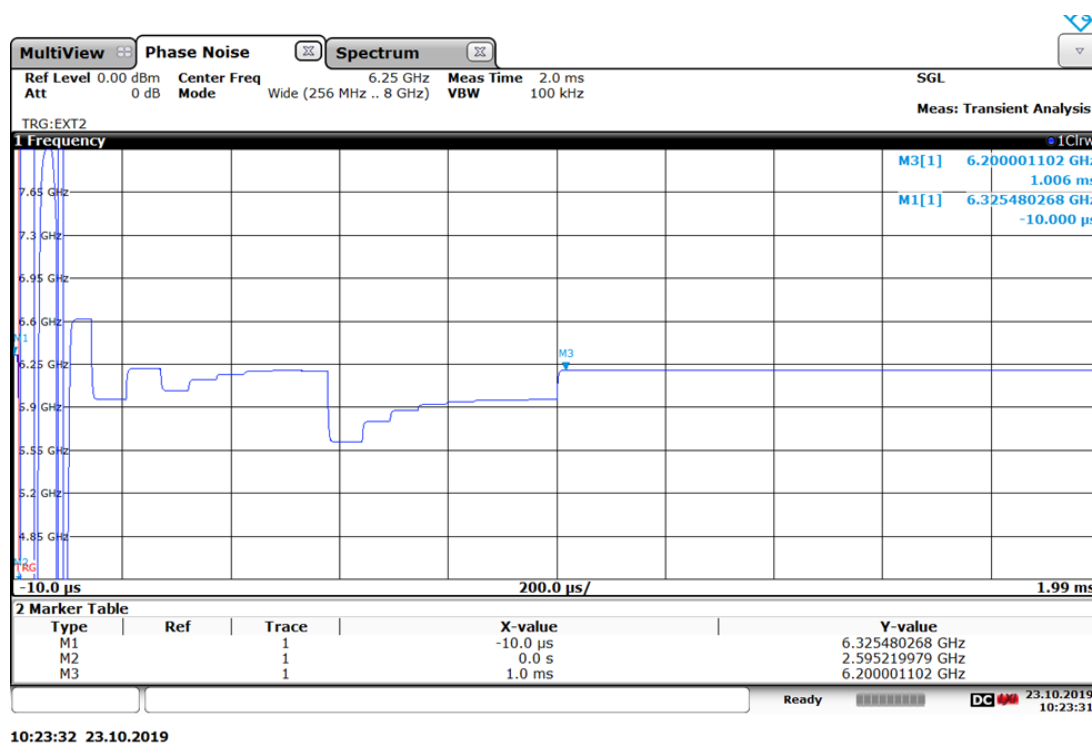


Figure 1. PLL Lock Time in Auto-Calibration with Instrument in Wide-Band Mode

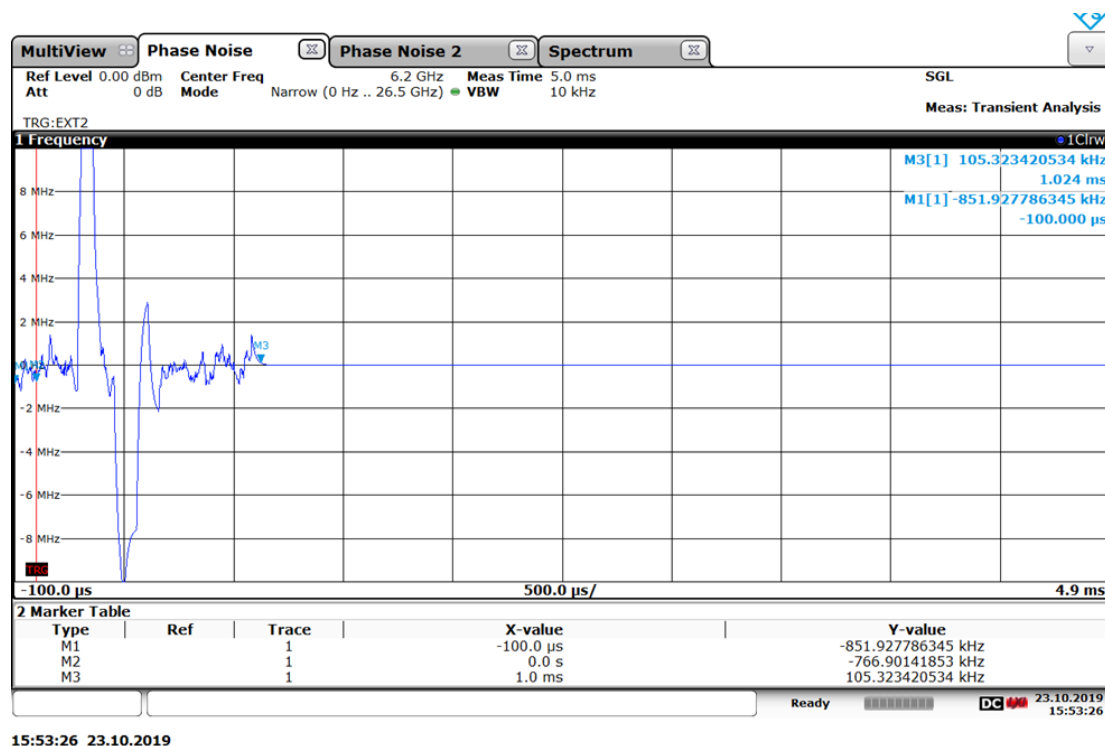


Figure 2. PLL Lock Time in Auto-Calibration with Instrument in Narrow-Band Mode

6. PLL Lock Time in VCO Manual Calibration Mode

The manual VCO calibration mode of the device can decrease frequency lock time considerably. In manual calibration mode, the device auto-calibration routine is disabled. VCO and frequency band selection must be done by the user by providing settings to specific VCO registers. The correct selection settings are obtained by running auto-calibration first and reading and storing the settings outside of the device for re-deploying them into the device during a fast frequency change. Manual calibration is applicable in applications that can store the VCO and band selection settings for each target PLL frequency in a look-up table ahead of time (i.e., after device power-up and before any operational PLL frequency change). The values for the look-up table are unique to each device. Since they are a result from the auto-calibration function, they are guaranteed to work across temperatures.

To pre-determine the VCO bands for manual mode operation, complete the following the procedure:

1. Use auto-calibration mode (the default setting).
2. Establish the desired operation and frequency conditions (including 8V97003 frequency divider settings and at the target operating temperature).
3. Check that VCO calibration finished (test the setting BandSelDone in Register 0x0044[6] = 1).
4. Read-back and store the register settings for:
 - the selected VCO (Register 0x0044[3:0])
 - the selected digital VCO band (Register 0x0045[6:0])
5. Repeat steps 2 and 3 for each target output frequency.

6. Build a look-up table that consists of each target frequency with the corresponding settings:

- PLL output frequency
- Feedback divider settings: Nint, Nfrac, and Nmod
- VCO (register 0x0044[3:0])
- Digital VCO band (register 0x0045[6:0])

The device can now be operated in manual mode to allow for faster switching between the frequencies in the look-up table. Automatic band selection must be disabled, and VCO manual mode enabled, as outlined in the following procedure:

1. Program the 8V97003 in normal mode for the first desired output frequency. This is done in order to calibrate to the correct VCO control voltage.
2. Disable automatic band selection: set BandSelDisable in register 0x0021[5] = 1.
3. Enable VCO manual mode: ManuBandEn in register 0x001F[7] = 1.
4. Set up the next desired output frequency:
 - a. Set feedback divider:
 - Nint in register 0x0010[7:0] and 0x0011[7:0]
 - Nfrac in registers 0x0012[7:0] through 0x0015[7:0]
 - Nmod in register 0x0016[7:0] through register 0x0019[7:0]
 - b. Set VCO in register 0x0044[3:0]
5. Set the VCO override values:
 - a. Take the VCO override value and apply it to register 0x001F[3:0].
 - b. Take the VCO digital band override value and apply it to register 0x0020[6:0].
6. Apply settings from step 4 by writing 1 to TransferOn in register 0x000F[0].
7. To jump to the next frequency in the look-up table, repeat steps 4 and 5.

In the following example, the 8V97003 was operated in manual calibration mode with output frequencies switches at various steps of 20MHz, 200MHz, and 600MHz.

Desired f _{out}	Nint	Nfrac	Nmod	VCO	Digital Band
6.20GHz	31	0	2	1	60
6.25GHz	31	1073741823	4294967292	1	76
6.27GHz	31	1503238548	4294967280	1	76
6.40GHz	32	0	2	1	94
6.80GHz	34	0	2	2	40

Trigger for the frequency-vs-time measurement in VCO manual mode is the SPI write to start the transfer of VCO, digital band settings to the internal register map, and TransferOn in register 0x000F[0]. Specifically, the rising edge of the nCS signal in this SPI write operation acts as trigger for time 0 in this lock time measurement.

Note: It is recommended to use the 1st order on the Delta Sigma Modulator when using manual calibration mode for the best phase noise performance. The order can be selected using register 0x001E[6:4]. For more information on the Delta Sigma Modulator registers, see Table 31 in the *8V97003 Datasheet*.

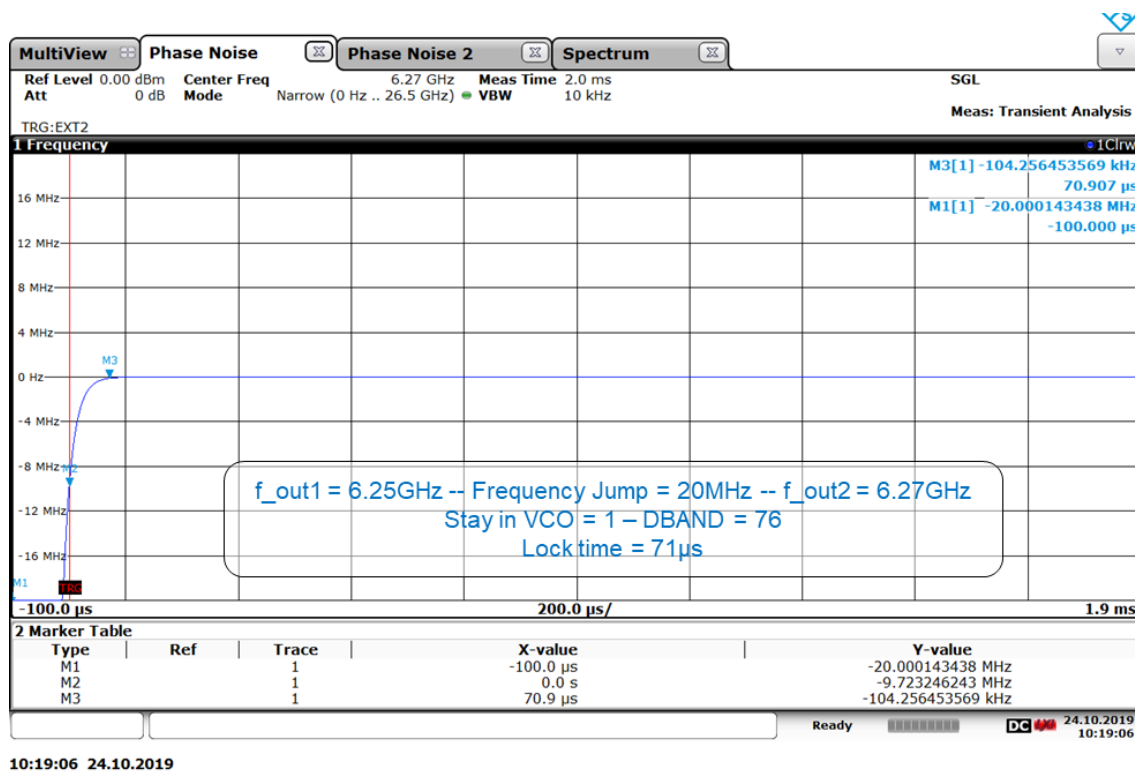


Figure 3. PLL Lock Time, 20MHz Step, VCO Manual Mode

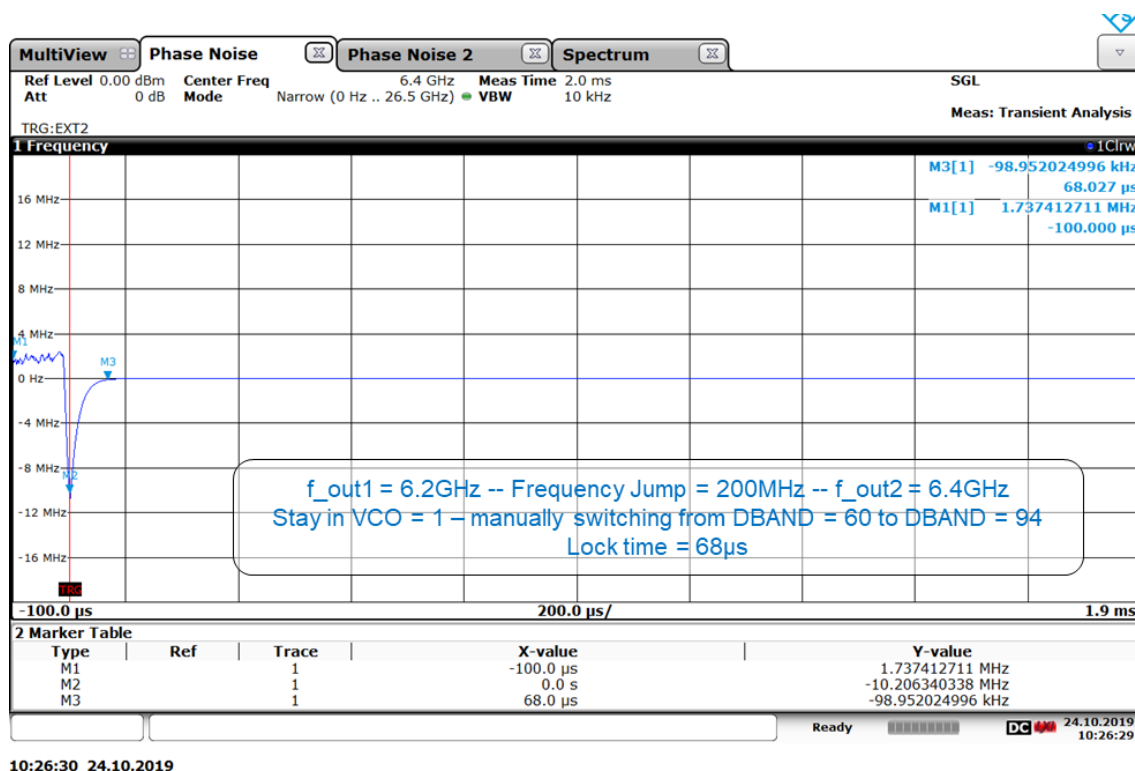


Figure 4. PLL Lock Time, 200MHz Step, VCO Manual Mode

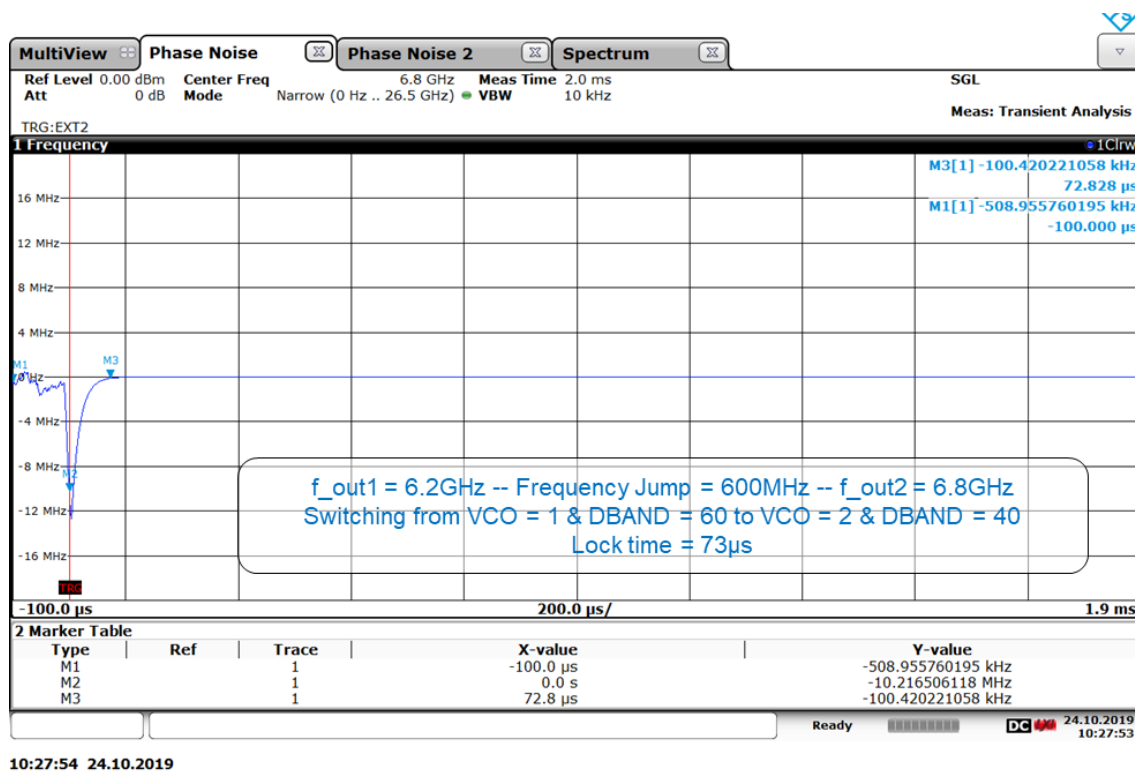


Figure 5. PLL Lock Time, 600MHz Step, VCO Manual Mode

7. Conclusion

When using auto-calibration mode, the 8V907003 will typically lock to ± 100 kHz output frequency tolerance in within 1mS. If a faster lock time is required, VCO Manual Calibration mode can be used to lock to ± 100 kHz output frequency tolerance typically within 70µS, with a maximum lock time of 100µS.

8. Revision History

Revision	Date	Description
1.1	Nov.20.20	Updated the second procedure in PLL Lock Time in VCO Manual Calibration Mode.
1.0	May.27.20	Initial release.

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