Register

This module is used for storing and retriving the data. The word register is a keyword in VHDL, so the name of the module is register_single.

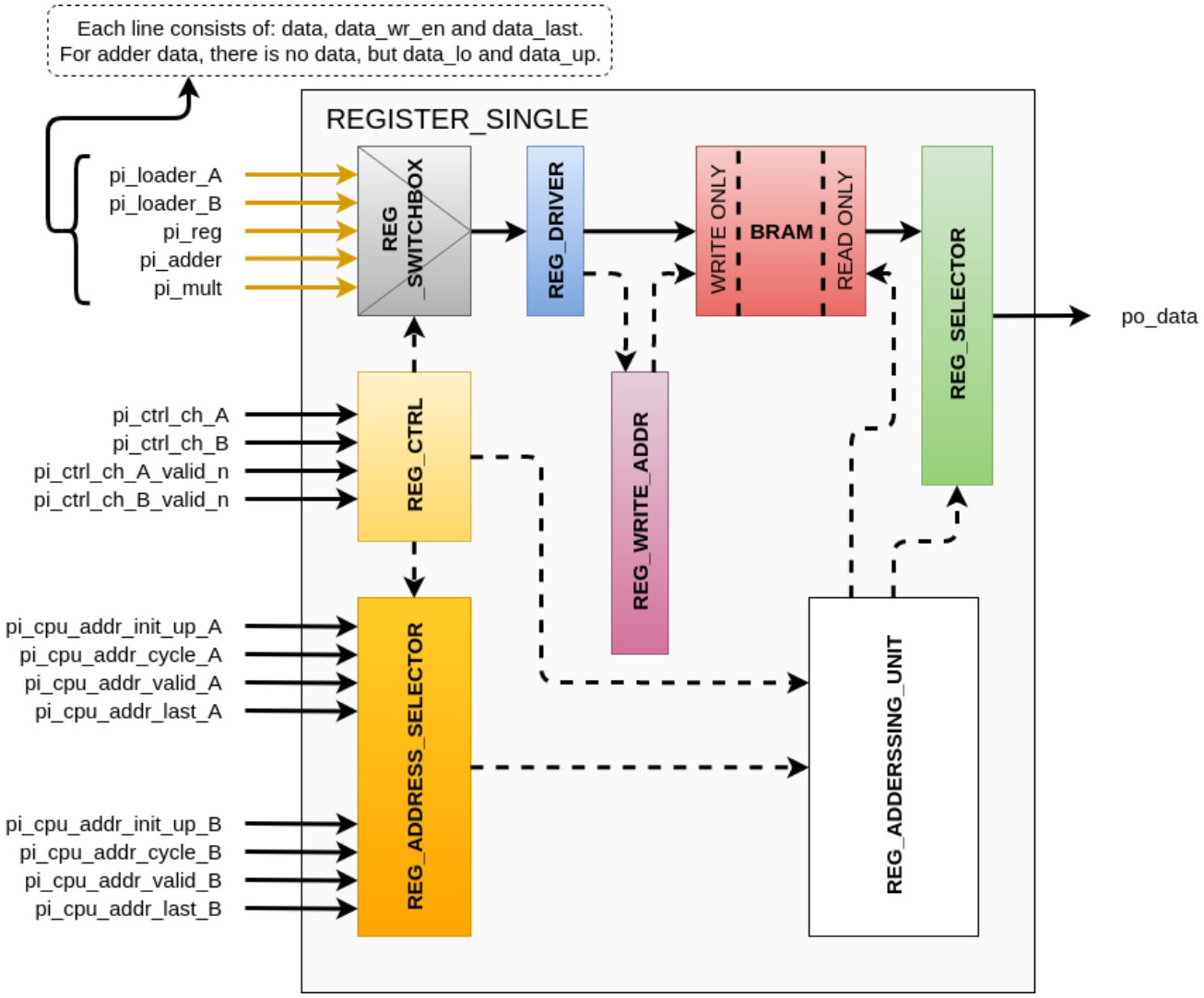
The generic map list is presented in the following table.

name	type	value	description
g_sim	boolean	false	Replaces the BRAM IP core with a FF memory for easier debugging in simulation.
g_lfsr	boolean	true	The addressing counter can be treated as a NBC or LFSR. When true/false, LFSR/NBC is used, respectively.
g_data_width	natural	64	Base precision of the system (limb size).
g_addr_width	natural	9	The width of the address for the limbs (in this case 2^9 = 512 limbs, each g_data_width=64 wide, this gives 32768 bits = 1 BRAM in 7 series Xilinx products).
g_ctrl_width	natural	8	Control communication line width.
g_id	natural	6	Id of the module (has to be coded in no more than 6 bits).

The port list is presented in the following table. TO BE CORREECTED!!!!!!!!!!!!!!!!

group	name	size	direction	description
general	pi_clk	1	in	Clock
	pi_rst	1	in	Reset
control	pi_ctrl_ch_A	g_ctrl_data	in	Control communication line - selects operation (+/-), source operand A
	pi_ctrl_ch_B	g_ctrl_data	in	Control communication line - selects source operand B
	pi_ctrl_valid_n	1	in	Valid signal (active low) for control data to indicate the header of the control communication stream; one signal for both control lines (A and B)
data	pi_data	g_data_width * num_of_phys_registers	in	All registers feed data to this bus. The adder contains two multiplexers to select (based on the control lines) data A and data B.
	pi_data_wr_en	1	in	Valid data (active high) for both operands simulatneously.
	pi_data_last	1	in	Last limb of the larger operand.
	pi_data_last	g_data_width	in	Result data up.
	po_data_down	g_data_width	out	Result data down.

The block diagram of the register is presented in the figure below.



Each block is described in their own sections:

- REG_ADDRESS_SELECTOR
- REG_ADDRESSING_UNIT
- REG_CTRL
- REG_DRIVER
- REG_SELECTOR
- REG_SWITCHBOX
- REG_WRITE_ADDR

example....