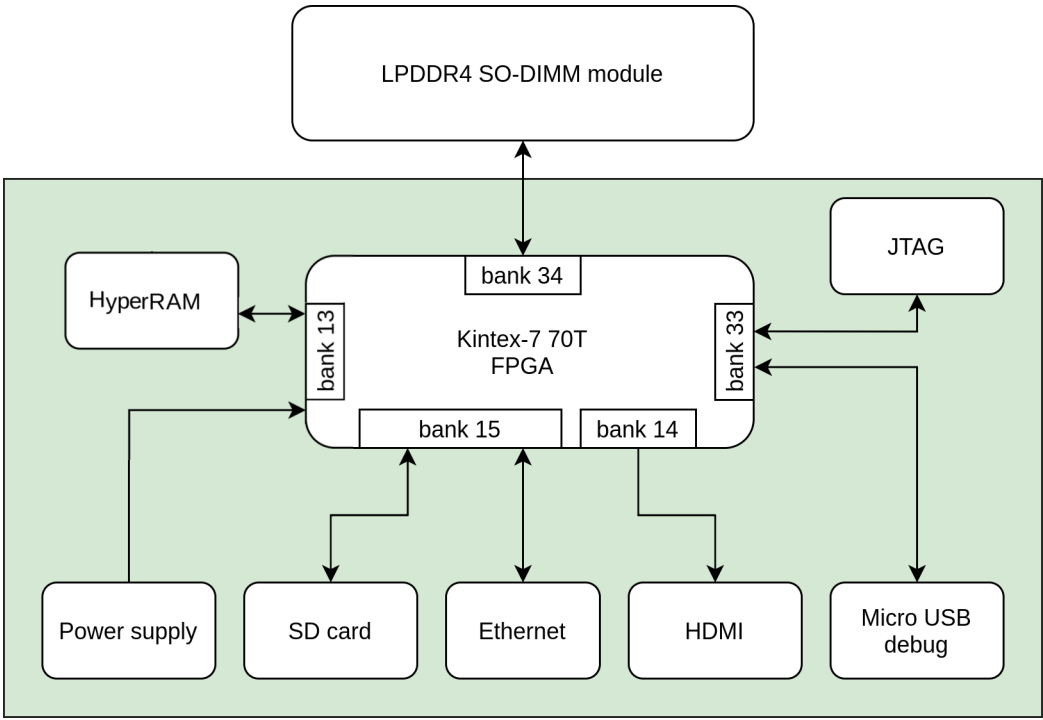


LPDDR4 Test Board



Sheet: HyperRAM

File: hyperram.sch

Sheet: FPGA Banks

File: fpga-banks.sch

Sheet: Interfaces

File: interfaces.sch

Sheet: Config SPI flash

File: config-spi.sch

Sheet: FPGA power

File: fpga-power.sch

Sheet: Ethernet

File: ethernet.sch

Sheet: Supply

File: supply.sch

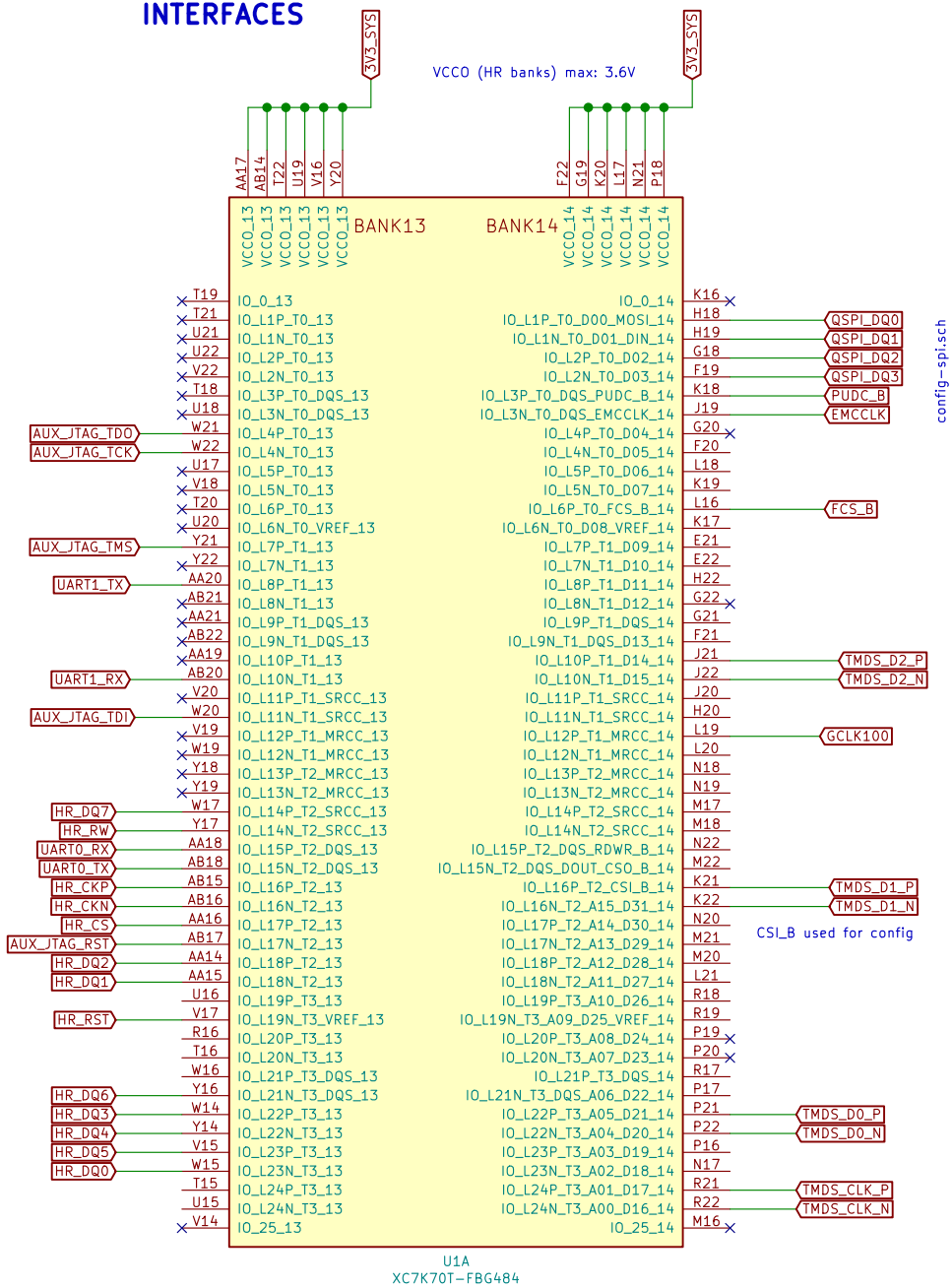
Sheet: SO-DIMM

File: sodimm.sch

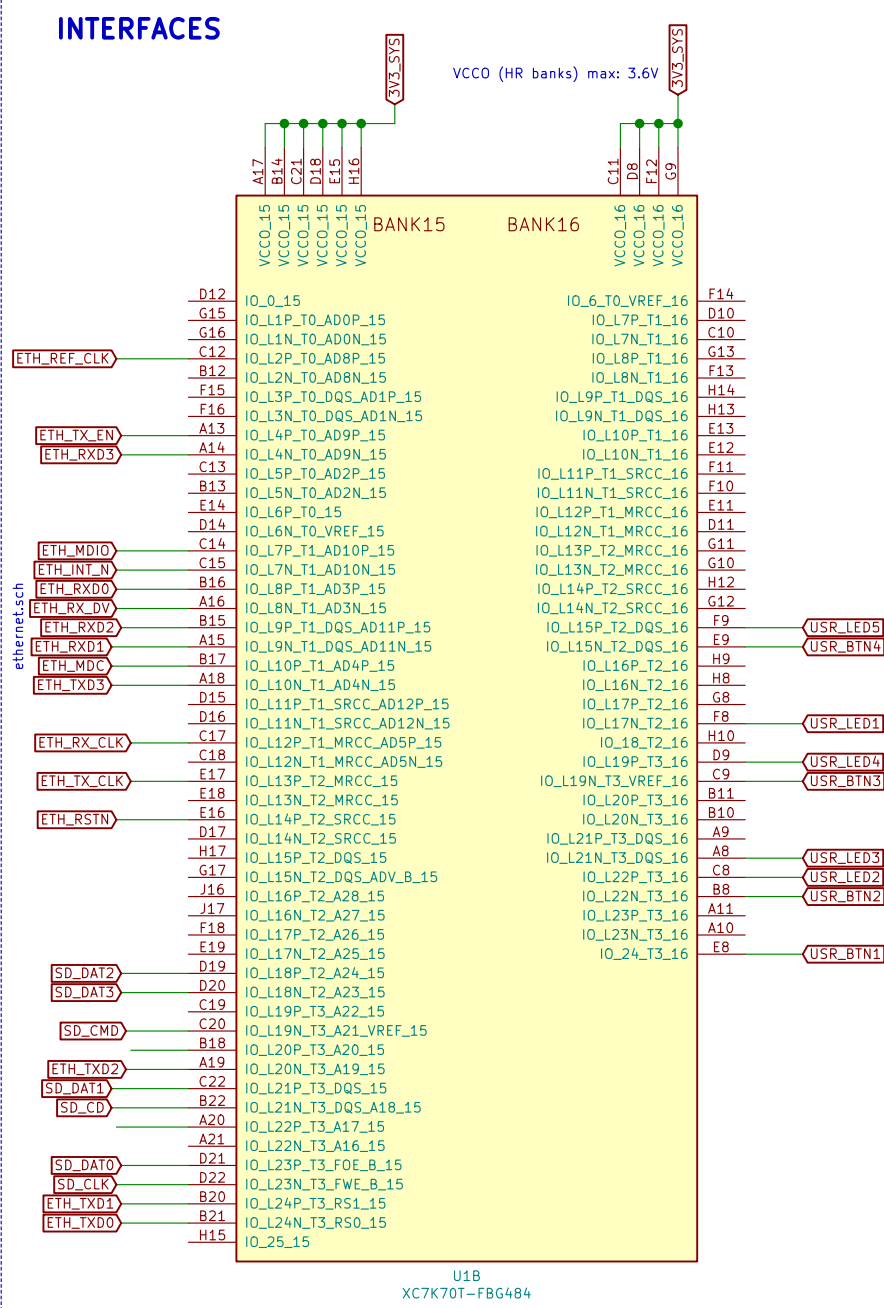
Logo ^{N1}oshw_logo
Logo ^{N2}antmicro_logo

| | | |
|--|-------|------------|
| LPDDR4 Test Board | | |
| Sheet: / File: lpddr4-test-board.sch | | |
| Title: LPDDR4 Test Board | | |
| Size: A3 | Date: | Rev: 1.0.4 |
| KiCad E.D.A. eeschema 5.1.4+dfsg1-1bpo10+1 | | Id: 1/9 |

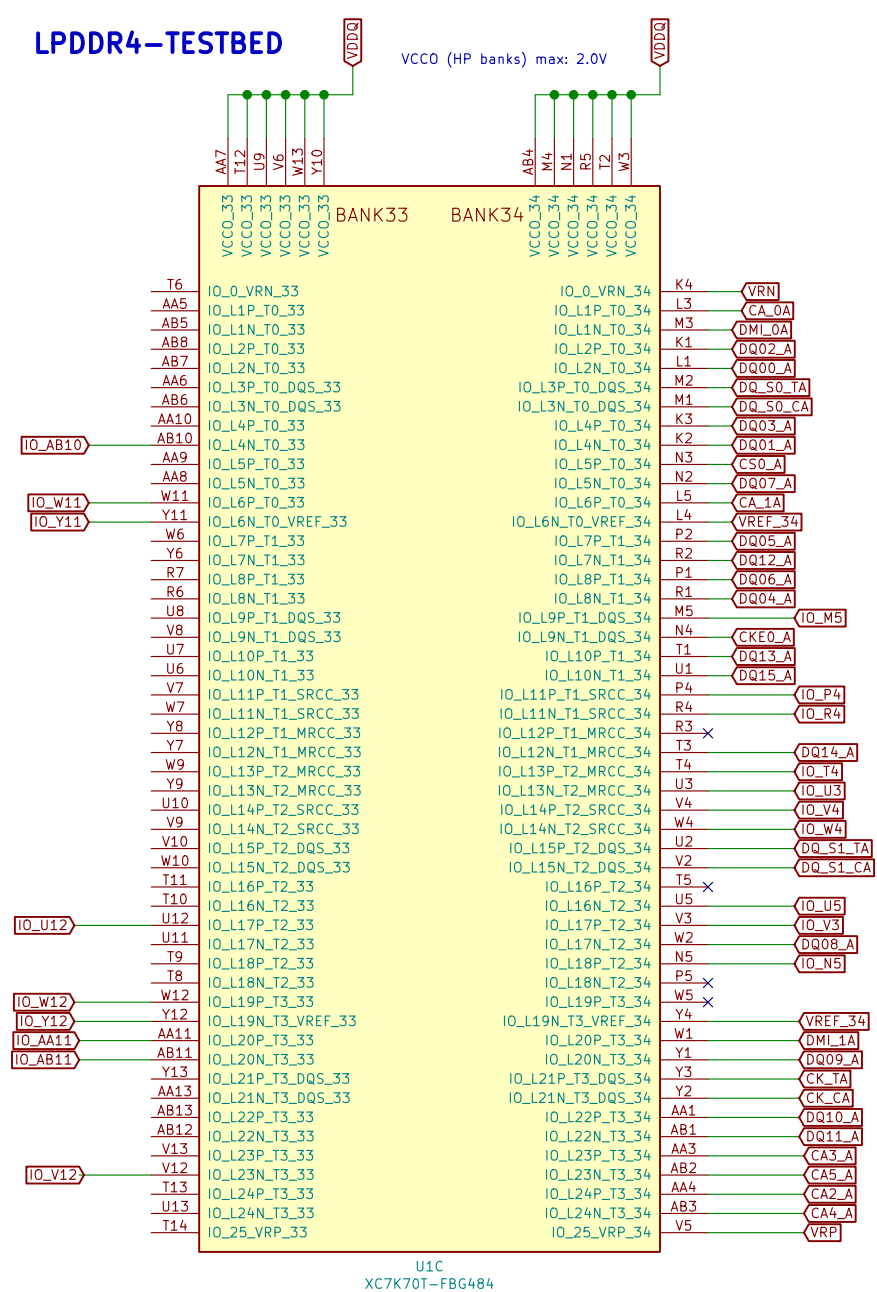
INTERFACES



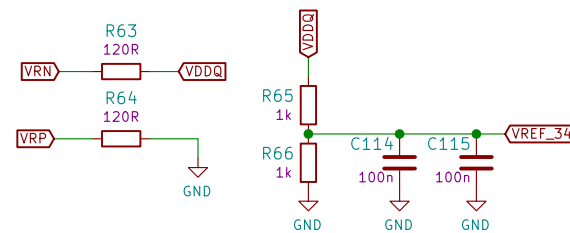
INTERFACES



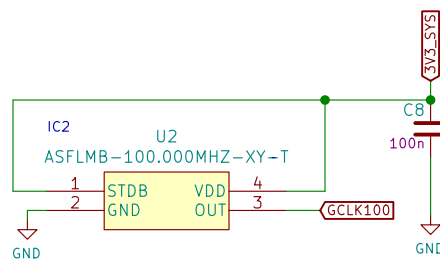
LPDDR4-TESTBED



LPDDR VREF

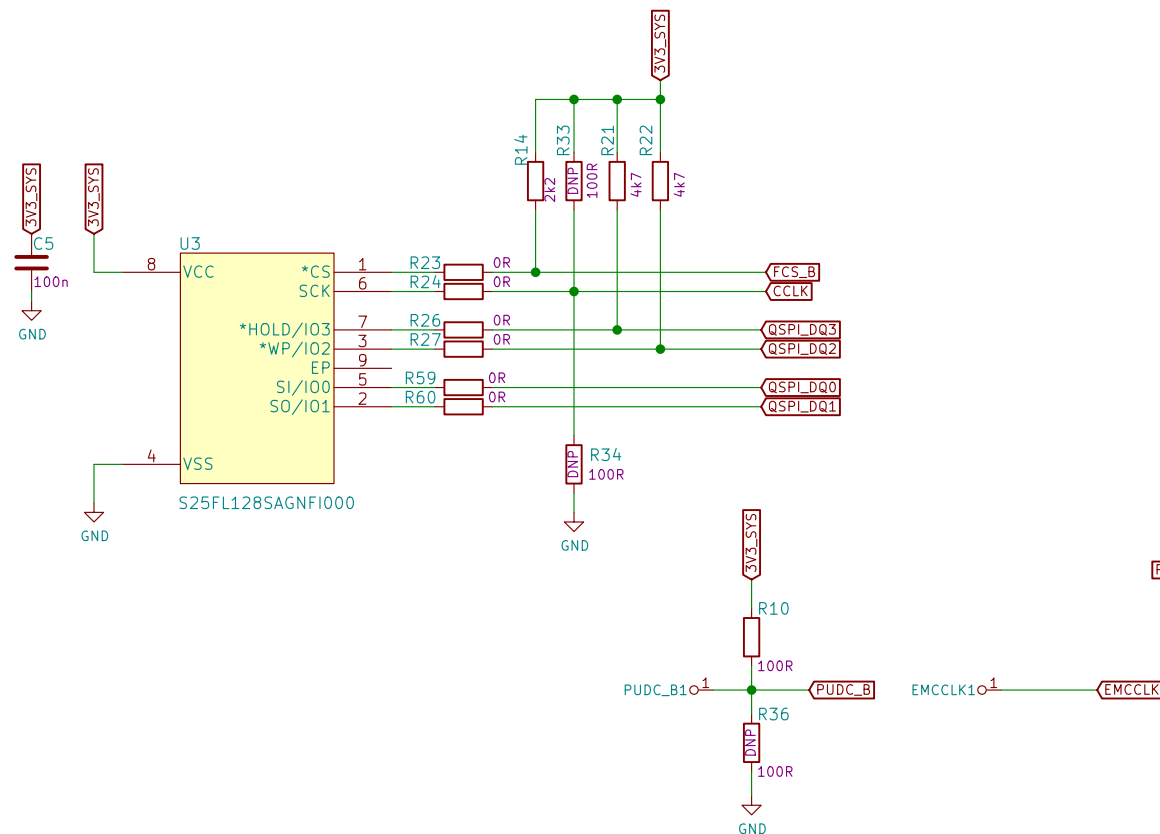


Clock source

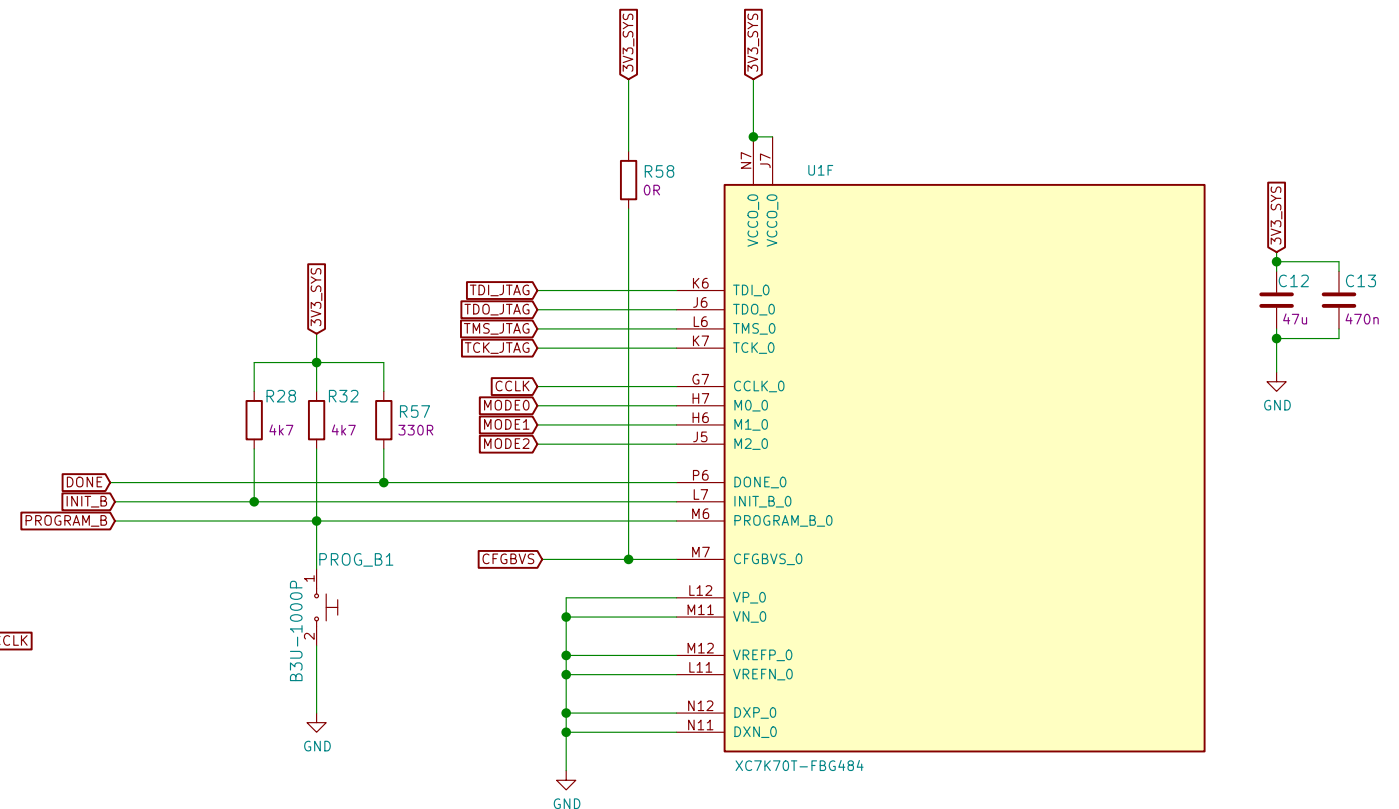


Follows Figure 2-14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

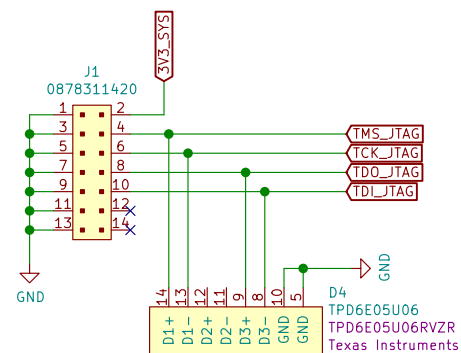
(Q)SPI flash



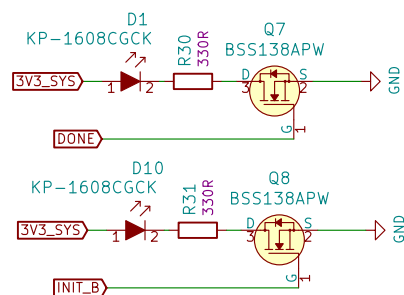
FPGA BANK 0



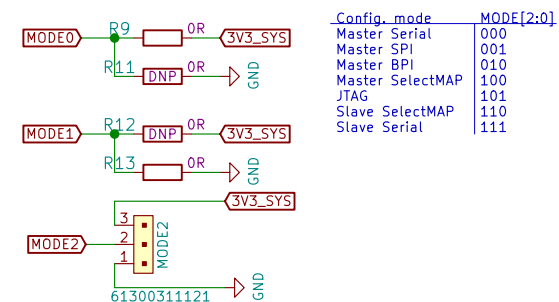
Compatible with Xilinx Platform Cable



STATUS LEDs



For details, see UG470 p. 21

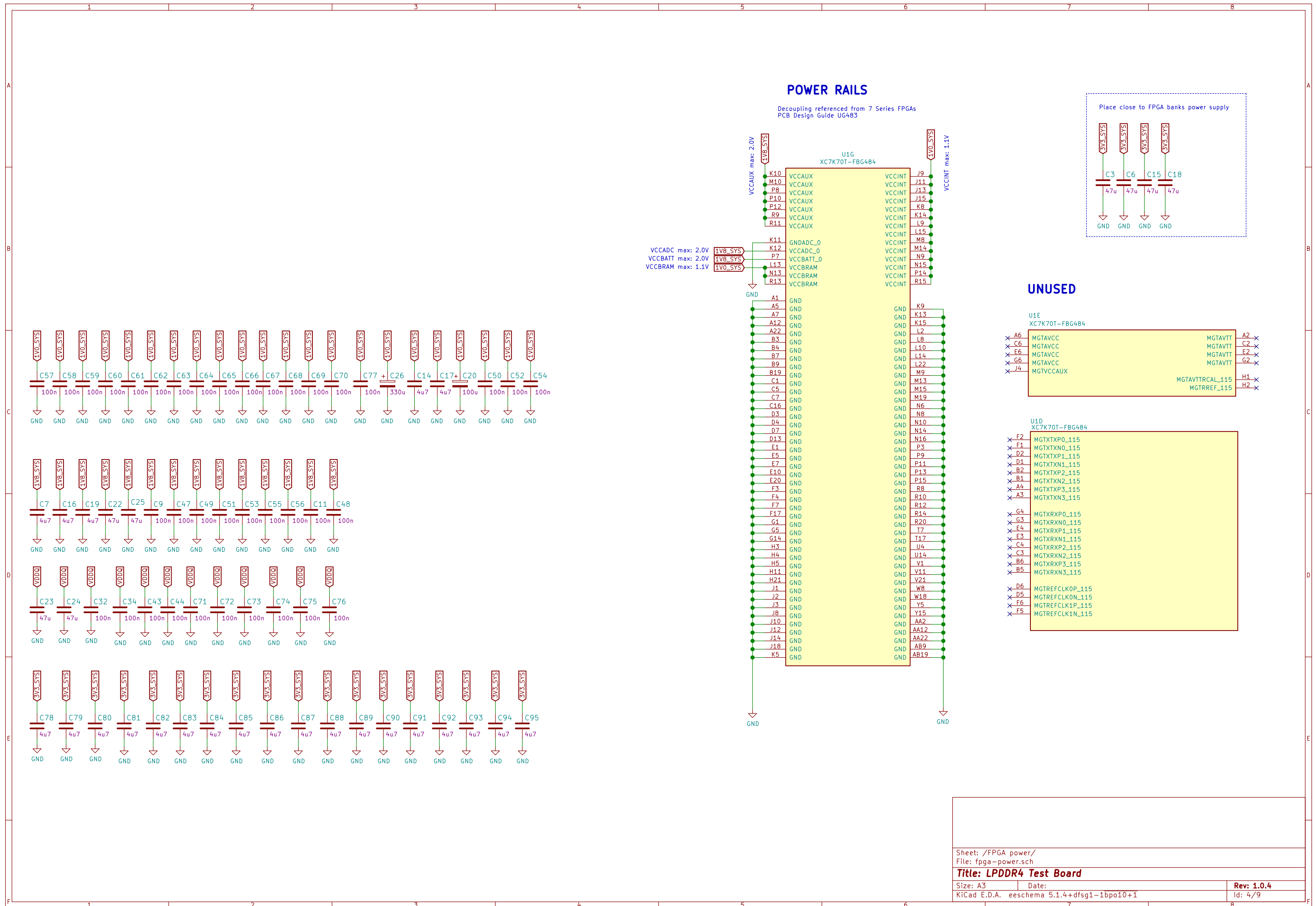


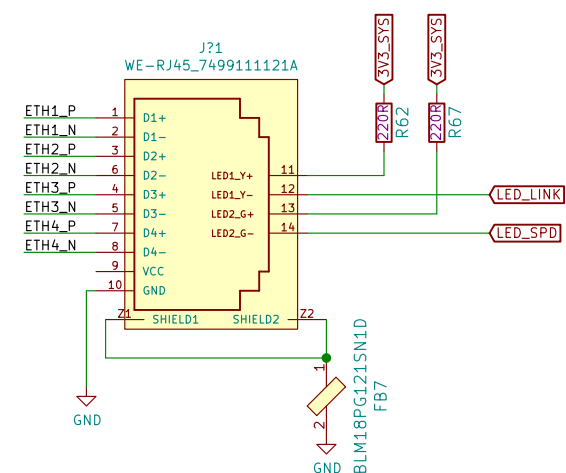
Sheet: /Config SPI flash/
File: config-spi.sch

Title: LPDDR4 Test Board

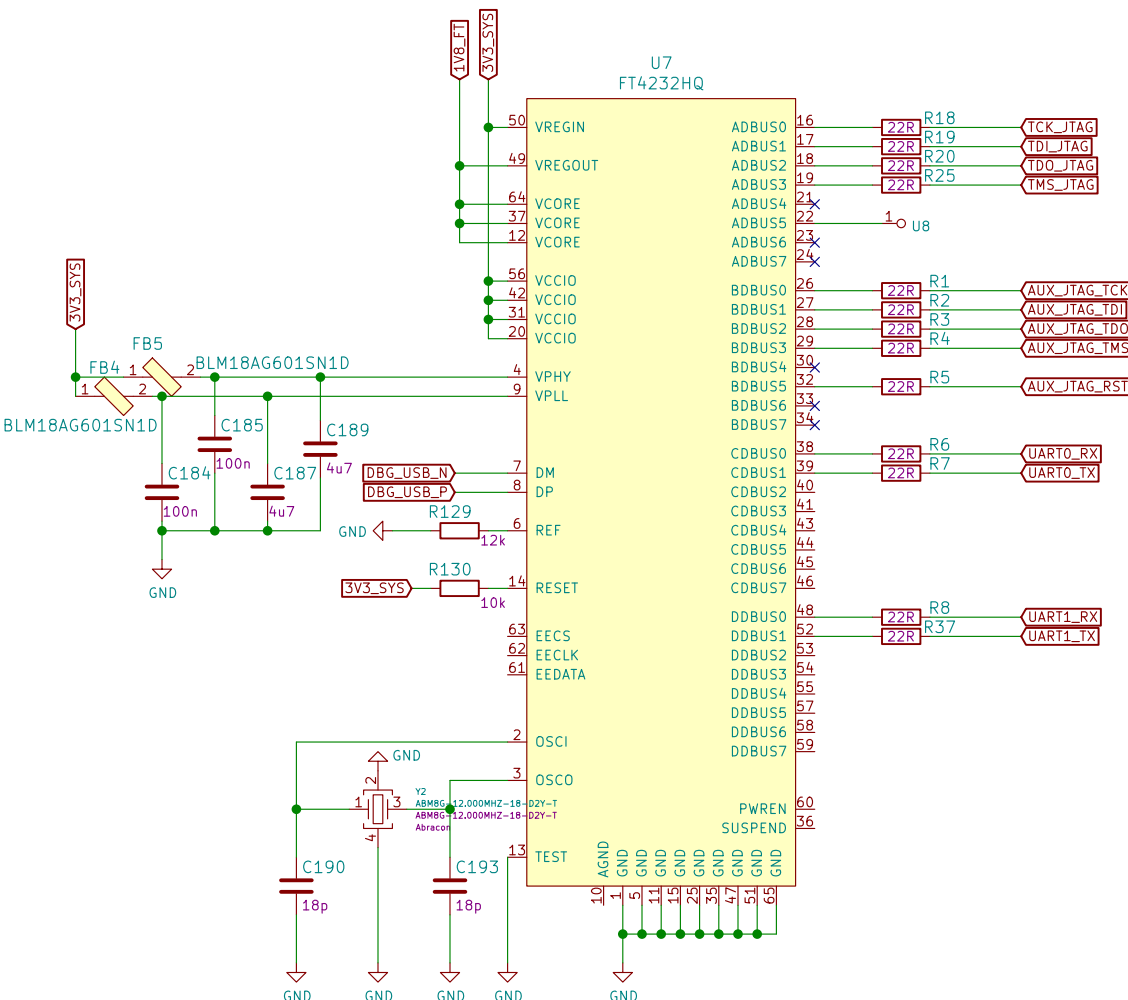
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|--|-------|
| Size: A3 | Date: |
| KiCad E.D.A. eeschema 5.1.4+dfsg1-1bpo10+1 | |

Rev: 1.0.4
Id: 3/9

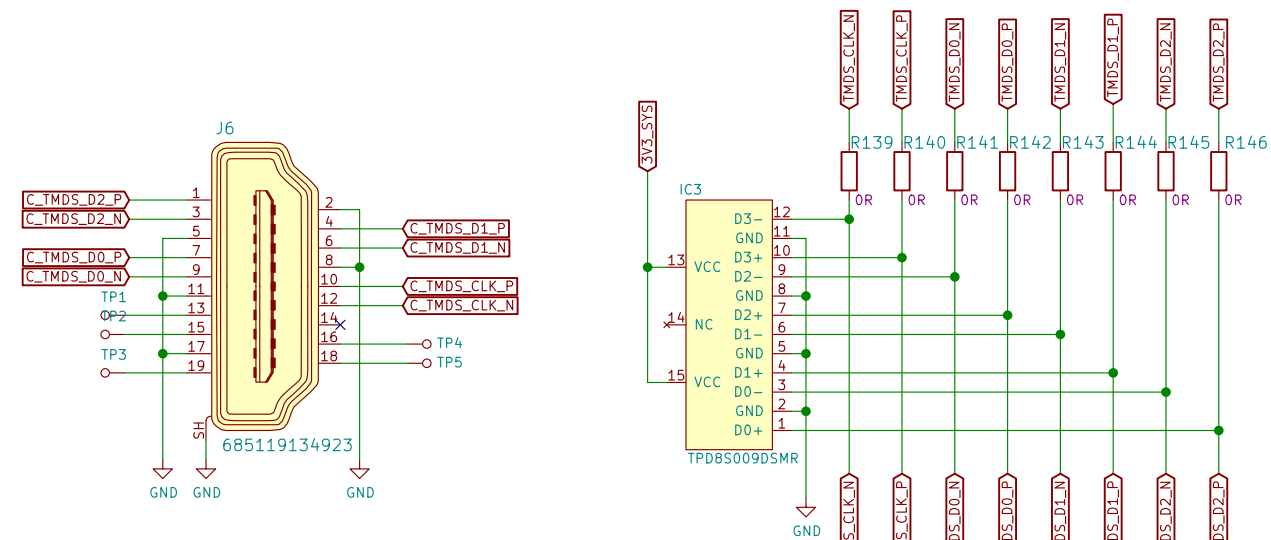




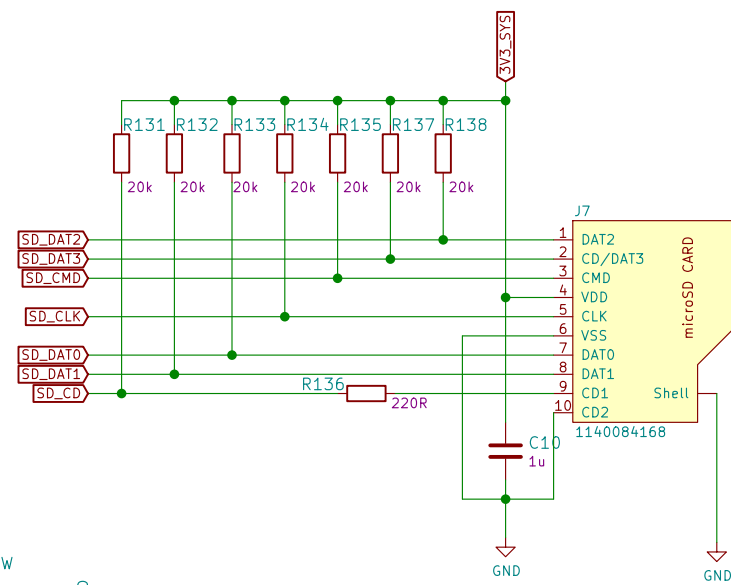
Debug UART



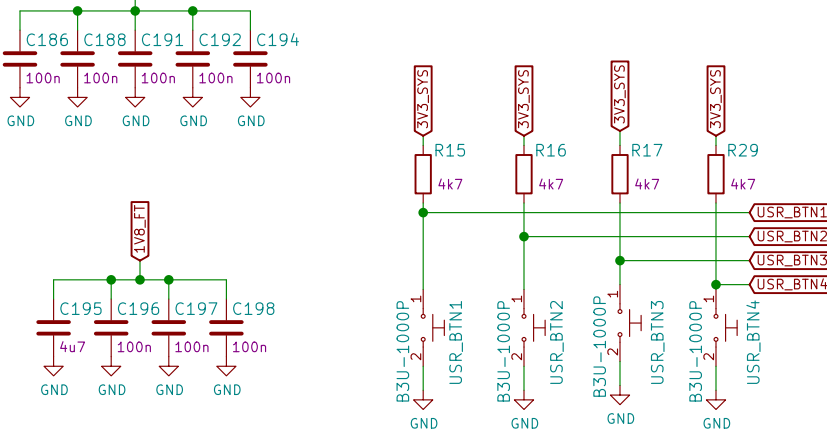
HDMI



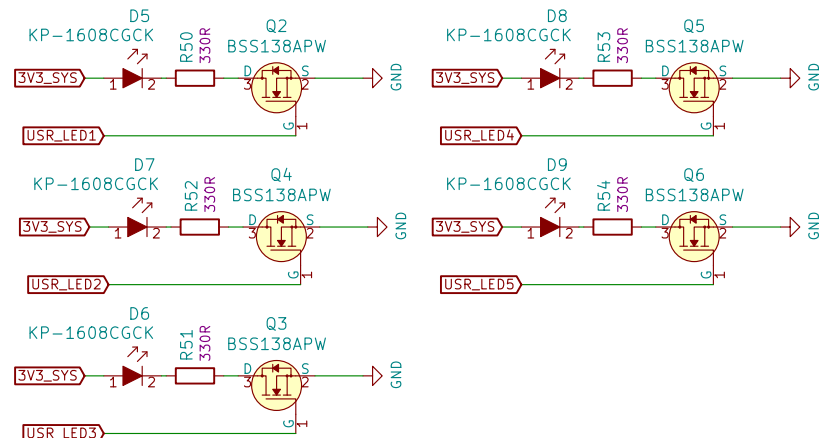
SD card



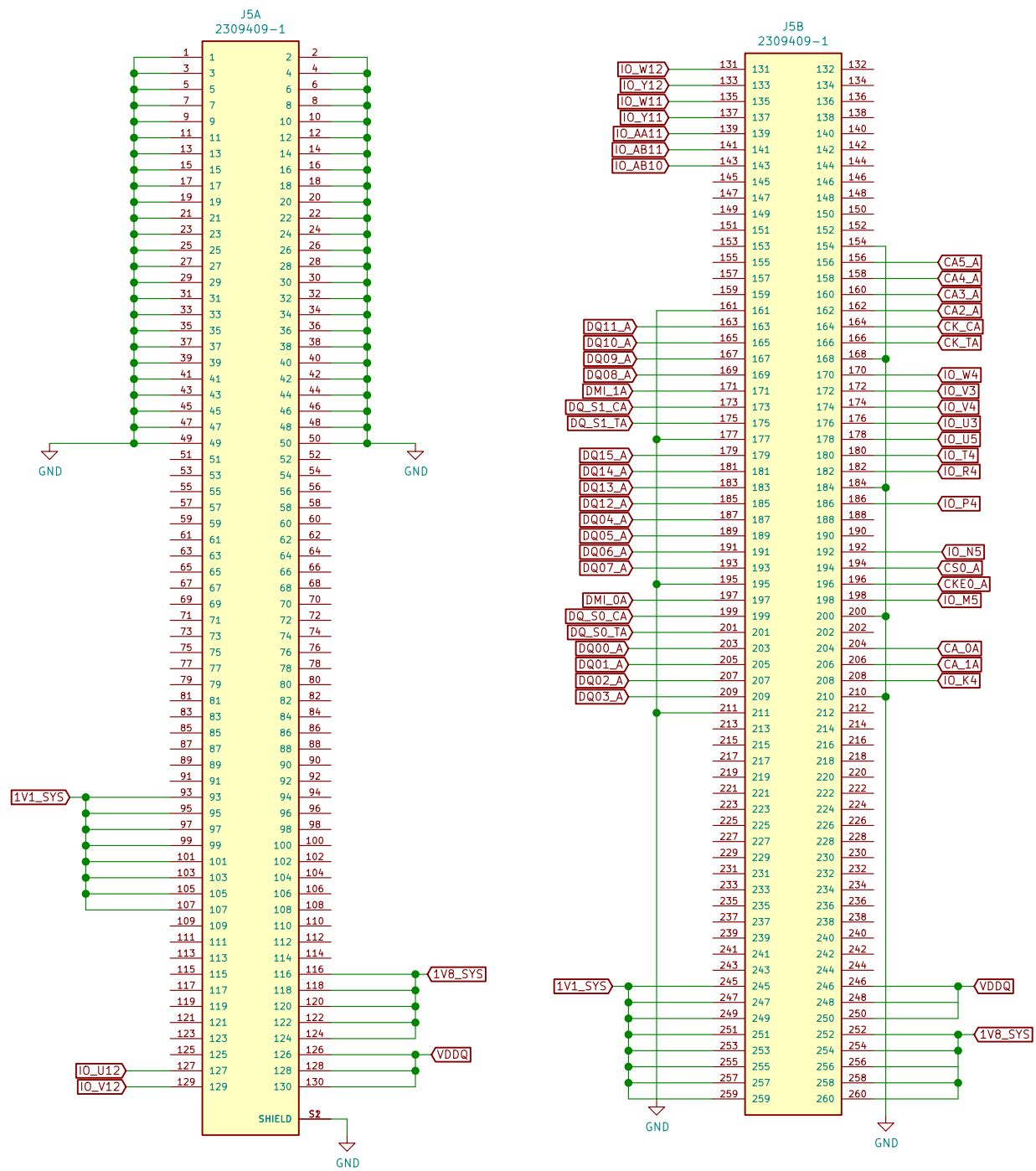
User buttons



User LEDs



DDR4 SODIMM connector



Mechanical protection



HyperRAM

