



SSD201

Smart HD Display Controller

Preliminary Data Sheet Version 0.4



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REVISION HISTORY

Revision No.	Description	Date
0.1	• Initial release	05/16/2019
0.2	• Updated Pin #50	07/19/2019
0.3	• Updated Pin #36, 37, 125 and 126	08/15/2019
0.4	• Added AC/DC Specifications	03/06/2020

FEATURES

- **High Performance Processor Core**
 - ARM Cortex-A7 Dual Core up to 1.2GHz
 - 32KB I-Cache/32KB D-Cache/256KB L2-Cache
 - Neon and FPU
 - Memory Management Unit for Linux support
 - DMA Engine
- **H.264/AVC Decoder**
 - Variable block size (16x16, 16x8, 8x16, 8x8, 8x4, 4x8 and 4x4)
 - CABAC/CAVLC support
 - Error detection, concealment and error resilience tools
 - Supports max. resolution FHD (1920x1080) with 60fps decode
- **H.265/HEVC Decoder**
 - I/P/B slices
 - All intra-prediction modes
 - All inter-prediction modes
 - Variable CTU size: 64x64 to 16x16
 - Variable Prediction Unit (PU) size: 64x64 to 4x4
 - Variable Transform Unit (TU) size: 32x32 to 4x4
 - High performance CABAC decoding
 - Sample Adaptive Offset (SAO)
 - Robust error concealment
 - Supports max. resolution FHD (1920x1080) with 60fps decode
- **JPEG Encoder**
 - Supports JPEG baseline encoding
 - Supports YUV422 or YUV420 formats
 - Supports max. resolution FHD (1920x1080) with 15fps
- **Display Subsystem**
 - Supports multi-window (max. 4 + 1 PIP) fetch, merge, and scale-up function
 - Built-in contrast, brightness, sharpness, and saturation control
 - TTL output up to HD 60fps with RGB565 or RGB666 or RGB888 format
- **MIPI TX DSI**
 - MIPI TX DSI 4-lane with max. 1.5Gbps and output up to FHD 60fps
- **2D Graphics Engine**
 - Line draw
 - Rectangle/gradient rectangle fill
 - Bitblt/Stretch Bitblt/Italic Bitblt
 - Palette mode (1/2/4/8-bit)
 - Format transformation
 - Color space conversion
 - Clipping
 - Alpha blending
 - Rotation/Mirror
 - Dither
- **Audio Processor**
 - One mono ADC for microphone input
 - Two stereo DMIC inputs
 - One stereo DAC for lineout
 - Supports 8K/16K/32K/48KHz sampling rate audio recording
 - ADC Pre-Amp gain supports 0dB, 6dB, 13dB, 23dB, 30dB, and 36dB
 - ADC boost gain supports -6dB ~ 15dB or 0dB ~ 21dB with interval 3dB
 - ADC digital gain supports -63.5dB ~ 33dB with interval 0.5dB, can be muted to zero
 - SNR of DR A-Weighted ADC > 90dB (@gain = 0dB)
- **NOR/NAND Flash Interface**
 - Supports 1/2/4-bit SPI-NOR / NAND (with ECC) flash with two chip selects
- **SDIO 2.0 Interface**
 - Compatible with SDIO spec. 2.0, data bus 1/4 bit mode
 - Compatible with SD spec. 2.0, data bus 1/4 bit mode

■ **USB 2.0 Interface**

- Two high-speed USB2.0 hosts
- Connects to external mouse, Wi-Fi, AI chip or hard disk

■ **DRAM Memory**

- Supports 16-bit 512Mb DDR2 memory with max. 1333Mbps
- One embedded DDR2 memory
- Supports ODT function
- Supports auto-refresh and self-refresh mode

■ **Ethernet**

- Supports two Ethernet ports
- Supports 10/100Mbps half/full-duplex
- One built-in 10/100M Ethernet PHY
- Supports one RMII to connect external PHY
- Supports two LEDs for ePHY

■ **Security Engines**

- Supports AES/DES/3DES/RSA/SHA-I/SHA-256
- Supports secure booting

■ **Real Time Clock (RTC)**

- Built-in RTC working with 32.768 KHz crystal
- Tick time interrupt (millisecond)
- Supports ultra-low power (<3uA) RTC-mode for long battery application

■ **Peripherals**

- Dedicated GPIOs for system control
- Four PWM outputs
- Three generic UARTs and one fast UART with flow control
- Three generic timers and one watchdog timer
- One SPI master
- Two I2C masters
- One IR input

■ **Miscellaneous**

- Built-in efuse with 1024-bit to store device ID, AES key, chip configurations, etc.
- Built-in power on reset (POR)
- Built-in SAR ADC with 3-channel analog inputs for different kinds of applications

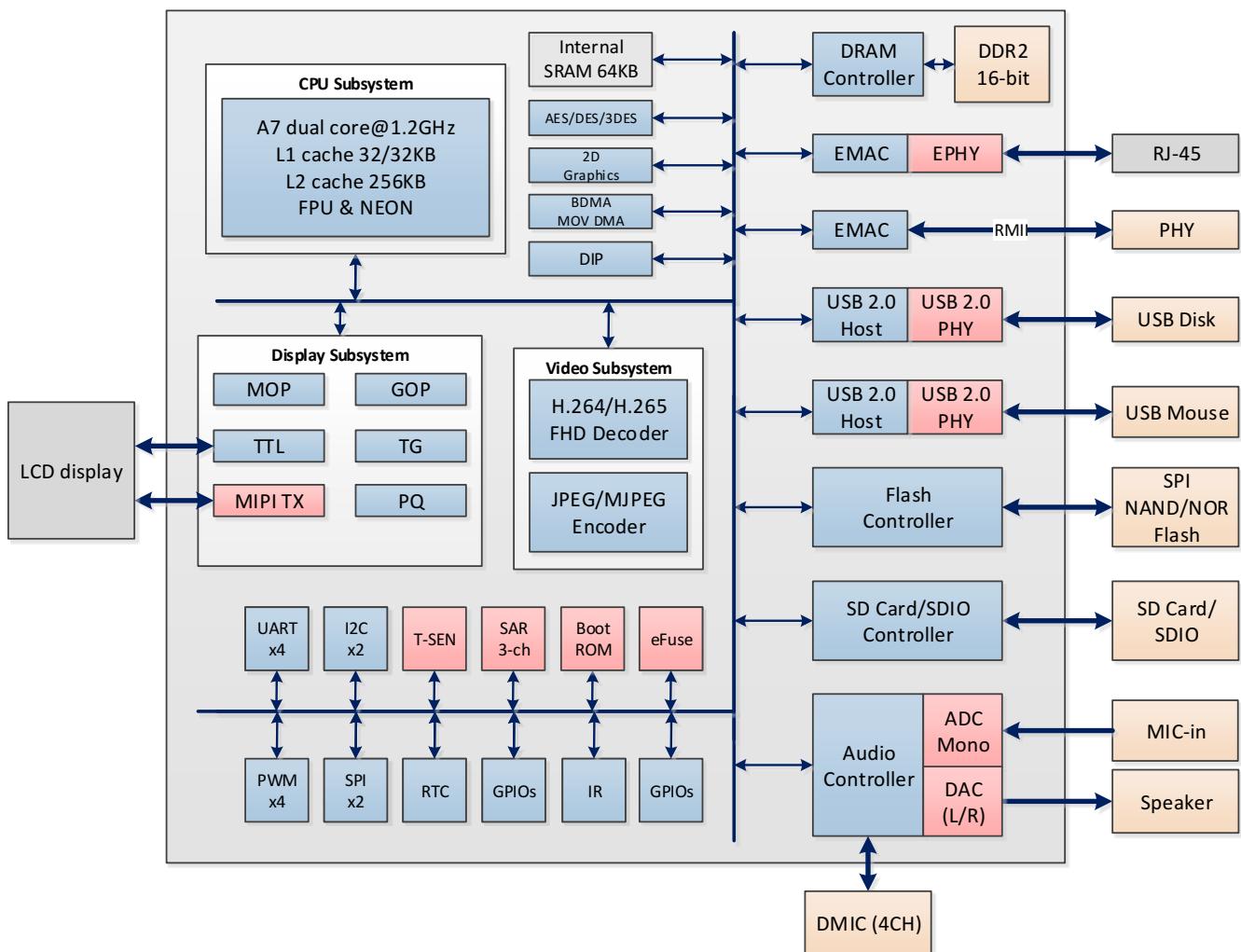
■ **Operating Voltage Range**

- Core: 0.9V
- I/O: 1.8V ~ 3.3V
- DRAM: 1.8V
- Power Consumption: TBD.
- Operation temperature -20°C ~ 85°C

■ **Package**

- 128-pin QFN, 12.3mm x 12.3mm

BLOCK DIAGRAM



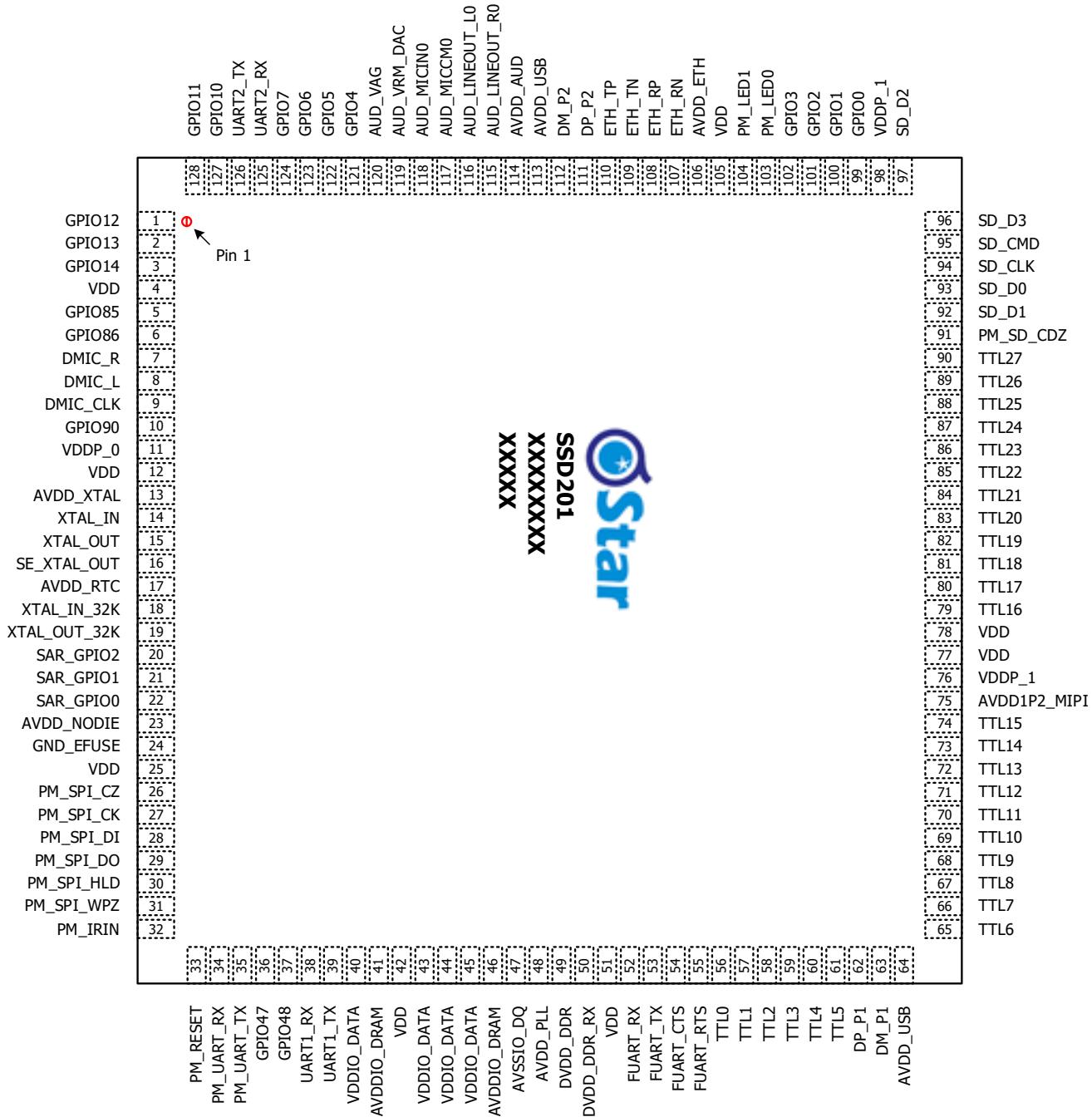
GENERAL DESCRIPTION

The SSD201 is a highly integrated SOC. Based on ARM Cortex-A7 dual-core, it integrates H.264/H.265 video decoder, 2D graphics engine, TTL/MIPI display with adjustable picture quality engine and other useful peripherals for smart display applications.

A typical utilization of the SSD201 application processor is demonstrated in the block diagram. The completed system includes a connectivity module (Wi-Fi or Ethernet), and a non-volatile storage (NOR flash, NAND flash or SD card). External crystal of 32KHz frequency is used to drive the Real Time Clock (RTC), which can keep time scale when the main system clock is off. The H.264/H.265 engine decodes video streams from network and sends them to the display sub-system. Before outputting to TTL or MIPI TX panel, the images can be enhanced with respect to brightness/contrast/saturation/sharpness to give the best picture quality. The NOR or NAND flash is usually reserved for operating system and application software. Moreover, other peripherals like SAR ADC, Audio ADC/DAC, UARTs, PWMs, GPIOs and SPI are supported to realize applications with maximal flexibility.

Besides, the SSD201 supports secure booting and personalization authentication mechanism for securing system. The AES/DES/3DES cipher engines could also help encrypt the compressed video/audio streams to protect privacy.

PIN DIAGRAM



SIGNAL DESCRIPTION

Signal Name	Signal Type	Function	QFN128 Pin Location
System Reset Interface			
PM_RESET	I	System Reset (Active High)	33
Debug UART Interface			
PM_UART_RX	I	Debug UART Receive Data Input with Pull Up Resistor / Slave I2C Serial Clock	34
PM_UART_TX	O	Debug UART Transmit Data Output with Pull Up Resistor / Slave I2C Serial Data	35
System Interface			
XTAL_IN	I	24MHz Crystal Input	14
XTAL_OUT	O	24MHz Crystal Output	15
XTAL_IN_32K	I	32.768KHz Crystal Input	18
XTAL_OUT_32K	O	32.768KHz Crystal Output	19
SE_XTAL_OUT	O	24MHz Clock Output	16
SPI Flash Interface			
PM_SPI_CZ	O	SPI Flash Chip Select (Active Low)	26
PM_SPI_DI	O	SPI Flash Serial Data To Device (MOSI)	28
PM_SPI_WPZ	O	SPI Flash Write Protect	31
PM_SPI_DO	I	SPI Flash Serial Data From Device (MISO)	29
PM_SPI_CK	O	SPI Flash Clock	27
PM_SPI_HLD	O	SPI Flash Hold	30
PM GPIO Interface			
PM_IRIN	I	General Purpose Input/Output Infrared Input from IR Receiver	32
SAR ADC Interface			
SAR_GPIO0	I	General Purpose Input/Output or Muxed to SARADC Input Channel 0	22
SAR_GPIO1	I	General Purpose Input/Output or Muxed to SARADC Input Channel 1	21
SAR_GPIO2	I	General Purpose Input/Output or Muxed to SARADC Input Channel 2	20
GPIO Interface			

Signal Name	Signal Type	Function	QFN128 Pin Location
GPIO0	I/O	General Purpose Input/Output 0	99
GPIO1	I/O	General Purpose Input/Output 1	100
GPIO2	I/O	General Purpose Input/Output 2	101
GPIO3	I/O	General Purpose Input/Output 3	102
GPIO4	I/O	General Purpose Input/Output 4	121
GPIO5	I/O	General Purpose Input/Output 5	122
GPIO6	I/O	General Purpose Input/Output 6	123
GPIO7	I/O	General Purpose Input/Output 7	124
GPIO10	I/O	General Purpose Input/Output 10	127
GPIO11	I/O	General Purpose Input/Output 11	128
GPIO12	I/O	General Purpose Input/Output 12	1
GPIO13	I/O	General Purpose Input/Output 13	2
GPIO14	I/O	General Purpose Input/Output 14	3
GPIO47	I/O	General Purpose Input/Output 47	36
GPIO48	I/O	General Purpose Input/Output 48	37
GPIO85	I/O	General Purpose Input/Output 85	5
GPIO86	I/O	General Purpose Input/Output 86	6
GPIO90	I/O	General Purpose Input/Output 90	10
UART Interface			
UART1_RX	I	UART 1 Receive Data Input	38
UART1_TX	O	UART 1 Transmit Data Output	39
UART2_RX	I	UART 2 Receive Data Input	125
UART2_TX	O	UART 2 Transmit Data Output	126
Fast UART Interface			
FUART_RX	I	Fast UART Receive Data Input	52
FUART_TX	O	Fast UART Transmit Data Output	53
FUART_CTS	I	Fast UART Clear to Send	54
FUART_RTS	O	Fast UART Request to Send	55
10/100M Ethernet Interface			
ETH_RN	I	10/100M Ethernet Differential Pair of Receiver Signal Negative	107
ETH_RP	I	10/100M Ethernet Differential Pair of Receiver Signal Positive	108
ETH_TN	O	10/100M Ethernet Differential Pair of Transmitter Signal Negative	109

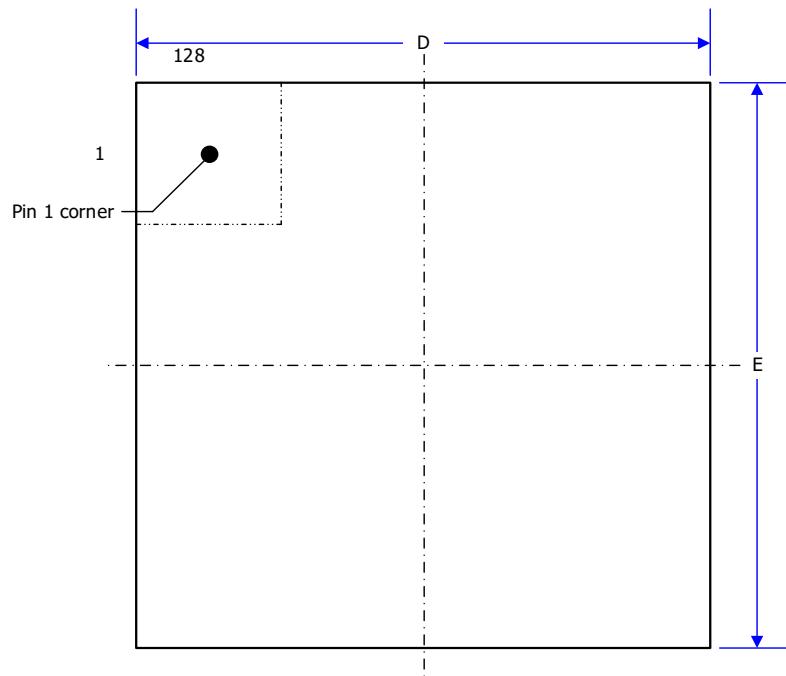
Signal Name	Signal Type	Function	QFN128 Pin Location
ETH_TP	O	10/100M Ethernet Differential Pair of Transmitter Signal Positive	110
PM_LED0	O	10/100M Ethernet LED0 Control Driven Active When Linked	103
PM_LED1	O	10/100M Ethernet LED1 Control Driven Active When Linked in 100 Base-TX and Blinking When Transmitting or Receiving Data	104
SD 2.0 Card Interface			
SD_CLK	O	SD 2.0 Clock	94
SD_CMD	O	SD 2.0 Command	95
SD_D0	I/O	SD 2.0 Data Bus 0	93
SD_D1	I/O	SD 2.0 Data Bus 1	92
SD_D2	I/O	SD 2.0 Data Bus 2	97
SD_D3	I/O	SD 2.0 Data Bus 3	96
PM_SD_CDZ	I	Power Manage SD 2.0 Card Detect	91
Line Out Interface			
AUD_LINEOUT_L0	O	Audio Left Channel Line Output	116
AUD_LINEOUT_R0	O	Audio Right Channel Line Output	115
AUD_VAG	O	Audio Reference Voltage from 1/2 AVDD_AUD	120
AUD_VRM_DAC	I	Audio Reference Voltage for DAC	119
Analog Microphone Interface			
AUD_MICINO	I	Audio Left Channel Microphone Positive Input	118
AUD_MICCM0	I	Audio Left Channel Microphone Negative Input	117
USB 2.0 Interface			
DM_P1	I/O	USB 2.0 Differential Pair, Negative	63
DP_P1	I/O	USB 2.0 Differential Pair, Positive	62
DM_P2	I/O	USB 2.0 Differential Pair, Negative	112
DP_P2	I/O	USB 2.0 Differential Pair, Positive	111
Parallel LCD Interface			
TTL0	O	Parallel LCD Data 0	56
TTL1	O	Parallel LCD Data 1	57
TTL2	O	Parallel LCD Data 2	58
TTL3	O	Parallel LCD Data 3	59
TTL4	O	Parallel LCD Data 4	60
TTL5	O	Parallel LCD Data 5	61

Signal Name	Signal Type	Function	QFN128 Pin Location
TTL6	O	Parallel LCD Data 6	65
TTL7	O	Parallel LCD Data 7	66
TTL8	O	Parallel LCD Data 8	67
TTL9	O	Parallel LCD Data 9	68
TTL10	O	Parallel LCD Data 10	69
TTL11	O	Parallel LCD Data 11	70
TTL12	O	Parallel LCD Data 12	71
TTL13	O	Parallel LCD Data 13	72
TTL14	O	Parallel LCD Data 14	73
TTL15	O	Parallel LCD Data 15	74
TTL16	O	Parallel LCD Data 16	79
TTL17	O	Parallel LCD Data 17	80
TTL18	O	Parallel LCD Data 18	81
TTL19	O	Parallel LCD Data 19	82
TTL20	O	Parallel LCD Data 20	83
TTL21	O	Parallel LCD Data 21	84
TTL22	O	Parallel LCD Data 22	85
TTL23	O	Parallel LCD Data 23	86
TTL24	O	Parallel LCD Data 24	87
TTL25	O	Parallel LCD Data 25	88
TTL26	O	Parallel LCD Data 26	89
TTL27	O	Parallel LCD Data 27	90
DMIC Interface			
DMIC_R	O	Digital Microphone Right	7
DMIC_L	I/O	Digital Microphone Left	8
DMIC_CLK	I	Digital Microphone Clock	9
Power pins			
VDD	Core Power	Digital Core Power	4, 12, 25, 42, 51, 77, 78, 105
VDDP_0	3.3V Power	Digital Power for VDDP_0 Group	11
VDDP_1	3.3V Power	Digital Power for VDDP_1 Group	76, 98
DVDD_DDR_RX	O	LDO output for DDR (Cap to GND)	50
DVDD_DDR	Core Power	Digital Power for DDR TX	49
VDDIO_DATA	DDR Power	Analog Power for DDR MCLK/DATA	40, 43, 44, 45

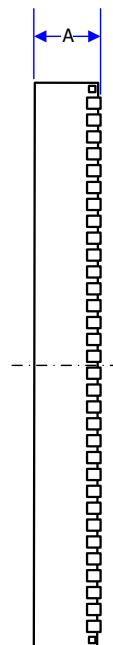
Signal Name	Signal Type	Function	QFN128 Pin Location
AVDDIO_DRAM	DDR Power	Stack DRAM Power	41, 46
AVDD1P2_MIPI	O	LDO Output for MIPI TX (Cap To GND)	75
AVDD_NODIE	3.3V Power	Analog Power for PM	23
AVDD_PLL	3.3V Power	Analog Power for PLL	48
AVDD_XTAL	3.3V Power	Analog Power for XTAL	13
AVDD_RTC	3.3V Power	Analog Power for RTC	17
AVDD_USB	3.3V Power	Analog Power for USB Port 1	64
AVDD_USB	3.3V Power	Analog Power for USB Port 2/3	113
AVDD_ETH	3.3V Power	Analog Power for Ethernet	106
AVDD_AUD	3.3V Power	Analog Power for Audio	114
GND_EFUSE	I	Power Source if eFuse is Burnt (Connected to Ground)	24
AVSSIO_DQ	GND	GND for AVSSIO_DQ	47
GND	GND	Digital Ground	ePad

MECHANICAL DIMENSIONS

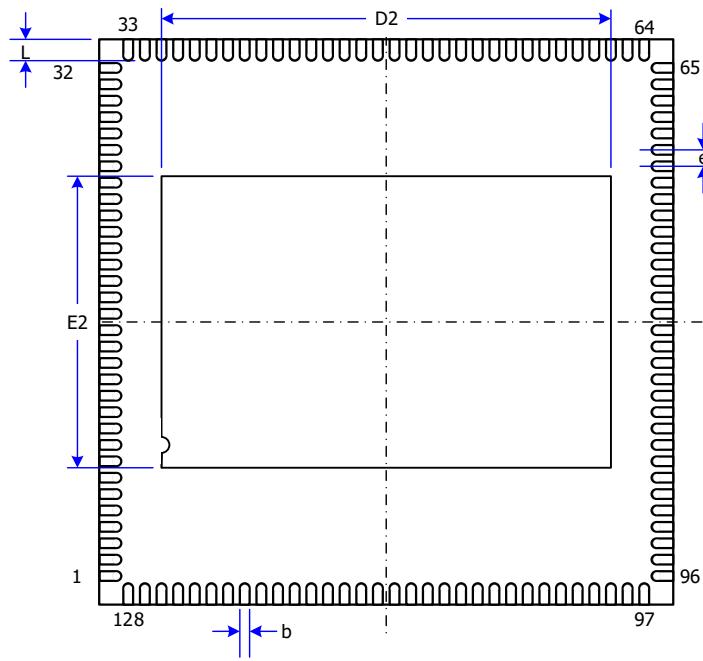
Top View



Side View



Bottom View



ELECTRICAL SPECIFICATIONS

Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
DIGITAL INPUTS					
Input Voltage, High	V _{IH}	2.5			V
Input Voltage, Low	V _{IL}			0.8	V
Input Current, High	I _{IH}			-1.0	uA
Input Current, Low	I _{IL}			1.0	uA
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Output Voltage, High	V _{OH}	VDDP-0.1 <small>Note</small>			V
Output Voltage, Low	V _{OL}			0.1	V
SAR ADC Input		0		V _{VDD_33}	V
AUDIO OUTPUTS					
Line-Out			2.54		V _{p-p}
XTAL Specifications					
Input Voltage, High	V _{IH}	2.0		3.6	V
Input Voltage, Low	V _{IL}	-0.3		0.8	V
Clock frequency			24		MHz
Crystal accuracy			+/-30		ppm
Long-term jitter			+/-500		ps

Note: 1. VDDP can be V_{VDD_33}, V_{VDD_15}

2. 0.9VRMS @10Kohm load

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V _{VDD_33}	3.14	3.3	3.46	V
1.8V Supply Voltage (DDR II)	V _{VDD_18}	1.71	1.8	1.89	V
Core Power Supply Voltage (Core)	V _{VDD_core}	0.87	0.9	0.93	V
Ambient Operation Temperature	T _A	-20		85	°C
Junction Temperature	T _J			125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V _{VDD_33}	2.97	3.3	3.63	V
1.8V Supply Voltage (DDR II)	V _{VDD_18}			1.98	V
Core Power Supply Voltage (Core)	V _{VDD_core}			1.1	V
Storage Temperature	T _{STG}	-40		150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

AC/DC SPECIFICATIONS

USB Interface

USB Full Speed DC Characteristics

Parameter	Min	Typ	Max	Unit
Input Levels				
Differential Receiver Input Sensitivity	0.2			V
Single-Ended Receiver Low Level Input Voltage			0.8	V
Single-Ended Receiver High Level Input Voltage	2.0			V
Output Levels				
Low Level Output Voltage			0.3	V
High Level Output Voltage	2.8			V
Termination				
Driver Output Impedance	40.5		49.5	Ω
Pull-up Resistor Impedance (Idle Bus)	0.9		1.575	kΩ
Pull-up Resistor Impedance (Upstream Port Receiving)	1.425		3.090	kΩ
Pull-down Resistor Impedance	14.25		24.80	kΩ

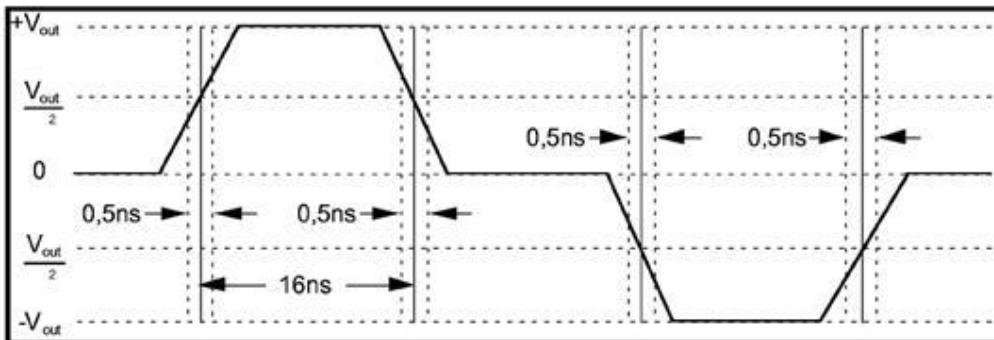
USB High Speed DC Characteristics

Parameter	Min	Typ	Max	Unit
Input Levels				
Differential Receiver Input Sensitivity	100			mV
Squelch Detection Threshold	100		150	mV
Output Levels				
Low Level Output Voltage (45Ω Load)	-10		10	mV
High Level Output Voltage (45Ω Load)	360		440	mV
Termination				
Driver Output Impedance	40.5		49.5	Ω

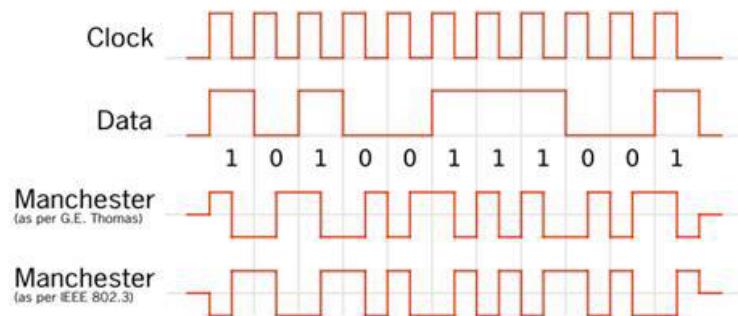
EPHY Interface

Parameter	Min	Typ	Max	Unit
ETHERNET ANALOG INTERFACE (10BASE-T)				
Analog Input Range	4.4	5	5.6	Vdp-p
Differential Input Impedance		100		ohm
ETHERNET ANALOG INTERFACE (100BASE-TX)				
Analog Input Range	1.9	2	2.1	Vdp-p
Differential Input Impedance		100		ohm
Rise/Fall Time	3	4	5	ns
Rise/Fall Time Symmetry		0.5		ns
Duty Cycle Distortion	-0.25		0.25	ns
Amplitude Symmetry	98	100	102	%
Overshoot		5		%

100BASE-TX



10BASE-T

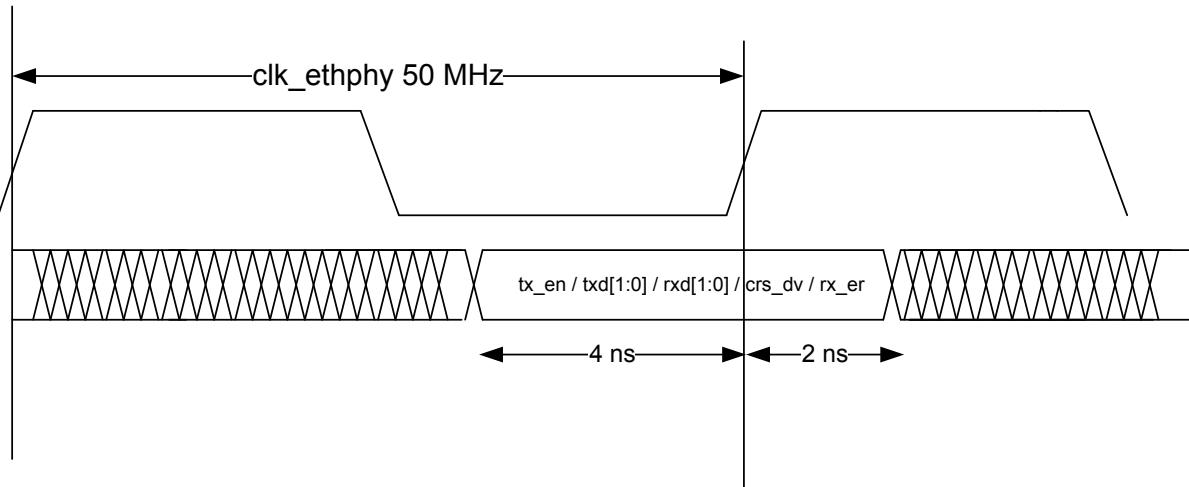


RMII interface

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
	REF_CLK Frequency		50		MHz
	REF_CLK Duty Cycle	35		65	%
Tsu	TXD[1:0], TX_EN, RXD[1:0], CRS_DV, RX_ER Data Setup to REF_CLK Rising Edge	4			ns
Thold	TXD[1:0], TX_EN, RXD[1:0], CRS_DV, RX_ER Data Hold from REF_CLK Rising Edge	2			ns

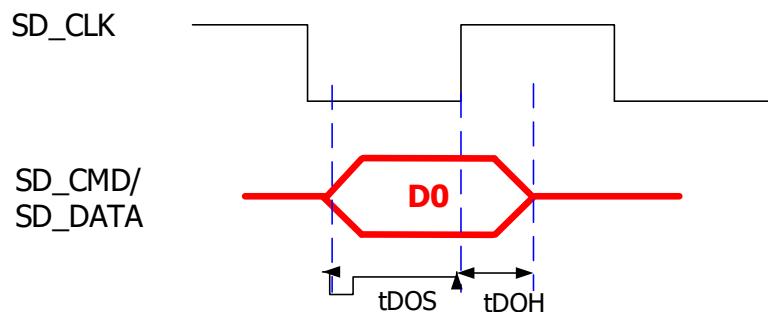
RMII Timing



SDIO Interface

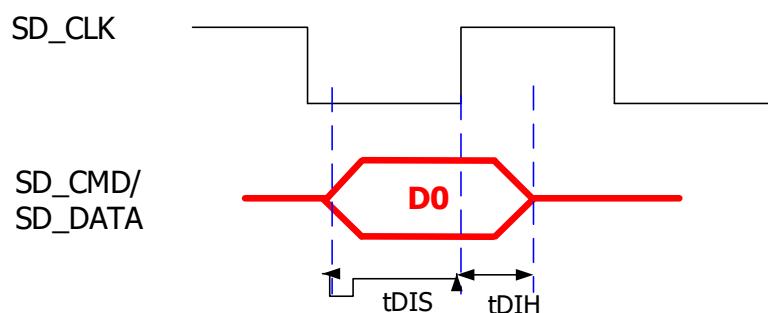
Data Output (TX) Timing

Symbol	Parameter	Min	Max	Unit	Remarks
tDOS	Data Output Setup Time	6	-	ns	
tDOH	Data Output Hold Time	6	-	ns	



Data Input (RX) Timing

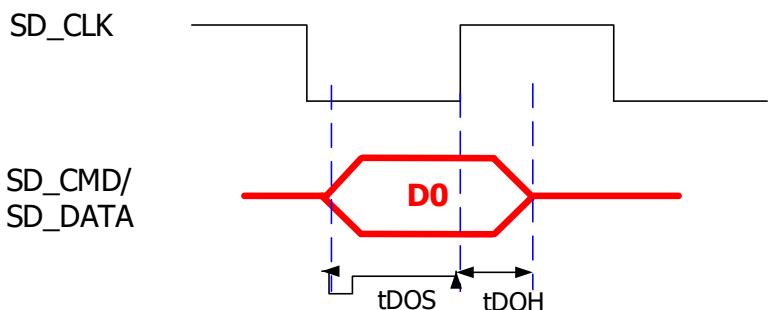
Symbol	Parameter	Min	Max	Unit	Remarks
tDIS	Data Input Setup Time	6	-	ns	
tDIH	Data Input Hold Time	1.5	-	ns	



SD Card Interface

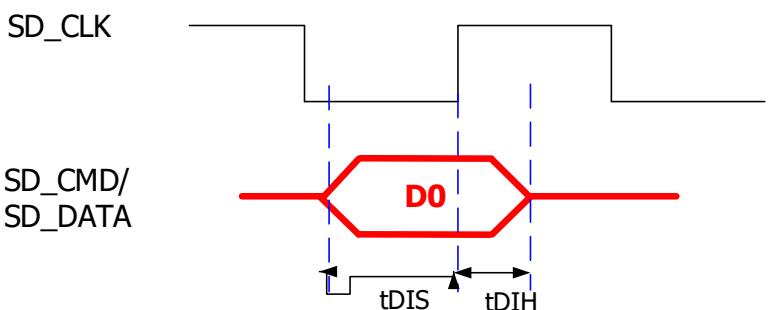
Data Output (TX) Timing

Symbol	Parameter	Min	Max	Unit	Remarks
tDOS	Data Output Setup Time	6	-	ns	
tDOH	Data Output Hold Time	6	-	ns	



Data Input (RX) Timing

Symbol	Parameter	Min	Max	Unit	Remarks
tDIS	Data Input Setup Time	6	-	ns	
tDIH	Data Input Hold Time	1.5	-	ns	



Audio Interface

Stereo Audio-DAC Interface

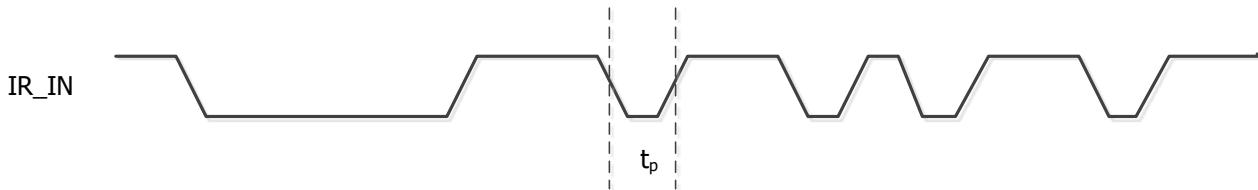
Parameter	Min	Typ	Max	Unit
Frequency Response (20KHz)	-1.0	0	+0.1	dB
THD+N (1KHz sine-wave; -3dBFS) [dB, non A-weighted]		-80		dB
S/N-ratio [dB, A-weighted]		92		dB
Dynamic-range [dB, A-weighted]		92		dB
Crosstalk (1KHz sine-wave: full scale)		-90		dB
Analog Output Level (1KHz sine-wave: full scale)		1		Vrms
Load Impedance		1000		ohm

Stereo Audio-ADC Interface

Parameter	Min	Typ	Max	Unit
THD+N (1KHz sine-wave; -3dBFS) [dB, non A-weighted]		-80		dB
S/N-ratio [dB, A-weighted]		90		dB
Dynamic Range [dB, A-weighted]		90		dB
Crosstalk (1KHz sine-wave: full scale)		-85		dB
Analog Input Range (-1.4dBFS)		1		Vrms

IR Receiver Interface

AC Timing Diagram



IR SW Mode

Parameter	Symbol	Standard Mode		Unit
		Min.	Max.	
Pulse Width	t_p	1.0	20000.0	us

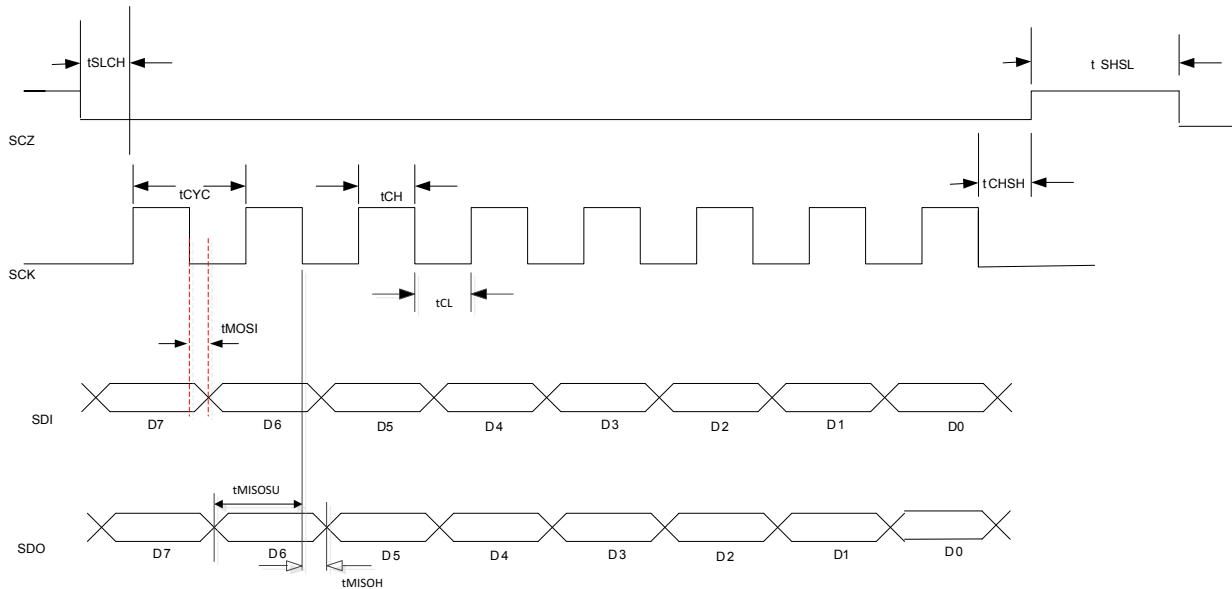
SAR Interface

SAR ADC DC Spec

Parameter	Min	Typ	Max	Unit
SAR ADC Input	0		AVDD_NODIE	V

SPI NOR Interface

SPI Data Timing - CSZ, SCK, SDI and SDO



SPI AC Characteristics for Operation

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
CS High	tSHSL	1		15	ns	
CS Setup	tSLCH	1		15	ns	
CS Hold	tCHSH	1		15	ns	
SCK period	tCYC	9.3			ns	
SCK High Time	tCH	45	50	55	%	
SCK Low Time	tCL	45	50	55	%	
Master Out Slave In	tMOSI	-2		(tCYC/2)-2	ns	Relative to the falling edge of SCK
Master In Slave Out Setup time	tMISOSU	4.6			ns	Relative to the falling edge of SCK
Master In Slave Out Hold time	tMISOH	0.3			ns	Relative to the falling edge of SCK

SPI DC Characteristics for Operation

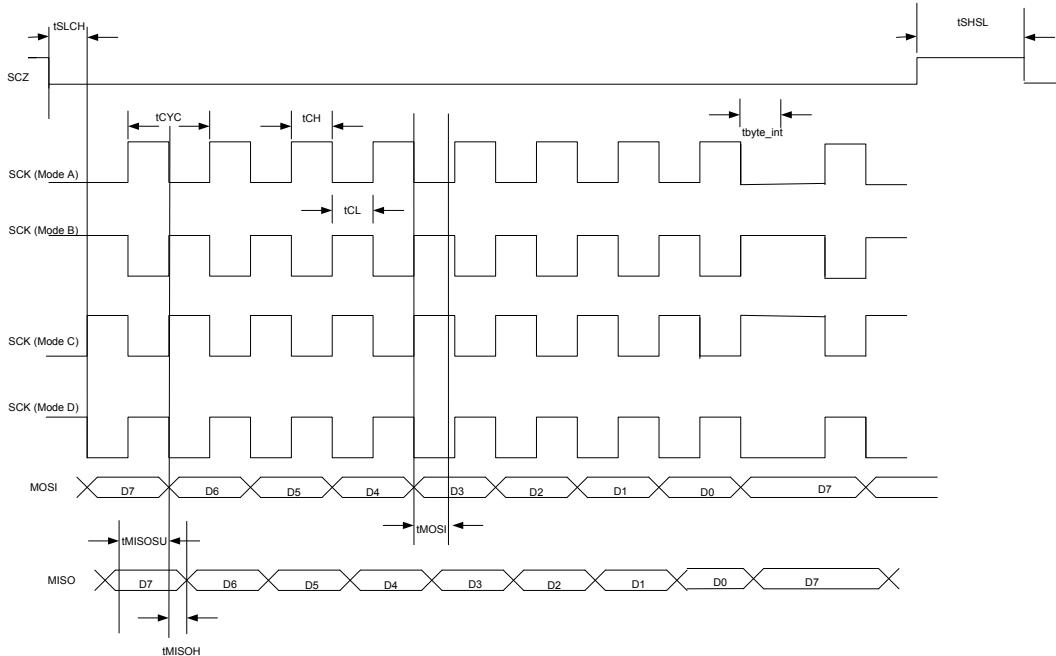
Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Input Low Voltage	VIL			0.9	V	
Input High Voltage	VIH	2.0			V	

MSPI Interface

AC Characteristics

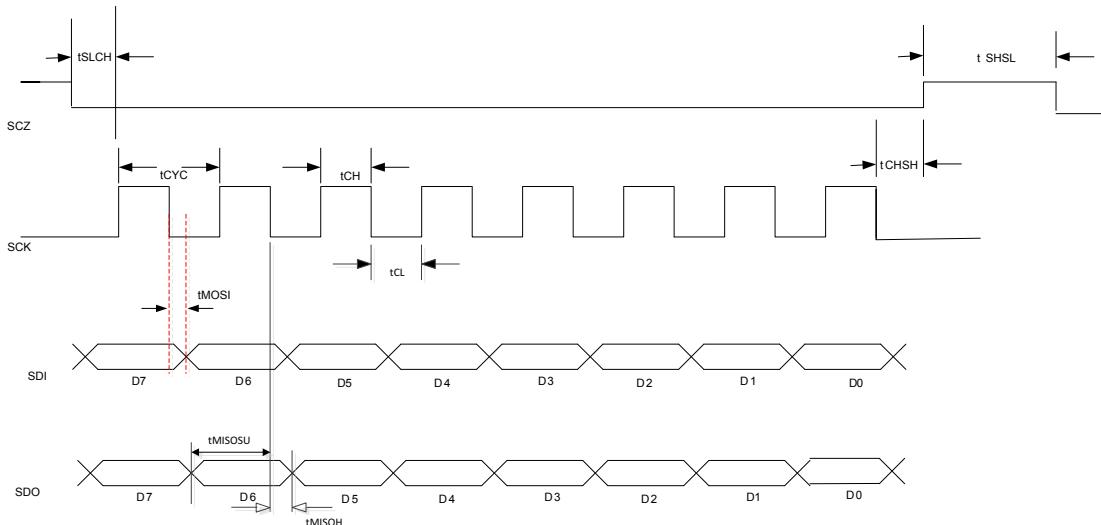
Parameter	Symbol	Min	Max	Unit	Remarks
SCZ Active Setup Time Relative to SCK	tSLCH	4	255	cycle	1 cycle = tCYC
SCZ Deselect Time	tSHSL	4.5	255	cycle	1 cycle = tCYC
SCK Period Time	tCYC	37.1		ns	
SCK High Time	tCH	tCYC/2		ns	
SCK Low Time	tCL	tCYC/2		ns	
Master Out Slave In	tMOSI	5-(tCYC/2)	(tCYC/2)-2	ns	Relative to the falling edge of SCK
Master In Slave Out Setup Time	tMISOSU	6		ns	Relative to the falling edge of SCK
Master In Slave Out Hold Time	tMISOH	0.3		ns	Relative to the falling edge of SCK
Byte Interval	tbyte_int	0	255	cycle	1 cycle = tCYC

Mode A/B/C/D



SPI NAND Interface

SPI Data Timing - CSZ, SCK, SDI and SDO



SPI AC Characteristics for Operation

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
CS High	tSHSL	1		15	tCYC	
CS Setup	tSLCH	1		15	tCYC	
CS Hold	tCHSH	1		15	tCYC	
SCK period	tCYC	9.3			ns	
SCK High Time	tCH	45	50	55	%	
SCK Low Time	tCL	45	50	55	%	
Master Out Slave In	tMOSI	-2		(tCYC/2)-2	ns	Relative to the falling edge of SCK
Master In Slave Out Setup time	tMISOSU	4.6			ns	Relative to the falling edge of SCK
Master In Slave Out Hold time	tMISOH	0.3			ns	Relative to the falling edge of SCK

SPI DC Characteristics for Operation

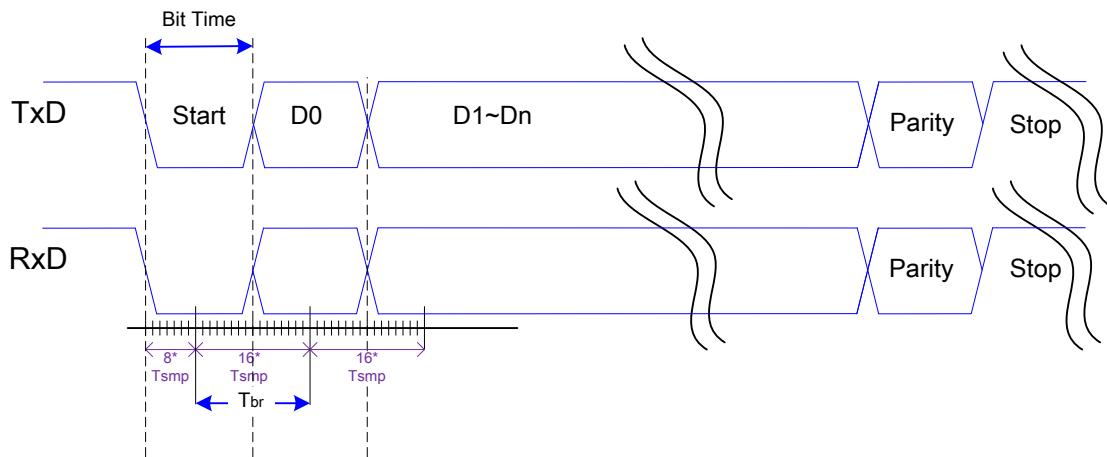
Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Input Low Voltage	VIL			0.9	V	
Input High Voltage	VIH	2.0			V	

UART Interface

AC Characteristics

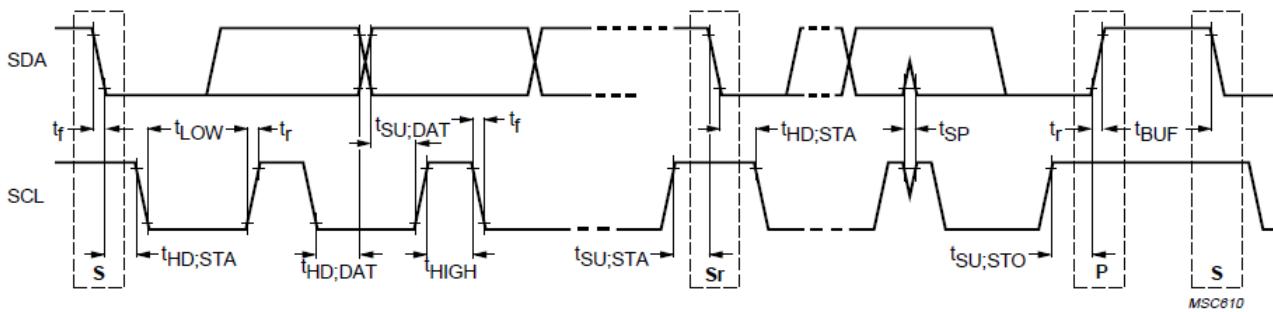
Parameter	Symbol	Min	Typ	Max	Unit
Baud Rate Period	Tbr		115200		bps
UART Sampling Period	Tsmp		1/16		Tbr

TxD/RxD Timing



I2C Interface

AC Timing Diagram



Standard Mode

Parameter	Symbol	Standard mode		Unit
		Min	Max	
Clock Frequency	fSCL	-	100	kHz
Re-start Hold Time	tHD;STA	4	-	µs
SCL Low Period	tLOW	4.7	-	µs
SCL High Period	tHIGH	4.0	-	µs
RE-start Set-up Time	tSU;STA	4.7	-	µs
SDA Hold Time	tHD;DAT	5	-	µs
SDA Set-up Time	tSU;DAT	250	-	ns
Rise Time of Signals	tr	-	1000	ns
Fall Time of Signals	tf	-	300	ns
STOP Set-up Time	tSU;STO	4.0	-	µs
Bus Free High Time between STOP and START Condition	tBUF	4.7	-	µs

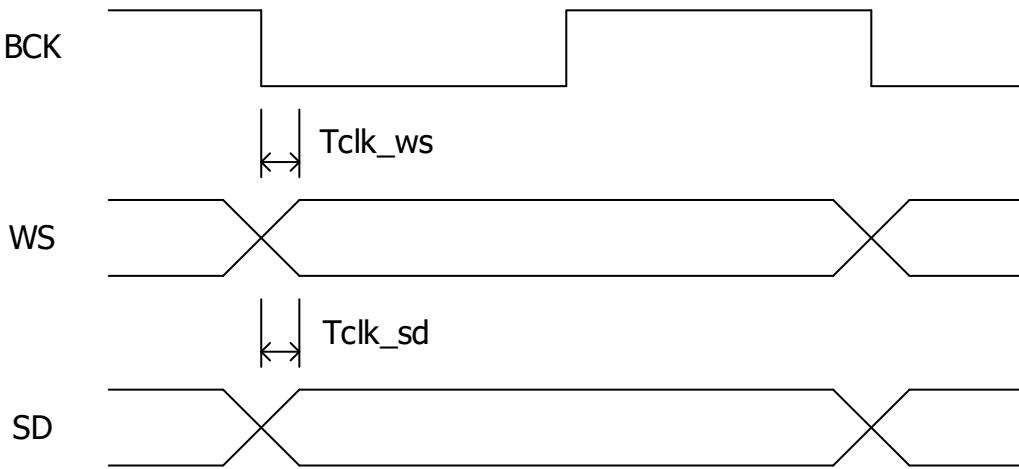
Fast Mode

Parameter	Symbol	Fast mode		Unit
		Min	Max	
Clock Frequency	fSCL	-	400	kHz
Re-start Hold Time	tHD;STA	0.6	-	μs
SCL Low Period	tLOW	1.3	-	μs
SCL High Period	tHIGH	0.6	-	μs
RE-start Set-up Time	tSU;STA	0.6	-	μs
SDA Hold Time	tHD;DAT	0	0.9-	μs
SDA Set-up Time	tSU;DAT	100	-	ns
Rise Time of Signals	tr	20+0.1Cb	300	ns
Fall Time of Signals	tf	20+0.1Cb	300	ns
STOP Set-up Time	tSU;STO	0.6	-	μs
Bus Free High Time between STOP and START Condition	tBUF	1.3	-	μs

Note: Cb = total capacitance of one bus line in pF

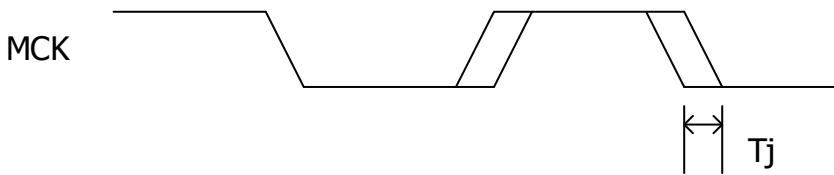
I2S Interface

I2S Audio Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
Edge of BCK to Changing WS	T_{clk_ws}	-8	-	8	ns
Edge of BCK to Changing SD	T_{clk_sd}	-8	-	8	ns
BCK Duty Cycle	-	-	50	-	%
BCK Period (FS = 48KHz)	-	-	326	-	ns
BCK Frequency (FS = 48KHz)	-	-	3.072	-	MHz

256FS Audio Clock Output Timing



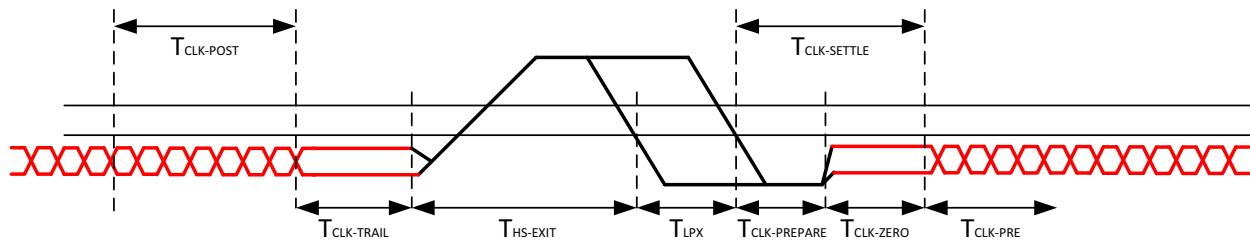
Parameter	Symbol	Min	Typ	Max	Unit
MCK Period (FS = 48KHz)	-	-	81.38	-	ns
MCK Frequency (FS = 48KHz)	-	-	12.288	-	MHz
Jitter	T_j	-	-	2	ns

Video DAC Interface

Parameter	Min	Typ	Max	Unit
VIDEO ANALOG OUTPUT				
CVBS/S-Video/YPbPr Output				
Output Low	0			V
Output High	1.3			V

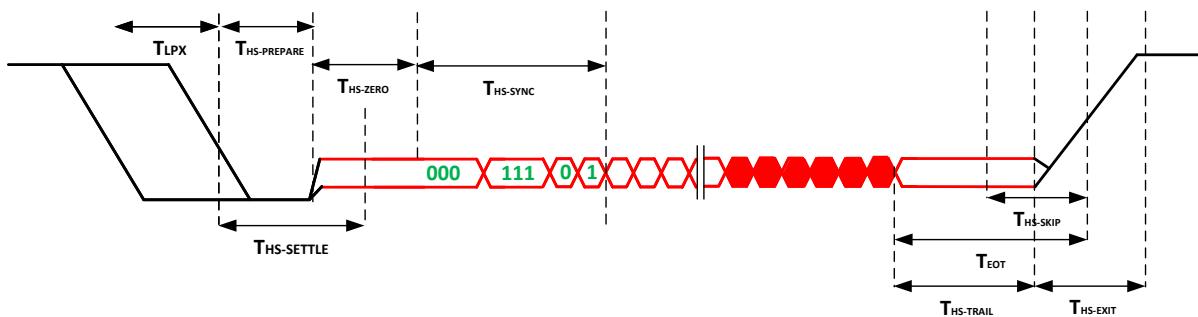
MIPI Interface

Clock Lane



Symbol	Description	Min	Max	Unit
UI	As HS differential data unit	0.83	12.5	ns
T _{CLK-POST}	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	-	60	ns
T _{LPX}	Transmitted length of any Low-Power state period	50	-	ns
T _{CLK_PREPARE}	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	95	ns
T _{CLK-ZERO}	Time that the transmitter drives the HS-0 state prior to starting the Clock.	262	-	ns
T _{CLK-PRE}	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8		UI
T _{CLK-SETTLE}	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-prepare.	95	300	ns
T _{HS-EXIT}	Time that the transmitter drives LP-11 following a HS burst.	100		ns
T _{CLK-TRAIL}	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60		ns

Data Lane



Symbol	Description	Min	Max	Unit
UI	As HS single data unit	0.83	12.5	ns
T _{HS-SKIP}	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	55 ns + 4*UI	ns
T _{LPX}	Transmitted length of any Low-Power state period	50	-	ns
T _{HS-PREPARE}	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	40 ns + 4*UI	85ns + 6*UI	ns
T _{HS-ZERO}	Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	105 ns + 10*UI	-	ns
T _{HS-SYNC}	Time that the HS Start-of-Transmission (SoT) procedure shall transmit '00011101' as sync pattern.	8 * UI	UI	
T _{HS-settle}	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns + 6*UI	145 ns + 10*UI	ns
T _{HS-EXIT}	Time that the transmitter drives LP-11 following a HS burst.	100		ns
T _{HS-TRAIL}	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	Max(8*UI, 60 ns + 4UI)		ns
T _{EOT}	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.	105 ns + 12*UI		ns

HARDWARE POWER SEQUENCE PROCEDURE

The timing requirements of the hardware reset signal are shown as below:

Hardware Reset

HWRESET: Chip Reset; High Reset (Level)

The HWRESET pin is suggested to connect with 3.3V standby as shown in Figure 1. The VIH is 2V (Typ) +/- 10% (2.2V~1.8V); the VIL is 1.2V (Typ) +/- 10% (1.08V~1.32V). The power sequence is as shown in Figure 2.

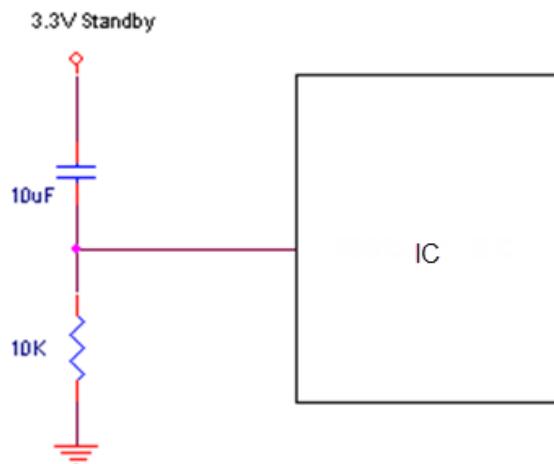
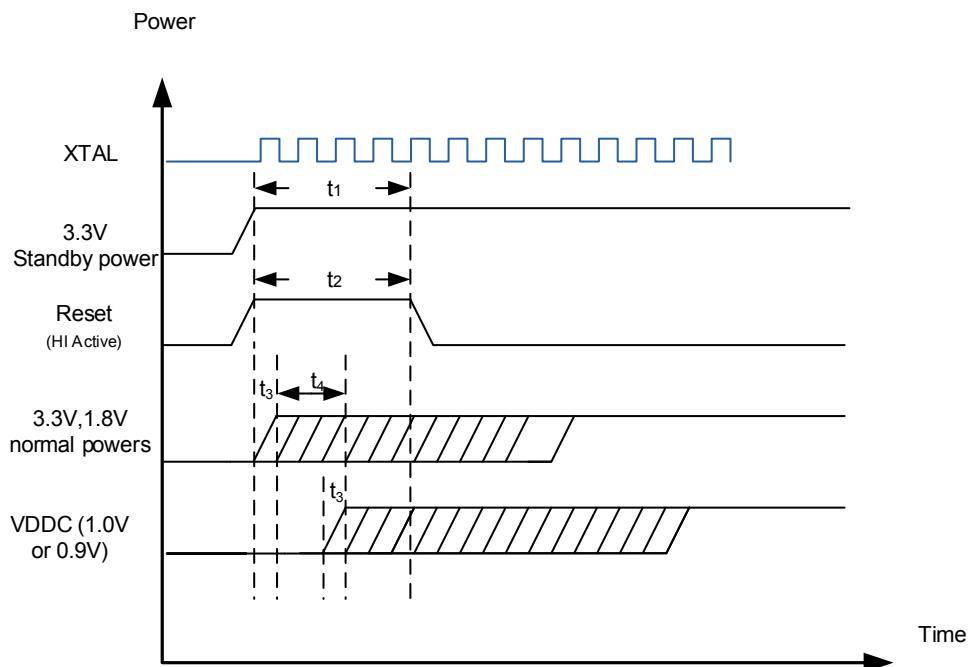


Figure 1: Reset Application Circuit

External Reset IC with External LDO

The timing is shown as Figure 2. The RST and power waveform must satisfy Figure 2 with parameters listed in Table 1.



Note:

- *3.3V standby power (AVDD_NODIE, AVDD_XTAL, AVDD_ETH)
- *1.0V/0.9V (VDD)
- *1.8V (AVDDIO_DRAM, VDDIO_DATA, VDDIO_CMD)
- *3.3V normal power (AVDD_AUD, AVDD_PLL, AVDD_USB, VDDP_1, VDDP_3)

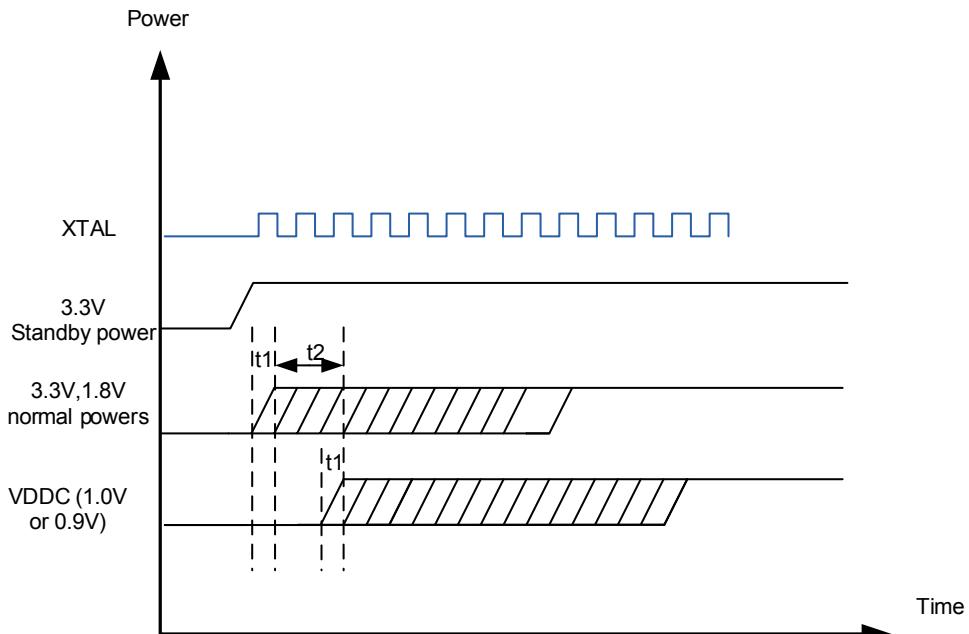
Figure 2: Power on Sequence

Table 1: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t ₁	XTAL stable to Reset falling	5	—	—	ms
t ₂	Reset pulse width	5	—	—	ms
t ₃	Normal 3.3V, 1.8V, and VDDC power rising time (0% to 100%)	—	—	20	ms
t ₄	Normal 3.3V and 1.8V to VDDC lead time	1	—	—	ms

Without External Reset IC with External LDO

The timing is shown as Figure 3. The power waveform must satisfy Figure 3 with parameters listed in Table 1.



Note:

- ***3.3V standby power (AVDD_NODIE, AVDD_XTAL, AVDD_ETH)**
- ***1.0V/0.9V (VDD)**
- ***1.8V (AVDDIO_DRAM, VDDIO_DATA, VDDIO_CMD)**
- ***3.3V normal power (AVDD_AUD, AVDD_PLL, AVDD_USB, VDDP_1, VDDP_3)**

Figure 3: Power on Sequence

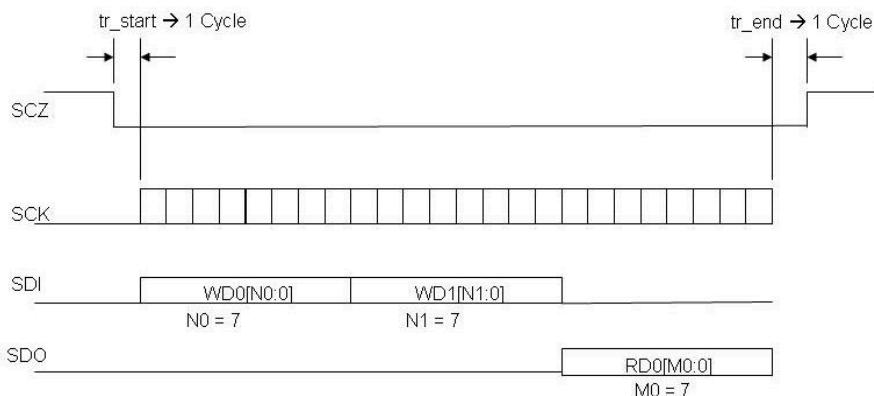
Table 2: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t_1	Normal 3.3V, 1.8V, and VDDC power rising time (0% to 100%)	—	—	20	ms
t_2	Normal 3.3V and 1.8V to VDDC lead time	1	—	—	ms

MSPI OPERATION EXAMPLE

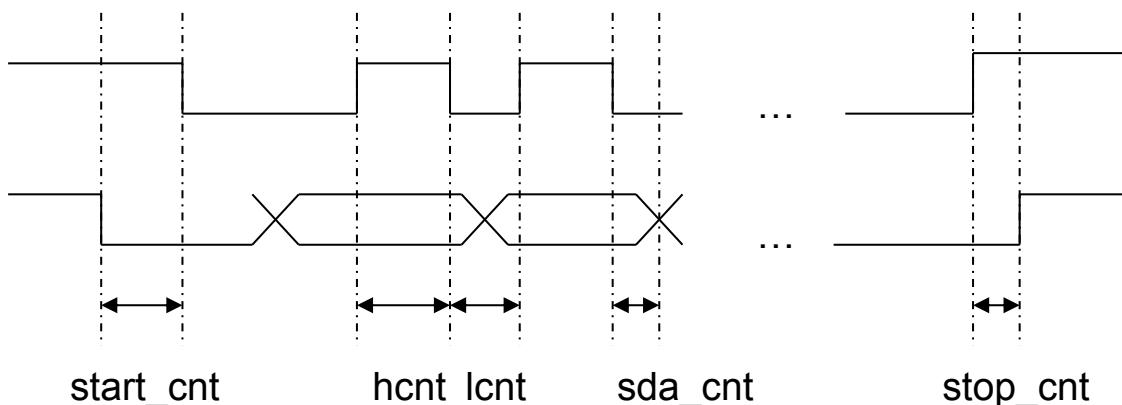
This section describes an example of MSPI operation.

- (0). Initial
- (1). CS goes low
- (2). Write 2Bytes data
- (3). Read 1Bytes data
- (4). CS goes high



I2C clock frequency configurable is between 100Khz ~ 400Khz

Set MIIC Speed



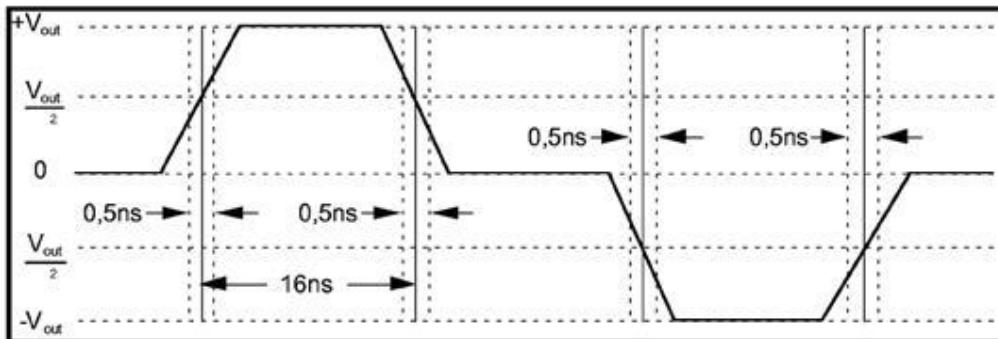
clk_miic	12MHz	24MHz
lcnt (>1.3us)	>16T	>31T
hcnt (>0.6us)	>8T	>15T
start (>0.6us)	>8T	>15T
stop (>0.6us)	>8T	>15T
between start and stop (>1.3us)	>16T	>31T
data_latch (>0us)	>0T	>0T
sda change (<0.9us)	<11T	<22T

Register name	Address	Description
reg_stop_cnt	'h08[15:0]	Sets the SCL and SDA count for stop
reg_hcnt	'h09[15:0]	Sets the SCL clock high-period count
reg_lcnt	'h0a[15:0]	Sets the SCL clock low-period count
reg_sda_cnt	'h0b[15:0]	Sets the clock count between falling edge SCL and SDA
reg_start_cnt	'h0c[15:0]	Sets the SCL and SDA count for start
reg_data_lat_cnt	'h0d[15:0]	Sets the data latch timing

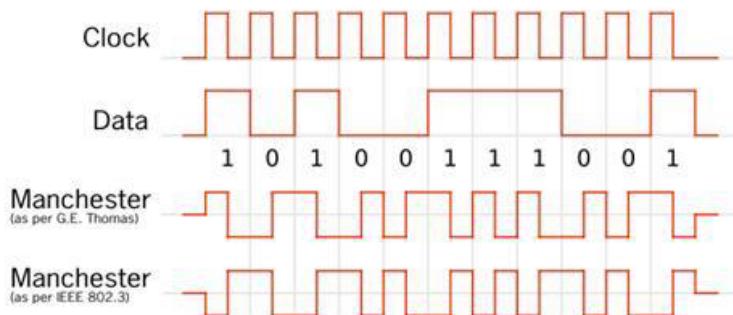
EPHY INTERFACE

Parameter	Min	Typ	Max	Unit
ETHERNET ANALOG INTERFACE (10BASE-T)				
Analog Input Range	4.4	5	5.6	Vdp-p
Differential Input Impedance		100		ohm
ETHERNET ANALOG INTERFACE (100BASE-TX)				
Analog Input Range	1.9	2	2.1	Vdp-p
Differential Input Impedance		100		ohm
Rise/Fall Time	3	4	5	ns
Rise/Fall Time Symmetry			0.5	ns
Duty Cycle Distortion	-0.25		0.25	ns
Amplitude Symmetry	98	100	102	%
Overshoot			5	%

100BASE-TX



10BASE-T

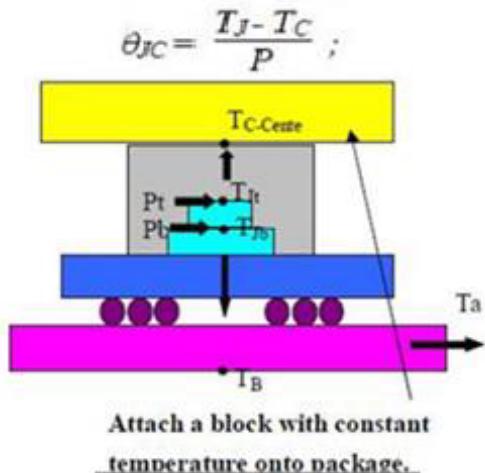


THERMAL RESISTANCE (°C/W)

Thermal simulation mode

1. PCB conditions (JEDEC JESD51-5)
2. PCB layers: 2L (1S1P)
3. PCB dimensions (mm x mm): 76.2 x 114.3
4. PCB thickness (mm): 1.6

PKG Type	PKG Size (mm) / Pin Count	PCB Layer	Theta jc (C/W)	Theta jb (C/W)	Ta (C)	Tj (C)	Theta ja (C/W)
QFN	12.3x12.3 / 128L	2L	6.9	10.82	75	125	22.6





ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
SSD201	-20°C to +85°C	QFN	128-pin

MARKING INFORMATION

SSD201

DISCLAIMER

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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. SSD201 comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.



PM CH3 REGISTER TABLE

PM_POR_STATUS Register (Bank = 06)

PM_POR_STATUS Register (Bank = 06)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (0600h)	REG0600	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_0[7:0]	7:0	PM power status 0.	
00h (0601h)	REG0601	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_0[15:8]	7:0	See description of '0600h'.	
01h (0602h)	REG0602	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_1[7:0]	7:0	PM power status 1.	
01h (0603h)	REG0603	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_1[15:8]	7:0	See description of '0602h'.	
02h (0604h)	REG0604	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_2[7:0]	7:0	PM power status 2.	
02h (0605h)	REG0605	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_2[15:8]	7:0	See description of '0604h'.	
03h (0606h)	REG0606	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_3[7:0]	7:0	PM power status 3.	
03h (0607h)	REG0607	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_3[15:8]	7:0	See description of '0606h'.	
04h (0608h)	REG0608	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_4[7:0]	7:0	PM power status 4.	
04h (0609h)	REG0609	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_4[15:8]	7:0	See description of '0608h'.	
05h (060Ah)	REG060A	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_5[7:0]	7:0	PM power status 5.	
05h (060Bh)	REG060B	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_5[15:8]	7:0	See description of '060Ah'.	
06h (060Ch)	REG060C	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_6[7:0]	7:0	PM power status 6.	
06h (060Dh)	REG060D	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_6[15:8]	7:0	See description of '060Ch'.	
07h	REG060E	7:0	Default : 0x00	Access : R/W



PM_POR_STATUS Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
(060Eh)	PM_POR_STATUS_7[7:0]	7:0	PM power status 7.	
07h (060Fh)	REG060F	7:0	Default : 0x00	Access : R/W
	PM_POR_STATUS_7[15:8]	7:0	See description of '060Eh'.	

PM_GPIO Register (Bank = 0F)

PM_GPIO Register (Bank = 0F)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (0F00h)	REG0F00	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_0	7	GPIO_0's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_0	6	GPIO_0's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_0	5	GPIO_0's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_0	4	GPIO_0's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_0	3	GPIO_0's glitch remover enable.	
	GPIO_PM_IN_0	2	GPIO_0's input.	
	GPIO_PM_OUT_0	1	GPIO_0's output.	
	GPIO_PM_OEN_0	0	GPIO_0's output enable.	
00h (0F01h)	REG0F01	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_0	7	GPIO_0's PAD PS.	
	GPIO_PM_PAD_PE_0	6	GPIO_0's PAD PE.	
	GPIO_PM_PAD_DRV1_0	5	GPIO_0's PAD DRV1.	
	GPIO_PM_PAD_DRV0_0	4	GPIO_0's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_0	1	GPIO_0's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_0	0	GPIO_0's FIQ final status for edge wake-up source.	
01h (0F02h)	REG0F02	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_1	7	GPIO_1's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_1	6	GPIO_1's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_1	5	GPIO_1's FIQ force for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
01h (0F03h)	GPIO_PM_WK_FIQ_MASK_1	4	GPIO_1's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_1	3	GPIO_1's glitch remover enable.	
	GPIO_PM_IN_1	2	GPIO_1's input.	
	GPIO_PM_OUT_1	1	GPIO_1's output.	
	GPIO_PM_OEN_1	0	GPIO_1's output enable.	
02h (0F04h)	REG0F03	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_1	7	GPIO_1's PAD PS.	
	GPIO_PM_PAD_PE_1	6	GPIO_1's PAD PE.	
	GPIO_PM_PAD_DRV1_1	5	GPIO_1's PAD DRV1.	
	GPIO_PM_PAD_DRV0_1	4	GPIO_1's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_1	1	GPIO_1's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_1	0	GPIO_1's FIQ final status for edge wake-up source.	
02h (0F05h)	REG0F04	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_2	7	GPIO_2's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_2	6	GPIO_2's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_2	5	GPIO_2's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_2	4	GPIO_2's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_2	3	GPIO_2's glitch remover enable.	
	GPIO_PM_IN_2	2	GPIO_2's input.	
	GPIO_PM_OUT_2	1	GPIO_2's output.	
	GPIO_PM_OEN_2	0	GPIO_2's output enable.	
	REG0F05	7:0	Default : 0x00	Access : RO, R/W

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	TATUS_2			
03h (0F06h)	REG0F06	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_3	7	GPIO_3's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_3	6	GPIO_3's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_3	5	GPIO_3's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_3	4	GPIO_3's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_3	3	GPIO_3's glitch remover enable.	
	GPIO_PM_IN_3	2	GPIO_3's input.	
	GPIO_PM_OUT_3	1	GPIO_3's output.	
	GPIO_PM_OEN_3	0	GPIO_3's output enable.	
03h (0F07h)	REG0F07	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_3	7	GPIO_3's PAD PS.	
	GPIO_PM_PAD_PE_3	6	GPIO_3's PAD PE.	
	GPIO_PM_PAD_DRV1_3	5	GPIO_3's PAD DRV1.	
	GPIO_PM_PAD_DRV0_3	4	GPIO_3's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_3	1	GPIO_3's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_3	0	GPIO_3's FIQ final status for edge wake-up source.	
04h (0F08h)	REG0F08	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_4	7	GPIO_4's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_4	6	GPIO_4's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_4	5	GPIO_4's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_4	4	GPIO_4's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_4	3	GPIO_4's glitch remover enable.	
	GPIO_PM_IN_4	2	GPIO_4's input.	
	GPIO_PM_OUT_4	1	GPIO_4's output.	
	GPIO_PM_OEN_4	0	GPIO_4's output enable.	
04h (0F09h)	REG0F09	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_4	7	GPIO_4's PAD PS.	
	GPIO_PM_PAD_PE_4	6	GPIO_4's PAD PE.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
05h (0F0Ah)	GPIO_PM_PAD_DRV1_4	5	GPIO_4's PAD DRV1.	
	GPIO_PM_PAD_DRV0_4	4	GPIO_4's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_4	1	GPIO_4's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_4	0	GPIO_4's FIQ final status for edge wake-up source.	
	REG0FOA	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_5	7	GPIO_5's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_5	6	GPIO_5's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_5	5	GPIO_5's FIQ force for edge wake-up source.	
05h (0F0Bh)	GPIO_PM_WK_FIQ_MASK_5	4	GPIO_5's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_5	3	GPIO_5's glitch remover enable.	
	GPIO_PM_IN_5	2	GPIO_5's input.	
	GPIO_PM_OUT_5	1	GPIO_5's output.	
	GPIO_PM_OEN_5	0	GPIO_5's output enable.	
	REG0FOB	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_5	7	GPIO_5's PAD PS.	
	GPIO_PM_PAD_PE_5	6	GPIO_5's PAD PE.	
	GPIO_PM_PAD_DRV1_5	5	GPIO_5's PAD DRV1.	
06h (0F0Ch)	GPIO_PM_PAD_DRV0_5	4	GPIO_5's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_5	1	GPIO_5's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_5	0	GPIO_5's FIQ final status for edge wake-up source.	
	REG0FOC	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_6	7	GPIO_6's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_6	6	GPIO_6's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_6	5	GPIO_6's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_6	4	GPIO_6's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_6	3	GPIO_6's glitch remover enable.	



PM_GPIO Register (Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_IN_6	2	GPIO_6's input.	
	GPIO_PM_OUT_6	1	GPIO_6's output.	
	GPIO_PM_OEN_6	0	GPIO_6's output enable.	
06h (0F0Dh)	REG0F0D	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_6	7	GPIO_6's PAD PS.	
	GPIO_PM_PAD_PE_6	6	GPIO_6's PAD PE.	
	GPIO_PM_PAD_DRV1_6	5	GPIO_6's PAD DRV1.	
	GPIO_PM_PAD_DRV0_6	4	GPIO_6's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_6	1	GPIO_6's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_6	0	GPIO_6's FIQ final status for edge wake-up source.	
07h (0F0Eh)	REG0F0E	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_7	7	GPIO_7's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_7	6	GPIO_7's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_7	5	GPIO_7's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_7	4	GPIO_7's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_7	3	GPIO_7's glitch remover enable.	
	GPIO_PM_IN_7	2	GPIO_7's input.	
	GPIO_PM_OUT_7	1	GPIO_7's output.	
	GPIO_PM_OEN_7	0	GPIO_7's output enable.	
07h (0F0Fh)	REG0F0F	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_7	7	GPIO_7's PAD PS.	
	GPIO_PM_PAD_PE_7	6	GPIO_7's PAD PE.	
	GPIO_PM_PAD_DRV1_7	5	GPIO_7's PAD DRV1.	
	GPIO_PM_PAD_DRV0_7	4	GPIO_7's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_7	1	GPIO_7's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_7	0	GPIO_7's FIQ final status for edge wake-up source.	
08h	REG0F10	7:0	Default : 0x11	Access : RO, R/W, WO

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description
(0F10h)	GPIO_PM_WK_FIQ_POL_8	7	GPIO_8's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_8	6	GPIO_8's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_8	5	GPIO_8's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_8	4	GPIO_8's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_8	3	GPIO_8's glitch remover enable.
	GPIO_PM_IN_8	2	GPIO_8's input.
	GPIO_PM_OUT_8	1	GPIO_8's output.
	GPIO_PM_OEN_8	0	GPIO_8's output enable.
08h (0F11h)	REG0F11	7:0	Default : 0x00
	GPIO_PM_PAD_PS_8	7	GPIO_8's PAD PS.
	GPIO_PM_PAD_PE_8	6	GPIO_8's PAD PE.
	GPIO_PM_PAD_DRV1_8	5	GPIO_8's PAD DRV1.
	GPIO_PM_PAD_DRV0_8	4	GPIO_8's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_8	1	GPIO_8's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_8	0	GPIO_8's FIQ final status for edge wake-up source.
09h (0F12h)	REG0F12	7:0	Default : 0x11
	GPIO_PM_WK_FIQ_POL_9	7	GPIO_9's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_9	6	GPIO_9's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_9	5	GPIO_9's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_9	4	GPIO_9's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_9	3	GPIO_9's glitch remover enable.
	GPIO_PM_IN_9	2	GPIO_9's input.
	GPIO_PM_OUT_9	1	GPIO_9's output.
	GPIO_PM_OEN_9	0	GPIO_9's output enable.
09h (0F13h)	REG0F13	7:0	Default : 0x00
	GPIO_PM_PAD_PS_9	7	GPIO_9's PAD PS.
	GPIO_PM_PAD_PE_9	6	GPIO_9's PAD PE.
	GPIO_PM_PAD_DRV1_9	5	GPIO_9's PAD DRV1.
	GPIO_PM_PAD_DRV0_9	4	GPIO_9's PAD DRV0.

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_9	1	GPIO_9's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_9	0	GPIO_9's FIQ final status for edge wake-up source.
0Ah (0F14h)	REG0F14	7:0	Default : 0x11
	GPIO_PM_WK_FIQ_POL_10	7	GPIO_10's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_10	6	GPIO_10's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_10	5	GPIO_10's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_10	4	GPIO_10's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_10	3	GPIO_10's glitch remover enable.
	GPIO_PM_IN_10	2	GPIO_10's input.
	GPIO_PM_OUT_10	1	GPIO_10's output.
	GPIO_PM_OEN_10	0	GPIO_10's output enable.
0Ah (0F15h)	REG0F15	7:0	Default : 0x00
	GPIO_PM_PAD_PS_10	7	GPIO_10's PAD PS.
	GPIO_PM_PAD_PE_10	6	GPIO_10's PAD PE.
	GPIO_PM_PAD_DRV1_10	5	GPIO_10's PAD DRV1.
	GPIO_PM_PAD_DRV0_10	4	GPIO_10's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_10	1	GPIO_10's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_10	0	GPIO_10's FIQ final status for edge wake-up source.
0Bh (0F16h)	REG0F16	7:0	Default : 0x11
	GPIO_PM_WK_FIQ_POL_11	7	GPIO_11's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_11	6	GPIO_11's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_11	5	GPIO_11's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_11	4	GPIO_11's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_11	3	GPIO_11's glitch remover enable.
	GPIO_PM_IN_11	2	GPIO_11's input.

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_OUT_11	1	GPIO_11's output.	
	GPIO_PM_OEN_11	0	GPIO_11's output enable.	
0Bh (0F17h)	REG0F17	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_11	7	GPIO_11's PAD PS.	
	GPIO_PM_PAD_PE_11	6	GPIO_11's PAD PE.	
	GPIO_PM_PAD_DRV1_11	5	GPIO_11's PAD DRV1.	
	GPIO_PM_PAD_DRV0_11	4	GPIO_11's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_11	1	GPIO_11's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_11	0	GPIO_11's FIQ final status for edge wake-up source.	
0Ch (0F18h)	REG0F18	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_12	7	GPIO_12's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_12	6	GPIO_12's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_12	5	GPIO_12's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_12	4	GPIO_12's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_12	3	GPIO_12's glitch remover enable.	
	GPIO_PM_IN_12	2	GPIO_12's input.	
	GPIO_PM_OUT_12	1	GPIO_12's output.	
	GPIO_PM_OEN_12	0	GPIO_12's output enable.	
0Ch (0F19h)	REG0F19	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_12	7	GPIO_12's PAD PS.	
	GPIO_PM_PAD_PE_12	6	GPIO_12's PAD PE.	
	GPIO_PM_PAD_DRV1_12	5	GPIO_12's PAD DRV1.	
	GPIO_PM_PAD_DRV0_12	4	GPIO_12's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_12	1	GPIO_12's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_12	0	GPIO_12's FIQ final status for edge wake-up source.	
0Dh	REG0F1A	7:0	Default : 0x11	Access : RO, R/W, WO

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description
(0F1Ah)	GPIO_PM_WK_FIQ_POL_13	7	GPIO_13's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_13	6	GPIO_13's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_13	5	GPIO_13's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_13	4	GPIO_13's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_13	3	GPIO_13's glitch remover enable.
	GPIO_PM_IN_13	2	GPIO_13's input.
	GPIO_PM_OUT_13	1	GPIO_13's output.
	GPIO_PM_OEN_13	0	GPIO_13's output enable.
0Dh (0F1Bh)	REG0F1B	7:0	Default : 0x00
	GPIO_PM_PAD_PS_13	7	GPIO_13's PAD PS.
	GPIO_PM_PAD_PE_13	6	GPIO_13's PAD PE.
	GPIO_PM_PAD_DRV1_13	5	GPIO_13's PAD DRV1.
	GPIO_PM_PAD_DRV0_13	4	GPIO_13's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_13	1	GPIO_13's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_13	0	GPIO_13's FIQ final status for edge wake-up source.
0Eh (0F1Ch)	REG0F1C	7:0	Default : 0x11
	GPIO_PM_WK_FIQ_POL_14	7	GPIO_14's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_14	6	GPIO_14's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_14	5	GPIO_14's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_14	4	GPIO_14's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_14	3	GPIO_14's glitch remover enable.
	GPIO_PM_IN_14	2	GPIO_14's input.
	GPIO_PM_OUT_14	1	GPIO_14's output.
0Eh (0F1Dh)	REG0F1D	7:0	Default : 0x00
	GPIO_PM_PAD_PS_14	7	GPIO_14's PAD PS.
	GPIO_PM_PAD_PE_14	6	GPIO_14's PAD PE.

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
0Fh (0F1Eh)	GPIO_PM_PAD_DRV1_14	5	GPIO_14's PAD DRV1.	
	GPIO_PM_PAD_DRV0_14	4	GPIO_14's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_14	1	GPIO_14's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_14	0	GPIO_14's FIQ final status for edge wake-up source.	
	REG0F1E	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_15	7	GPIO_15's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_15	6	GPIO_15's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_15	5	GPIO_15's FIQ force for edge wake-up source.	
0Fh (0F1Fh)	GPIO_PM_WK_FIQ_MASK_15	4	GPIO_15's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_15	3	GPIO_15's glitch remover enable.	
	GPIO_PM_IN_15	2	GPIO_15's input.	
	GPIO_PM_OUT_15	1	GPIO_15's output.	
	GPIO_PM_OEN_15	0	GPIO_15's output enable.	
	REG0F1F	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_15	7	GPIO_15's PAD PS.	
	GPIO_PM_PAD_PE_15	6	GPIO_15's PAD PE.	
	GPIO_PM_PAD_DRV1_15	5	GPIO_15's PAD DRV1.	
10h (0F20h)	GPIO_PM_PAD_DRV0_15	4	GPIO_15's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_15	1	GPIO_15's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_15	0	GPIO_15's FIQ final status for edge wake-up source.	
	REG0F20	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_16	7	GPIO_16's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_16	6	GPIO_16's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_16	5	GPIO_16's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_16	4	GPIO_16's FIQ mask for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description
10h (0F21h)	GPIO_PM_GLHRM_EN_16	3	GPIO_16's glitch remover enable.
	GPIO_PM_IN_16	2	GPIO_16's input.
	GPIO_PM_OUT_16	1	GPIO_16's output.
	GPIO_PM_OEN_16	0	GPIO_16's output enable.
11h (0F22h)	REG0F21	7:0	Default : 0x00
	GPIO_PM_PAD_PS_16	7	GPIO_16's PAD PS.
	GPIO_PM_PAD_PE_16	6	GPIO_16's PAD PE.
	GPIO_PM_PAD_DRV1_16	5	GPIO_16's PAD DRV1.
	GPIO_PM_PAD_DRV0_16	4	GPIO_16's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_16	1	GPIO_16's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_16	0	GPIO_16's FIQ final status for edge wake-up source.
11h (0F23h)	REG0F22	7:0	Default : 0x11
	GPIO_PM_WK_FIQ_POL_17	7	GPIO_17's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_17	6	GPIO_17's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_17	5	GPIO_17's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_17	4	GPIO_17's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_17	3	GPIO_17's glitch remover enable.
	GPIO_PM_IN_17	2	GPIO_17's input.
	GPIO_PM_OUT_17	1	GPIO_17's output.
	GPIO_PM_OEN_17	0	GPIO_17's output enable.
11h (0F23h)	REG0F23	7:0	Default : 0x00
	GPIO_PM_PAD_PS_17	7	GPIO_17's PAD PS.
	GPIO_PM_PAD_PE_17	6	GPIO_17's PAD PE.
	GPIO_PM_PAD_DRV1_17	5	GPIO_17's PAD DRV1.
	GPIO_PM_PAD_DRV0_17	4	GPIO_17's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_17	1	GPIO_17's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_17	0	GPIO_17's FIQ final status for edge wake-up source.

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	TATUS_17			
12h (0F24h)	REG0F24	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_18	7	GPIO_18's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_18	6	GPIO_18's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_18	5	GPIO_18's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_18	4	GPIO_18's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_18	3	GPIO_18's glitch remover enable.	
	GPIO_PM_IN_18	2	GPIO_18's input.	
	GPIO_PM_OUT_18	1	GPIO_18's output.	
	GPIO_PM_OEN_18	0	GPIO_18's output enable.	
12h (0F25h)	REG0F25	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_18	7	GPIO_18's PAD PS.	
	GPIO_PM_PAD_PE_18	6	GPIO_18's PAD PE.	
	GPIO_PM_PAD_DRV1_18	5	GPIO_18's PAD DRV1.	
	GPIO_PM_PAD_DRV0_18	4	GPIO_18's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_18	1	GPIO_18's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_18	0	GPIO_18's FIQ final status for edge wake-up source.	
13h (0F26h)	REG0F26	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_19	7	GPIO_19's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_19	6	GPIO_19's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_19	5	GPIO_19's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_19	4	GPIO_19's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_19	3	GPIO_19's glitch remover enable.	
	GPIO_PM_IN_19	2	GPIO_19's input.	
	GPIO_PM_OUT_19	1	GPIO_19's output.	
	GPIO_PM_OEN_19	0	GPIO_19's output enable.	
13h	REG0F27	7:0	Default : 0x00	Access : RO, R/W

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
(0F27h)	GPIO_PM_PAD_PS_19	7	GPIO_19's PAD PS.	
	GPIO_PM_PAD_PE_19	6	GPIO_19's PAD PE.	
	GPIO_PM_PAD_DRV1_19	5	GPIO_19's PAD DRV1.	
	GPIO_PM_PAD_DRV0_19	4	GPIO_19's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_19	1	GPIO_19's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_19	0	GPIO_19's FIQ final status for edge wake-up source.	
14h (0F28h)	REG0F28	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_20	7	GPIO_20's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_20	6	GPIO_20's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_20	5	GPIO_20's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_20	4	GPIO_20's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_20	3	GPIO_20's glitch remover enable.	
	GPIO_PM_IN_20	2	GPIO_20's input.	
	GPIO_PM_OUT_20	1	GPIO_20's output.	
	GPIO_PM_OEN_20	0	GPIO_20's output enable (IR).	
	REG0F29	7:0	Default : 0x00	Access : RO, R/W
14h (0F29h)	GPIO_PM_PAD_PS_20	7	GPIO_20's PAD PS.	
	GPIO_PM_PAD_PE_20	6	GPIO_20's PAD PE.	
	GPIO_PM_PAD_DRV1_20	5	GPIO_20's PAD DRV1.	
	GPIO_PM_PAD_DRV0_20	4	GPIO_20's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_20	1	GPIO_20's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_20	0	GPIO_20's FIQ final status for edge wake-up source.	
	REG0F2A	7:0	Default : 0x11	Access : RO, R/W, WO
15h (0F2Ah)	GPIO_PM_WK_FIQ_POL_21	7	GPIO_21's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_21	6	GPIO_21's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_21	5	GPIO_21's FIQ force for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description
21	GPIO_PM_WK_FIQ_MASK_2	4	GPIO_21's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_21	3	GPIO_21's glitch remover enable.
	GPIO_PM_IN_21	2	GPIO_21's input.
	GPIO_PM_OUT_21	1	GPIO_21's output.
	GPIO_PM_OEN_21	0	GPIO_21's output enable (UART_RX).
	REG0F2B	7:0	Default : 0x00 Access : RO, R/W
15h (0F2Bh)	GPIO_PM_PAD_PS_21	7	GPIO_21's PAD PS.
	GPIO_PM_PAD_PE_21	6	GPIO_21's PAD PE.
	GPIO_PM_PAD_DRV1_21	5	GPIO_21's PAD DRV1.
	GPIO_PM_PAD_DRV0_21	4	GPIO_21's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_21	1	GPIO_21's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_21	0	GPIO_21's FIQ final status for edge wake-up source.
	REG0F2C	7:0	Default : 0x11 Access : RO, R/W, WO
16h (0F2Ch)	GPIO_PM_WK_FIQ_POL_22	7	GPIO_22's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_22	6	GPIO_22's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_22	5	GPIO_22's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_22	4	GPIO_22's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_22	3	GPIO_22's glitch remover enable.
	GPIO_PM_IN_22	2	GPIO_22's input.
	GPIO_PM_OUT_22	1	GPIO_22's output.
	GPIO_PM_OEN_22	0	GPIO_22's output enable (CEC).
	REG0F2D	7:0	Default : 0x00 Access : RO, R/W
16h (0F2Dh)	GPIO_PM_PAD_PS_22	7	GPIO_22's PAD PS.
	GPIO_PM_PAD_PE_22	6	GPIO_22's PAD PE.
	GPIO_PM_PAD_DRV1_22	5	GPIO_22's PAD DRV1.
	GPIO_PM_PAD_DRV0_22	4	GPIO_22's PAD DRV0.
	-	3:2	Reserved.

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_WK_FIQ_RAW_STATUS_22	1	GPIO_22's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_22	0	GPIO_22's FIQ final status for edge wake-up source.	
17h (0F2Eh)	REG0F2E	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_23	7	GPIO_23's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_23	6	GPIO_23's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_23	5	GPIO_23's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_23	4	GPIO_23's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_23	3	GPIO_23's glitch remover enable.	
	GPIO_PM_IN_23	2	GPIO_23's input.	
	GPIO_PM_OUT_23	1	GPIO_23's output.	
	GPIO_PM_OEN_23	0	GPIO_23's output enable (un-connect).	
17h (0F2Fh)	REG0F2F	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_23	7	GPIO_23's PAD PS.	
	GPIO_PM_PAD_PE_23	6	GPIO_23's PAD PE.	
	GPIO_PM_PAD_DRV1_23	5	GPIO_23's PAD DRV1.	
	GPIO_PM_PAD_DRV0_23	4	GPIO_23's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_23	1	GPIO_23's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_23	0	GPIO_23's FIQ final status for edge wake-up source.	
18h (0F30h)	REG0F30	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_24	7	GPIO_24's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_24	6	GPIO_24's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_24	5	GPIO_24's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_24	4	GPIO_24's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_24	3	GPIO_24's glitch remover enable.	
	GPIO_PM_IN_24	2	GPIO_24's input.	
	GPIO_PM_OUT_24	1	GPIO_24's output.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_OEN_24	0	GPIO_24's output enable (SPI_CZ).	
18h (0F31h)	REG0F31	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_24	7	GPIO_24's PAD PS.	
	GPIO_PM_PAD_PE_24	6	GPIO_24's PAD PE.	
	GPIO_PM_PAD_DRV1_24	5	GPIO_24's PAD DRV1.	
	GPIO_PM_PAD_DRV0_24	4	GPIO_24's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_24	1	GPIO_24's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_24	0	GPIO_24's FIQ final status for edge wake-up source.	
19h (0F32h)	REG0F32	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_25	7	GPIO_25's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_25	6	GPIO_25's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_25	5	GPIO_25's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_25	4	GPIO_25's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_25	3	GPIO_25's glitch remover enable.	
	GPIO_PM_IN_25	2	GPIO_25's input.	
	GPIO_PM_OUT_25	1	GPIO_25's output.	
	GPIO_PM_OEN_25	0	GPIO_25's output enable (SPI_CK).	
19h (0F33h)	REG0F33	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_25	7	GPIO_25's PAD PS.	
	GPIO_PM_PAD_PE_25	6	GPIO_25's PAD PE.	
	GPIO_PM_PAD_DRV1_25	5	GPIO_25's PAD DRV1.	
	GPIO_PM_PAD_DRV0_25	4	GPIO_25's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_25	1	GPIO_25's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_25	0	GPIO_25's FIQ final status for edge wake-up source.	
1Ah (0F34h)	REG0F34	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_26	7	GPIO_26's FIQ polarity for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description
1Ah (0F35h)	GPIO_PM_WK_FIQ_CLR_26	6	GPIO_26's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_26	5	GPIO_26's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_26	4	GPIO_26's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_26	3	GPIO_26's glitch remover enable.
	GPIO_PM_IN_26	2	GPIO_26's input.
	GPIO_PM_OUT_26	1	GPIO_26's output.
	GPIO_PM_OEN_26	0	GPIO_26's output enable (SPI_DI).
1Bh (0F36h)	REG0F35	7:0	Default : 0x00
	GPIO_PM_PAD_PS_26	7	GPIO_26's PAD PS.
	GPIO_PM_PAD_PE_26	6	GPIO_26's PAD PE.
	GPIO_PM_PAD_DRV1_26	5	GPIO_26's PAD DRV1.
	GPIO_PM_PAD_DRV0_26	4	GPIO_26's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_26	1	GPIO_26's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_26	0	GPIO_26's FIQ final status for edge wake-up source.
1Bh (0F37h)	REG0F36	7:0	Default : 0x11
	GPIO_PM_WK_FIQ_POL_27	7	GPIO_27's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_27	6	GPIO_27's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_27	5	GPIO_27's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_27	4	GPIO_27's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_27	3	GPIO_27's glitch remover enable.
	GPIO_PM_IN_27	2	GPIO_27's input.
	GPIO_PM_OUT_27	1	GPIO_27's output.
	GPIO_PM_OEN_27	0	GPIO_27's output enable (SPI_DO).

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
1Ch (0F38h)	GPIO_PM_PAD_DRV0_27	4	GPIO_27's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_27	1	GPIO_27's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_27	0	GPIO_27's FIQ final status for edge wake-up source.	
1Ch (0F38h)	REG0F38	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_28	7	GPIO_28's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_28	6	GPIO_28's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_28	5	GPIO_28's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_28	4	GPIO_28's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_28	3	GPIO_28's glitch remover enable.	
	GPIO_PM_IN_28	2	GPIO_28's input.	
	GPIO_PM_OUT_28	1	GPIO_28's output.	
	GPIO_PM_OEN_28	0	GPIO_28's output enable.	
1Ch (0F39h)	REG0F39	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_28	7	GPIO_28's PAD PS.	
	GPIO_PM_PAD_PE_28	6	GPIO_28's PAD PE.	
	GPIO_PM_PAD_DRV1_28	5	GPIO_28's PAD DRV1.	
	GPIO_PM_PAD_DRV0_28	4	GPIO_28's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_28	1	GPIO_28's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_28	0	GPIO_28's FIQ final status for edge wake-up source.	
1Dh (0F3Ah)	REG0F3A	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_29	7	GPIO_29's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_29	6	GPIO_29's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_29	5	GPIO_29's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_29	4	GPIO_29's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_29	3	GPIO_29's glitch remover enable.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_IN_29	2	GPIO_29's input.	
	GPIO_PM_OUT_29	1	GPIO_29's output.	
	GPIO_PM_OEN_29	0	GPIO_29's output enable.	
1Dh (0F3Bh)	REG0F3B	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_29	7	GPIO_29's PAD PS.	
	GPIO_PM_PAD_PE_29	6	GPIO_29's PAD PE.	
	GPIO_PM_PAD_DRV1_29	5	GPIO_29's PAD DRV1.	
	GPIO_PM_PAD_DRV0_29	4	GPIO_29's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_29	1	GPIO_29's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_29	0	GPIO_29's FIQ final status for edge wake-up source.	
1Eh (0F3Ch)	REG0F3C	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_30	7	GPIO_30's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_30	6	GPIO_30's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_30	5	GPIO_30's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_30	4	GPIO_30's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_30	3	GPIO_30's glitch remover enable.	
	GPIO_PM_IN_30	2	GPIO_30's input.	
	GPIO_PM_OUT_30	1	GPIO_30's output.	
	GPIO_PM_OEN_30	0	GPIO_30's output enable.	
1Eh (0F3Dh)	REG0F3D	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_30	7	GPIO_30's PAD PS.	
	GPIO_PM_PAD_PE_30	6	GPIO_30's PAD PE.	
	GPIO_PM_PAD_DRV1_30	5	GPIO_30's PAD DRV1.	
	GPIO_PM_PAD_DRV0_30	4	GPIO_30's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_30	1	GPIO_30's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_30	0	GPIO_30's FIQ final status for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
1Fh (0F3Eh)	REG0F3E	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_31	7	GPIO_31's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_31	6	GPIO_31's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_31	5	GPIO_31's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_31	4	GPIO_31's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_31	3	GPIO_31's glitch remover enable.	
	GPIO_PM_IN_31	2	GPIO_31's input.	
	GPIO_PM_OUT_31	1	GPIO_31's output.	
	GPIO_PM_OEN_31	0	GPIO_31's output enable.	
1Fh (0F3Fh)	REG0F3F	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_31	7	GPIO_31's PAD PS.	
	GPIO_PM_PAD_PE_31	6	GPIO_31's PAD PE.	
	GPIO_PM_PAD_DRV1_31	5	GPIO_31's PAD DRV1.	
	GPIO_PM_PAD_DRV0_31	4	GPIO_31's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_31	1	GPIO_31's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_31	0	GPIO_31's FIQ final status for edge wake-up source.	
20h (0F40h)	REG0F40	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_32	7	GPIO_32's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_32	6	GPIO_32's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_32	5	GPIO_32's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_32	4	GPIO_32's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_32	3	GPIO_32's glitch remover enable.	
	GPIO_PM_IN_32	2	GPIO_32's input.	
	GPIO_PM_OUT_32	1	GPIO_32's output.	
	GPIO_PM_OEN_32	0	GPIO_32's output enable.	
20h (0F41h)	REG0F41	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_32	7	GPIO_32's PAD PS.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description
	GPIO_PM_PAD_PE_32	6	GPIO_32's PAD PE.
	GPIO_PM_PAD_DRV1_32	5	GPIO_32's PAD DRV1.
	GPIO_PM_PAD_DRV0_32	4	GPIO_32's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_32	1	GPIO_32's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_32	0	GPIO_32's FIQ final status for edge wake-up source.
21h (0F42h)	REG0F42	7:0	Default : 0x11 Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_33	7	GPIO_33's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_33	6	GPIO_33's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_33	5	GPIO_33's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_33	4	GPIO_33's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_33	3	GPIO_33's glitch remover enable.
	GPIO_PM_IN_33	2	GPIO_33's input.
	GPIO_PM_OUT_33	1	GPIO_33's output.
	GPIO_PM_OEN_33	0	GPIO_33's output enable.
21h (0F43h)	REG0F43	7:0	Default : 0x00 Access : RO, R/W
	GPIO_PM_PAD_PS_33	7	GPIO_33's PAD PS.
	GPIO_PM_PAD_PE_33	6	GPIO_33's PAD PE.
	GPIO_PM_PAD_DRV1_33	5	GPIO_33's PAD DRV1.
	GPIO_PM_PAD_DRV0_33	4	GPIO_33's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_33	1	GPIO_33's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_33	0	GPIO_33's FIQ final status for edge wake-up source.
22h (0F44h)	REG0F44	7:0	Default : 0x11 Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_34	7	GPIO_34's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_34	6	GPIO_34's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_34	5	GPIO_34's FIQ force for edge wake-up source.

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
22h (0F45h)	GPIO_PM_WK_FIQ_MASK_34	4	GPIO_34's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_34	3	GPIO_34's glitch remover enable.	
	GPIO_PM_IN_34	2	GPIO_34's input.	
	GPIO_PM_OUT_34	1	GPIO_34's output.	
	GPIO_PM_OEN_34	0	GPIO_34's output enable.	
23h (0F46h)	REG0F45	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_34	7	GPIO_34's PAD PS.	
	GPIO_PM_PAD_PE_34	6	GPIO_34's PAD PE.	
	GPIO_PM_PAD_DRV1_34	5	GPIO_34's PAD DRV1.	
	GPIO_PM_PAD_DRV0_34	4	GPIO_34's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_34	1	GPIO_34's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_34	0	GPIO_34's FIQ final status for edge wake-up source.	
23h (0F47h)	REG0F46	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_35	7	GPIO_35's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_35	6	GPIO_35's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_35	5	GPIO_35's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_35	4	GPIO_35's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_35	3	GPIO_35's glitch remover enable.	
	GPIO_PM_IN_35	2	GPIO_35's input.	
	GPIO_PM_OUT_35	1	GPIO_35's output.	
	GPIO_PM_OEN_35	0	GPIO_35's output enable.	
23h (0F47h)	REG0F47	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_35	7	GPIO_35's PAD PS.	
	GPIO_PM_PAD_PE_35	6	GPIO_35's PAD PE.	
	GPIO_PM_PAD_DRV1_35	5	GPIO_35's PAD DRV1.	
	GPIO_PM_PAD_DRV0_35	4	GPIO_35's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_35	1	GPIO_35's FIQ raw status for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	ATUS_35			
	GPIO_PM_WK_FIQ_FINAL_S TATUS_35	0	GPIO_35's FIQ final status for edge wake-up source.	
24h (0F48h)	REG0F48	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_36	7	GPIO_36's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_36	6	GPIO_36's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_36	5	GPIO_36's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_36	4	GPIO_36's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_36	3	GPIO_36's glitch remover enable.	
	GPIO_PM_IN_36	2	GPIO_36's input.	
	GPIO_PM_OUT_36	1	GPIO_36's output.	
	GPIO_PM_OEN_36	0	GPIO_36's output enable.	
24h (0F49h)	REG0F49	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_36	7	GPIO_36's PAD PS.	
	GPIO_PM_PAD_PE_36	6	GPIO_36's PAD PE.	
	GPIO_PM_PAD_DRV1_36	5	GPIO_36's PAD DRV1.	
	GPIO_PM_PAD_DRV0_36	4	GPIO_36's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_ST ATUS_36	1	GPIO_36's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_S TATUS_36	0	GPIO_36's FIQ final status for edge wake-up source.	
25h (0F4Ah)	REG0F4A	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_37	7	GPIO_37's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_37	6	GPIO_37's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_37	5	GPIO_37's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_37	4	GPIO_37's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_37	3	GPIO_37's glitch remover enable.	
	GPIO_PM_IN_37	2	GPIO_37's input.	
	GPIO_PM_OUT_37	1	GPIO_37's output.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_OEN_37	0	GPIO_37's output enable.	
25h (0F4Bh)	REG0F4B	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_37	7	GPIO_37's PAD PS.	
	GPIO_PM_PAD_PE_37	6	GPIO_37's PAD PE.	
	GPIO_PM_PAD_DRV1_37	5	GPIO_37's PAD DRV1.	
	GPIO_PM_PAD_DRV0_37	4	GPIO_37's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_37	1	GPIO_37's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_37	0	GPIO_37's FIQ final status for edge wake-up source.	
26h (0F4Ch)	REG0F4C	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_38	7	GPIO_38's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_38	6	GPIO_38's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_38	5	GPIO_38's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_38	4	GPIO_38's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_38	3	GPIO_38's glitch remover enable.	
	GPIO_PM_IN_38	2	GPIO_38's input.	
	GPIO_PM_OUT_38	1	GPIO_38's output.	
	GPIO_PM_OEN_38	0	GPIO_38's output enable.	
26h (0F4Dh)	REG0F4D	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_38	7	GPIO_38's PAD PS.	
	GPIO_PM_PAD_PE_38	6	GPIO_38's PAD PE.	
	GPIO_PM_PAD_DRV1_38	5	GPIO_38's PAD DRV1.	
	GPIO_PM_PAD_DRV0_38	4	GPIO_38's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_38	1	GPIO_38's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_38	0	GPIO_38's FIQ final status for edge wake-up source.	
27h (0F4Eh)	REG0F4E	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_39	7	GPIO_39's FIQ polarity for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
27h (0F4Fh)	GPIO_PM_WK_FIQ_CLR_39	6	GPIO_39's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_39	5	GPIO_39's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_39	4	GPIO_39's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_39	3	GPIO_39's glitch remover enable.	
	GPIO_PM_IN_39	2	GPIO_39's input.	
	GPIO_PM_OUT_39	1	GPIO_39's output.	
	GPIO_PM_OEN_39	0	GPIO_39's output enable (PAD_GT0_MDC).	
28h (0F50h)	REG0F4F	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_39	7	GPIO_39's PAD PS.	
	GPIO_PM_PAD_PE_39	6	GPIO_39's PAD PE.	
	GPIO_PM_PAD_DRV1_39	5	GPIO_39's PAD DRV1.	
	GPIO_PM_PAD_DRV0_39	4	GPIO_39's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_39	1	GPIO_39's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_39	0	GPIO_39's FIQ final status for edge wake-up source.	
	REG0F50	7:0	Default : 0x11	Access : RO, R/W, WO
28h (0F51h)	GPIO_PM_WK_FIQ_POL_40	7	GPIO_40's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_40	6	GPIO_40's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_40	5	GPIO_40's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_40	4	GPIO_40's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_40	3	GPIO_40's glitch remover enable.	
	GPIO_PM_IN_40	2	GPIO_40's input.	
	GPIO_PM_OUT_40	1	GPIO_40's output.	
	GPIO_PM_OEN_40	0	GPIO_40's output enable (PAD_GT0_MDIO).	
	REG0F51	7:0	Default : 0x00	Access : RO, R/W

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
29h (0F52h)	GPIO_PM_PAD_DRV0_40	4	GPIO_40's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_40	1	GPIO_40's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_40	0	GPIO_40's FIQ final status for edge wake-up source.	
29h (0F52h)	REG0F52	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_41	7	GPIO_41's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_41	6	GPIO_41's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_41	5	GPIO_41's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_41	4	GPIO_41's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_41	3	GPIO_41's glitch remover enable.	
	GPIO_PM_IN_41	2	GPIO_41's input.	
	GPIO_PM_OUT_41	1	GPIO_41's output.	
	GPIO_PM_OEN_41	0	GPIO_41's output enable (PAD_GT0_RX_CLK).	
29h (0F53h)	REG0F53	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_41	7	GPIO_41's PAD PS.	
	GPIO_PM_PAD_PE_41	6	GPIO_41's PAD PE.	
	GPIO_PM_PAD_DRV1_41	5	GPIO_41's PAD DRV1.	
	GPIO_PM_PAD_DRV0_41	4	GPIO_41's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_41	1	GPIO_41's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_41	0	GPIO_41's FIQ final status for edge wake-up source.	
2Ah (0F54h)	REG0F54	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_42	7	GPIO_42's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_42	6	GPIO_42's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_42	5	GPIO_42's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_42	4	GPIO_42's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_42	3	GPIO_42's glitch remover enable.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_IN_42	2	GPIO_42's input.	
	GPIO_PM_OUT_42	1	GPIO_42's output.	
	GPIO_PM_OEN_42	0	GPIO_42's output enable (PAD_GT0_RX_CTL).	
2Ah (0F55h)	REG0F55	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_42	7	GPIO_42's PAD PS.	
	GPIO_PM_PAD_PE_42	6	GPIO_42's PAD PE.	
	GPIO_PM_PAD_DRV1_42	5	GPIO_42's PAD DRV1.	
	GPIO_PM_PAD_DRV0_42	4	GPIO_42's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_42	1	GPIO_42's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_42	0	GPIO_42's FIQ final status for edge wake-up source.	
2Bh (0F56h)	REG0F56	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_43	7	GPIO_43's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_43	6	GPIO_43's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_43	5	GPIO_43's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_43	4	GPIO_43's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_43	3	GPIO_43's glitch remover enable.	
	GPIO_PM_IN_43	2	GPIO_43's input.	
	GPIO_PM_OUT_43	1	GPIO_43's output.	
	GPIO_PM_OEN_43	0	GPIO_43's output enable (PAD_GT0_RX_D0).	
2Bh (0F57h)	REG0F57	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_43	7	GPIO_43's PAD PS.	
	GPIO_PM_PAD_PE_43	6	GPIO_43's PAD PE.	
	GPIO_PM_PAD_DRV1_43	5	GPIO_43's PAD DRV1.	
	GPIO_PM_PAD_DRV0_43	4	GPIO_43's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_43	1	GPIO_43's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_43	0	GPIO_43's FIQ final status for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
2Ch (0F58h)	REG0F58	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_44	7	GPIO_44's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_44	6	GPIO_44's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_44	5	GPIO_44's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_44	4	GPIO_44's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_44	3	GPIO_44's glitch remover enable.	
	GPIO_PM_IN_44	2	GPIO_44's input.	
	GPIO_PM_OUT_44	1	GPIO_44's output.	
	GPIO_PM_OEN_44	0	GPIO_44's output enable (PAD_GT0_RX_D1).	
2Ch (0F59h)	REG0F59	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_44	7	GPIO_44's PAD PS.	
	GPIO_PM_PAD_PE_44	6	GPIO_44's PAD PE.	
	GPIO_PM_PAD_DRV1_44	5	GPIO_44's PAD DRV1.	
	GPIO_PM_PAD_DRV0_44	4	GPIO_44's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_44	1	GPIO_44's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_44	0	GPIO_44's FIQ final status for edge wake-up source.	
2Dh (0F5Ah)	REG0F5A	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_45	7	GPIO_45's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_45	6	GPIO_45's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_45	5	GPIO_45's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_45	4	GPIO_45's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_45	3	GPIO_45's glitch remover enable.	
	GPIO_PM_IN_45	2	GPIO_45's input.	
	GPIO_PM_OUT_45	1	GPIO_45's output.	
	GPIO_PM_OEN_45	0	GPIO_45's output enable (PAD_GT0_RX_D2).	
2Dh (0F5Bh)	REG0F5B	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_45	7	GPIO_45's PAD PS.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description
2Eh (0F5Ch)	GPIO_PM_PAD_PE_45	6	GPIO_45's PAD PE.
	GPIO_PM_PAD_DRV1_45	5	GPIO_45's PAD DRV1.
	GPIO_PM_PAD_DRV0_45	4	GPIO_45's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_45	1	GPIO_45's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_45	0	GPIO_45's FIQ final status for edge wake-up source.
	REG0F5C	7:0	Default : 0x11 Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_46	7	GPIO_46's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_46	6	GPIO_46's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_46	5	GPIO_46's FIQ force for edge wake-up source.
2Eh (0F5Dh)	GPIO_PM_WK_FIQ_MASK_46	4	GPIO_46's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_46	3	GPIO_46's glitch remover enable.
	GPIO_PM_IN_46	2	GPIO_46's input.
	GPIO_PM_OUT_46	1	GPIO_46's output.
	GPIO_PM_OEN_46	0	GPIO_46's output enable (PAD_GT0_RX_D3).
	REG0F5D	7:0	Default : 0x00 Access : RO, R/W
	GPIO_PM_PAD_PS_46	7	GPIO_46's PAD PS.
	GPIO_PM_PAD_PE_46	6	GPIO_46's PAD PE.
	GPIO_PM_PAD_DRV1_46	5	GPIO_46's PAD DRV1.
	GPIO_PM_PAD_DRV0_46	4	GPIO_46's PAD DRV0.
2Fh (0F5Eh)	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_46	1	GPIO_46's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_46	0	GPIO_46's FIQ final status for edge wake-up source.
	REG0F5E	7:0	Default : 0x11 Access : RO, R/W, WO
2Fh (0F5Eh)	GPIO_PM_WK_FIQ_POL_47	7	GPIO_47's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_47	6	GPIO_47's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_47	5	GPIO_47's FIQ force for edge wake-up source.

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description
2Fh (0F5Fh)	GPIO_PM_WK_FIQ_MASK_47	4	GPIO_47's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_47	3	GPIO_47's glitch remover enable.
	GPIO_PM_IN_47	2	GPIO_47's input.
	GPIO_PM_OUT_47	1	GPIO_47's output.
	GPIO_PM_OEN_47	0	GPIO_47's output enable (PAD_GT0_TX_CLK).
30h (0F60h)	REG0F5F	7:0	Default : 0x00 Access : RO, R/W
	GPIO_PM_PAD_PS_47	7	GPIO_47's PAD PS.
	GPIO_PM_PAD_PE_47	6	GPIO_47's PAD PE.
	GPIO_PM_PAD_DRV1_47	5	GPIO_47's PAD DRV1.
	GPIO_PM_PAD_DRV0_47	4	GPIO_47's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_47	1	GPIO_47's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_47	0	GPIO_47's FIQ final status for edge wake-up source.
30h (0F61h)	REG0F60	7:0	Default : 0x11 Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_48	7	GPIO_48's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_48	6	GPIO_48's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_48	5	GPIO_48's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_48	4	GPIO_48's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_48	3	GPIO_48's glitch remover enable.
	GPIO_PM_IN_48	2	GPIO_48's input.
	GPIO_PM_OUT_48	1	GPIO_48's output.
	GPIO_PM_OEN_48	0	GPIO_48's output enable (PAD_GT0_TX_CTL).

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	ATUS_48			
	GPIO_PM_WK_FIQ_FINAL_S TATUS_48	0	GPIO_48's FIQ final status for edge wake-up source.	
31h (0F62h)	REG0F62	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_49	7	GPIO_49's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_49	6	GPIO_49's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_49	5	GPIO_49's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_49	4	GPIO_49's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_49	3	GPIO_49's glitch remover enable.	
	GPIO_PM_IN_49	2	GPIO_49's input.	
	GPIO_PM_OUT_49	1	GPIO_49's output.	
	GPIO_PM_OEN_49	0	GPIO_49's output enable (PAD_GT0_TX_D0).	
31h (0F63h)	REG0F63	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_49	7	GPIO_49's PAD PS.	
	GPIO_PM_PAD_PE_49	6	GPIO_49's PAD PE.	
	GPIO_PM_PAD_DRV1_49	5	GPIO_49's PAD DRV1.	
	GPIO_PM_PAD_DRV0_49	4	GPIO_49's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_ST ATUS_49	1	GPIO_49's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_S TATUS_49	0	GPIO_49's FIQ final status for edge wake-up source.	
32h (0F64h)	REG0F64	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_50	7	GPIO_50's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_50	6	GPIO_50's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_50	5	GPIO_50's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_50	4	GPIO_50's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_50	3	GPIO_50's glitch remover enable.	
	GPIO_PM_IN_50	2	GPIO_50's input.	
	GPIO_PM_OUT_50	1	GPIO_50's output.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_OEN_50	0	GPIO_50's output enable (PAD_GT0_TX_D1).	
32h (0F65h)	REG0F65	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_50	7	GPIO_50's PAD PS.	
	GPIO_PM_PAD_PE_50	6	GPIO_50's PAD PE.	
	GPIO_PM_PAD_DRV1_50	5	GPIO_50's PAD DRV1.	
	GPIO_PM_PAD_DRV0_50	4	GPIO_50's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_50	1	GPIO_50's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_50	0	GPIO_50's FIQ final status for edge wake-up source.	
33h (0F66h)	REG0F66	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_51	7	GPIO_51's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_51	6	GPIO_51's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_51	5	GPIO_51's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_51	4	GPIO_51's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_51	3	GPIO_51's glitch remover enable.	
	GPIO_PM_IN_51	2	GPIO_51's input.	
	GPIO_PM_OUT_51	1	GPIO_51's output.	
	GPIO_PM_OEN_51	0	GPIO_51's output enable (PAD_GT0_TX_D2).	
33h (0F67h)	REG0F67	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_51	7	GPIO_51's PAD PS.	
	GPIO_PM_PAD_PE_51	6	GPIO_51's PAD PE.	
	GPIO_PM_PAD_DRV1_51	5	GPIO_51's PAD DRV1.	
	GPIO_PM_PAD_DRV0_51	4	GPIO_51's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_51	1	GPIO_51's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_51	0	GPIO_51's FIQ final status for edge wake-up source.	
34h (0F68h)	REG0F68	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_52	7	GPIO_52's FIQ polarity for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
34h (0F69h)	GPIO_PM_WK_FIQ_CLR_52	6	GPIO_52's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_52	5	GPIO_52's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_52	4	GPIO_52's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_52	3	GPIO_52's glitch remover enable.	
	GPIO_PM_IN_52	2	GPIO_52's input.	
	GPIO_PM_OUT_52	1	GPIO_52's output.	
	GPIO_PM_OEN_52	0	GPIO_52's output enable (PAD_GT0_TX_D3).	
35h (0F6Ah)	REG0F69	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_52	7	GPIO_52's PAD PS.	
	GPIO_PM_PAD_PE_52	6	GPIO_52's PAD PE.	
	GPIO_PM_PAD_DRV1_52	5	GPIO_52's PAD DRV1.	
	GPIO_PM_PAD_DRV0_52	4	GPIO_52's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_52	1	GPIO_52's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_52	0	GPIO_52's FIQ final status for edge wake-up source.	
35h (0F6Bh)	REG0F6A	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_53	7	GPIO_53's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_53	6	GPIO_53's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_53	5	GPIO_53's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_53	4	GPIO_53's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_53	3	GPIO_53's glitch remover enable.	
	GPIO_PM_IN_53	2	GPIO_53's input.	
	GPIO_PM_OUT_53	1	GPIO_53's output.	
	GPIO_PM_OEN_53	0	GPIO_53's output enable (PAD_GT1_MDC).	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
36h (0F6Ch)	GPIO_PM_PAD_DRV0_53	4	GPIO_53's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_53	1	GPIO_53's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_53	0	GPIO_53's FIQ final status for edge wake-up source.	
36h (0F6Ch)	REG0F6C	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_54	7	GPIO_54's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_54	6	GPIO_54's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_54	5	GPIO_54's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_54	4	GPIO_54's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_54	3	GPIO_54's glitch remover enable.	
	GPIO_PM_IN_54	2	GPIO_54's input.	
	GPIO_PM_OUT_54	1	GPIO_54's output.	
	GPIO_PM_OEN_54	0	GPIO_54's output enable (PAD_GT1_MDIO).	
36h (0F6Dh)	REG0F6D	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_54	7	GPIO_54's PAD PS.	
	GPIO_PM_PAD_PE_54	6	GPIO_54's PAD PE.	
	GPIO_PM_PAD_DRV1_54	5	GPIO_54's PAD DRV1.	
	GPIO_PM_PAD_DRV0_54	4	GPIO_54's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_54	1	GPIO_54's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_54	0	GPIO_54's FIQ final status for edge wake-up source.	
37h (0F6Eh)	REG0F6E	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_55	7	GPIO_55's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_55	6	GPIO_55's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_55	5	GPIO_55's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_55	4	GPIO_55's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_55	3	GPIO_55's glitch remover enable.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_IN_55	2	GPIO_55's input.	
	GPIO_PM_OUT_55	1	GPIO_55's output.	
	GPIO_PM_OEN_55	0	GPIO_55's output enable (PAD_GT1_RX_CLK).	
37h (0F6Fh)	REG0F6F	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_55	7	GPIO_55's PAD PS.	
	GPIO_PM_PAD_PE_55	6	GPIO_55's PAD PE.	
	GPIO_PM_PAD_DRV1_55	5	GPIO_55's PAD DRV1.	
	GPIO_PM_PAD_DRV0_55	4	GPIO_55's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_55	1	GPIO_55's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_55	0	GPIO_55's FIQ final status for edge wake-up source.	
38h (0F70h)	REG0F70	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_56	7	GPIO_56's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_56	6	GPIO_56's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_56	5	GPIO_56's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_56	4	GPIO_56's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_56	3	GPIO_56's glitch remover enable.	
	GPIO_PM_IN_56	2	GPIO_56's input.	
	GPIO_PM_OUT_56	1	GPIO_56's output.	
	GPIO_PM_OEN_56	0	GPIO_56's output enable (PAD_GT1_RX_CTL).	
38h (0F71h)	REG0F71	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_56	7	GPIO_56's PAD PS.	
	GPIO_PM_PAD_PE_56	6	GPIO_56's PAD PE.	
	GPIO_PM_PAD_DRV1_56	5	GPIO_56's PAD DRV1.	
	GPIO_PM_PAD_DRV0_56	4	GPIO_56's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_56	1	GPIO_56's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_56	0	GPIO_56's FIQ final status for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
39h (0F72h)	REG0F72	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_57	7	GPIO_57's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_57	6	GPIO_57's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_57	5	GPIO_57's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_57	4	GPIO_57's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_57	3	GPIO_57's glitch remover enable.	
	GPIO_PM_IN_57	2	GPIO_57's input.	
	GPIO_PM_OUT_57	1	GPIO_57's output.	
	GPIO_PM_OEN_57	0	GPIO_57's output enable (PAD_GT1_RX_D0).	
39h (0F73h)	REG0F73	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_57	7	GPIO_57's PAD PS.	
	GPIO_PM_PAD_PE_57	6	GPIO_57's PAD PE.	
	GPIO_PM_PAD_DRV1_57	5	GPIO_57's PAD DRV1.	
	GPIO_PM_PAD_DRV0_57	4	GPIO_57's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_57	1	GPIO_57's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_57	0	GPIO_57's FIQ final status for edge wake-up source.	
3Ah (0F74h)	REG0F74	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_58	7	GPIO_58's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_58	6	GPIO_58's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_58	5	GPIO_58's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_58	4	GPIO_58's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_58	3	GPIO_58's glitch remover enable.	
	GPIO_PM_IN_58	2	GPIO_58's input.	
	GPIO_PM_OUT_58	1	GPIO_58's output.	
	GPIO_PM_OEN_58	0	GPIO_58's output enable (PAD_GT1_RX_D1).	
3Ah (0F75h)	REG0F75	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_58	7	GPIO_58's PAD PS.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description
3Bh (0F76h)	GPIO_PM_PAD_PE_58	6	GPIO_58's PAD PE.
	GPIO_PM_PAD_DRV1_58	5	GPIO_58's PAD DRV1.
	GPIO_PM_PAD_DRV0_58	4	GPIO_58's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_58	1	GPIO_58's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_58	0	GPIO_58's FIQ final status for edge wake-up source.
	REG0F76	7:0	Default : 0x11 Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_59	7	GPIO_59's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_59	6	GPIO_59's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_59	5	GPIO_59's FIQ force for edge wake-up source.
3Bh (0F77h)	GPIO_PM_WK_FIQ_MASK_59	4	GPIO_59's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_59	3	GPIO_59's glitch remover enable.
	GPIO_PM_IN_59	2	GPIO_59's input.
	GPIO_PM_OUT_59	1	GPIO_59's output.
	GPIO_PM_OEN_59	0	GPIO_59's output enable (PAD_GT1_RX_D2).
	REG0F77	7:0	Default : 0x00 Access : RO, R/W
	GPIO_PM_PAD_PS_59	7	GPIO_59's PAD PS.
	GPIO_PM_PAD_PE_59	6	GPIO_59's PAD PE.
	GPIO_PM_PAD_DRV1_59	5	GPIO_59's PAD DRV1.
	GPIO_PM_PAD_DRV0_59	4	GPIO_59's PAD DRV0.
3Ch (0F78h)	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_59	1	GPIO_59's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_59	0	GPIO_59's FIQ final status for edge wake-up source.
	REG0F78	7:0	Default : 0x11 Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_60	7	GPIO_60's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_60	6	GPIO_60's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_60	5	GPIO_60's FIQ force for edge wake-up source.



PM_GPIO Register (Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
3Ch (0F79h)	GPIO_PM_WK_FIQ_MASK_60	4	GPIO_60's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_60	3	GPIO_60's glitch remover enable.
	GPIO_PM_IN_60	2	GPIO_60's input.
	GPIO_PM_OUT_60	1	GPIO_60's output.
	GPIO_PM_OEN_60	0	GPIO_60's output enable (PAD_GT1_RX_D3).
3Dh (0F7Ah)	REG0F79	7:0	Default : 0x00 Access : RO, R/W
	GPIO_PM_PAD_PS_60	7	GPIO_60's PAD PS.
	GPIO_PM_PAD_PE_60	6	GPIO_60's PAD PE.
	GPIO_PM_PAD_DRV1_60	5	GPIO_60's PAD DRV1.
	GPIO_PM_PAD_DRV0_60	4	GPIO_60's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_STATUS_60	1	GPIO_60's FIQ raw status for edge wake-up source.
	GPIO_PM_WK_FIQ_FINAL_STATUS_60	0	GPIO_60's FIQ final status for edge wake-up source.
3Dh (0F7Bh)	REG0F7A	7:0	Default : 0x11 Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_61	7	GPIO_61's FIQ polarity for edge wake-up source.
	GPIO_PM_WK_FIQ_CLR_61	6	GPIO_61's FIQ clear for edge wake-up source.
	GPIO_PM_WK_FIQ_FORCE_61	5	GPIO_61's FIQ force for edge wake-up source.
	GPIO_PM_WK_FIQ_MASK_61	4	GPIO_61's FIQ mask for edge wake-up source.
	GPIO_PM_GLHRM_EN_61	3	GPIO_61's glitch remover enable.
	GPIO_PM_IN_61	2	GPIO_61's input.
	GPIO_PM_OUT_61	1	GPIO_61's output.
	GPIO_PM_OEN_61	0	GPIO_61's output enable (PAD_GT1_TX_CLK).
3Dh (0F7Bh)	REG0F7B	7:0	Default : 0x00 Access : RO, R/W
	GPIO_PM_PAD_PS_61	7	GPIO_61's PAD PS.
	GPIO_PM_PAD_PE_61	6	GPIO_61's PAD PE.
	GPIO_PM_PAD_DRV1_61	5	GPIO_61's PAD DRV1.
	GPIO_PM_PAD_DRV0_61	4	GPIO_61's PAD DRV0.
	-	3:2	Reserved.
	GPIO_PM_WK_FIQ_RAW_ST	1	GPIO_61's FIQ raw status for edge wake-up source.

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	ATUS_61			
	GPIO_PM_WK_FIQ_FINAL_S TATUS_61	0	GPIO_61's FIQ final status for edge wake-up source.	
3Eh (0F7Ch)	REG0F7C	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_62	7	GPIO_62's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_62	6	GPIO_62's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_62	5	GPIO_62's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_62	4	GPIO_62's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_62	3	GPIO_62's glitch remover enable.	
	GPIO_PM_IN_62	2	GPIO_62's input.	
	GPIO_PM_OUT_62	1	GPIO_62's output.	
	GPIO_PM_OEN_62	0	GPIO_62's output enable (PAD_GT1_TX_CTL).	
3Eh (0F7Dh)	REG0F7D	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_62	7	GPIO_62's PAD PS.	
	GPIO_PM_PAD_PE_62	6	GPIO_62's PAD PE.	
	GPIO_PM_PAD_DRV1_62	5	GPIO_62's PAD DRV1.	
	GPIO_PM_PAD_DRV0_62	4	GPIO_62's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_ST ATUS_62	1	GPIO_62's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_S TATUS_62	0	GPIO_62's FIQ final status for edge wake-up source.	
3Fh (0F7Eh)	REG0F7E	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_63	7	GPIO_63's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_63	6	GPIO_63's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_63	5	GPIO_63's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_63	4	GPIO_63's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_63	3	GPIO_63's glitch remover enable.	
	GPIO_PM_IN_63	2	GPIO_63's input.	
	GPIO_PM_OUT_63	1	GPIO_63's output.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_OEN_63	0	GPIO_63's output enable (PAD_GT1_TX_D0).	
3Fh (0F7Fh)	REG0F7F	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_63	7	GPIO_63's PAD PS.	
	GPIO_PM_PAD_PE_63	6	GPIO_63's PAD PE.	
	GPIO_PM_PAD_DRV1_63	5	GPIO_63's PAD DRV1.	
	GPIO_PM_PAD_DRV0_63	4	GPIO_63's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_63	1	GPIO_63's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_63	0	GPIO_63's FIQ final status for edge wake-up source.	
40h (0F80h)	REG0F80	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_64	7	GPIO_64's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_64	6	GPIO_64's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_64	5	GPIO_64's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_64	4	GPIO_64's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_64	3	GPIO_64's glitch remover enable.	
	GPIO_PM_IN_64	2	GPIO_64's input.	
	GPIO_PM_OUT_64	1	GPIO_64's output.	
	GPIO_PM_OEN_64	0	GPIO_64's output enable (PAD_GT1_TX_D1).	
40h (0F81h)	REG0F81	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_64	7	GPIO_64's PAD PS.	
	GPIO_PM_PAD_PE_64	6	GPIO_64's PAD PE.	
	GPIO_PM_PAD_DRV1_64	5	GPIO_64's PAD DRV1.	
	GPIO_PM_PAD_DRV0_64	4	GPIO_64's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_64	1	GPIO_64's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_64	0	GPIO_64's FIQ final status for edge wake-up source.	
41h (0F82h)	REG0F82	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_65	7	GPIO_65's FIQ polarity for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
41h (0F83h)	GPIO_PM_WK_FIQ_CLR_65	6	GPIO_65's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_65	5	GPIO_65's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_65	4	GPIO_65's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_65	3	GPIO_65's glitch remover enable.	
	GPIO_PM_IN_65	2	GPIO_65's input.	
	GPIO_PM_OUT_65	1	GPIO_65's output.	
	GPIO_PM_OEN_65	0	GPIO_65's output enable (PAD_GT1_TX_D2).	
42h (0F84h)	REG0F83	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_65	7	GPIO_65's PAD PS.	
	GPIO_PM_PAD_PE_65	6	GPIO_65's PAD PE.	
	GPIO_PM_PAD_DRV1_65	5	GPIO_65's PAD DRV1.	
	GPIO_PM_PAD_DRV0_65	4	GPIO_65's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_65	1	GPIO_65's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_65	0	GPIO_65's FIQ final status for edge wake-up source.	
	REG0F84	7:0	Default : 0x11	Access : RO, R/W, WO
42h (0F85h)	GPIO_PM_WK_FIQ_POL_66	7	GPIO_66's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_66	6	GPIO_66's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_66	5	GPIO_66's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_66	4	GPIO_66's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_66	3	GPIO_66's glitch remover enable.	
	GPIO_PM_IN_66	2	GPIO_66's input.	
	GPIO_PM_OUT_66	1	GPIO_66's output.	
	GPIO_PM_OEN_66	0	GPIO_66's output enable (PAD_GT1_TX_D3).	
	REG0F85	7:0	Default : 0x00	Access : RO, R/W

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
43h (0F86h)	GPIO_PM_PAD_DRV0_66	4	GPIO_66's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_66	1	GPIO_66's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_66	0	GPIO_66's FIQ final status for edge wake-up source.	
43h (0F86h)	REG0F86	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_67	7	GPIO_67's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_67	6	GPIO_67's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_67	5	GPIO_67's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_67	4	GPIO_67's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_67	3	GPIO_67's glitch remover enable.	
	GPIO_PM_IN_67	2	GPIO_67's input.	
	GPIO_PM_OUT_67	1	GPIO_67's output.	
	GPIO_PM_OEN_67	0	GPIO_67's output enable (PAD_PM_HDMI_CEC).	
43h (0F87h)	REG0F87	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_67	7	GPIO_67's PAD PS.	
	GPIO_PM_PAD_PE_67	6	GPIO_67's PAD PE.	
	GPIO_PM_PAD_DRV1_67	5	GPIO_67's PAD DRV1.	
	GPIO_PM_PAD_DRV0_67	4	GPIO_67's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_67	1	GPIO_67's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_67	0	GPIO_67's FIQ final status for edge wake-up source.	
44h (0F88h)	REG0F88	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_68	7	GPIO_68's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_68	6	GPIO_68's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_68	5	GPIO_68's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_68	4	GPIO_68's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_68	3	GPIO_68's glitch remover enable.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_IN_68	2	GPIO_68's input.	
	GPIO_PM_OUT_68	1	GPIO_68's output.	
	GPIO_PM_OEN_68	0	GPIO_68's output enable (PAD_PM_SPI_WPZ).	
44h (0F89h)	REG0F89	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_68	7	GPIO_68's PAD PS.	
	GPIO_PM_PAD_PE_68	6	GPIO_68's PAD PE.	
	GPIO_PM_PAD_DRV1_68	5	GPIO_68's PAD DRV1.	
	GPIO_PM_PAD_DRV0_68	4	GPIO_68's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_68	1	GPIO_68's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_68	0	GPIO_68's FIQ final status for edge wake-up source.	
45h (0F8Ah)	REG0F8A	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_69	7	GPIO_69's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_69	6	GPIO_69's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_69	5	GPIO_69's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_69	4	GPIO_69's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_69	3	GPIO_69's glitch remover enable.	
	GPIO_PM_IN_69	2	GPIO_69's input.	
	GPIO_PM_OUT_69	1	GPIO_69's output.	
	GPIO_PM_OEN_69	0	GPIO_69's output enable (PAD_PM_SPI_HOLDZ).	
45h (0F8Bh)	REG0F8B	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_69	7	GPIO_69's PAD PS.	
	GPIO_PM_PAD_PE_69	6	GPIO_69's PAD PE.	
	GPIO_PM_PAD_DRV1_69	5	GPIO_69's PAD DRV1.	
	GPIO_PM_PAD_DRV0_69	4	GPIO_69's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_69	1	GPIO_69's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_69	0	GPIO_69's FIQ final status for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
46h (0F8Ch)	REG0F8C	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_70	7	GPIO_70's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_70	6	GPIO_70's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_70	5	GPIO_70's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_70	4	GPIO_70's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_70	3	GPIO_70's glitch remover enable.	
	GPIO_PM_IN_70	2	GPIO_70's input.	
	GPIO_PM_OUT_70	1	GPIO_70's output.	
	GPIO_PM_OEN_70	0	GPIO_70's output enable (PAD_PM_SPI_RSTZ).	
46h (0F8Dh)	REG0F8D	7:0	Default : 0x00	Access : RO, R/W
	GPIO_PM_PAD_PS_70	7	GPIO_70's PAD PS.	
	GPIO_PM_PAD_PE_70	6	GPIO_70's PAD PE.	
	GPIO_PM_PAD_DRV1_70	5	GPIO_70's PAD DRV1.	
	GPIO_PM_PAD_DRV0_70	4	GPIO_70's PAD DRV0.	
	-	3:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_STATUS_70	1	GPIO_70's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_STATUS_70	0	GPIO_70's FIQ final status for edge wake-up source.	
47h (0F8Eh)	REG0F8E	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_71	7	GPIO_71's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_71	6	GPIO_71's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_71	5	GPIO_71's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_71	4	GPIO_71's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_71	3	GPIO_71's glitch remover enable.	
	GPIO_PM_IN_71	2	GPIO_71's input.	
	GPIO_PM_OUT_71	1	GPIO_71's output.	
	GPIO_PM_OEN_71	0	GPIO_71's output enable (PAD_PM_SD_CDZ).	
47h (0F8Fh)	REG0F8F	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_WK_FIQ_RAW_ST ATUS_71	1	GPIO_71's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_S TATUS_71	0	GPIO_71's FIQ final status for edge wake-up source.	
48h (0F90h)	REG0F90	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_72	7	GPIO_72's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_72	6	GPIO_72's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_72	5	GPIO_72's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_72	4	GPIO_72's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_72	3	GPIO_72's glitch remover enable.	
	GPIO_PM_IN_72	2	GPIO_72's input.	
	GPIO_PM_OUT_72	1	GPIO_72's output.	
	GPIO_PM_OEN_72	0	GPIO_72's output enable (PAD_VID0).	
48h (0F91h)	REG0F91	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_ST ATUS_72	1	GPIO_72's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_S TATUS_72	0	GPIO_72's FIQ final status for edge wake-up source.	
49h (0F92h)	REG0F92	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_73	7	GPIO_73's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_73	6	GPIO_73's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_73	5	GPIO_73's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_73	4	GPIO_73's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_73	3	GPIO_73's glitch remover enable.	
	GPIO_PM_IN_73	2	GPIO_73's input.	
	GPIO_PM_OUT_73	1	GPIO_73's output.	
	GPIO_PM_OEN_73	0	GPIO_73's output enable (PAD_VID1).	
49h (0F93h)	REG0F93	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_ST	1	GPIO_73's FIQ raw status for edge wake-up source.	

**PM_GPIO Register (Bank = 0F)**

Index (Absolute)	Mnemonic	Bit	Description	
	ATUS_73			
	GPIO_PM_WK_FIQ_FINAL_S TATUS_73	0	GPIO_73's FIQ final status for edge wake-up source.	
4Ah (0F94h)	REG0F94	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_74	7	GPIO_74's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_74	6	GPIO_74's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_74	5	GPIO_74's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_74	4	GPIO_74's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_74	3	GPIO_74's glitch remover enable.	
	GPIO_PM_IN_74	2	GPIO_74's input.	
	GPIO_PM_OUT_74	1	GPIO_74's output.	
	GPIO_PM_OEN_74	0	GPIO_74's output enable (PAD_LED0).	
4Ah (0F95h)	REG0F95	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_ST ATUS_74	1	GPIO_74's FIQ raw status for edge wake-up source.	
	GPIO_PM_WK_FIQ_FINAL_S TATUS_74	0	GPIO_74's FIQ final status for edge wake-up source.	
4Bh (0F96h)	REG0F96	7:0	Default : 0x11	Access : RO, R/W, WO
	GPIO_PM_WK_FIQ_POL_75	7	GPIO_75's FIQ polarity for edge wake-up source.	
	GPIO_PM_WK_FIQ_CLR_75	6	GPIO_75's FIQ clear for edge wake-up source.	
	GPIO_PM_WK_FIQ_FORCE_75	5	GPIO_75's FIQ force for edge wake-up source.	
	GPIO_PM_WK_FIQ_MASK_75	4	GPIO_75's FIQ mask for edge wake-up source.	
	GPIO_PM_GLHRM_EN_75	3	GPIO_75's glitch remover enable.	
	GPIO_PM_IN_75	2	GPIO_75's input.	
	GPIO_PM_OUT_75	1	GPIO_75's output.	
	GPIO_PM_OEN_75	0	GPIO_75's output enable (PAD_LED1).	
4Bh (0F97h)	REG0F97	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	GPIO_PM_WK_FIQ_RAW_ST ATUS_75	1	GPIO_75's FIQ raw status for edge wake-up source.	



PM_GPIO Register (Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_PM_WK_FIQ_FINAL_S TATUS_75	0	GPIO_75's FIQ final status for edge wake-up source.	
7Eh (0FFCh)	REG0FFC	7:0	Default : 0x00	Access : R/W
	RESERVE5[7:0]	7:0	RESERVE5 (for HW ECO ONLY). [1:0]: for GCR_PWRGD_LVL_H. [15:2]: reserved.	
7Eh (0FFDh)	REG0FFD	7:0	Default : 0x00	Access : R/W
	RESERVE5[15:8]	7:0	See description of '0FFCh'.	
7Fh (0FFEh)	REG0FFE	7:0	Default : 0xFF	Access : R/W
	RESERVE6[7:0]	7:0	RESERVE6 (for HW ECO ONLY).	
7Fh (0FFFh)	REG0FFF	7:0	Default : 0xFF	Access : R/W
	RESERVE6[15:8]	7:0	See description of '0FFEh'.	

PM_SAR Register (Bank = 14)

PM_SAR Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1400h)	REG1400	7:0	Default : 0x40	Access : R/W
	SAR_START	7	SAR start signal.	
	SAR_PD	6	SAR digital power down.	
	SAR_MODE	5	Select SAR digital operation mode. 0: One-shot. 1: Freerun.	
	SINGLE	4	Enable SINGLE channel mode. 0: Disable. 1: Enable.	
	KEYPAD_LEVEL	3	Level of keypad.	
	SAR_SINGLE_CH[2:0]	2:0	Select channel for single channel mode.	
	REG1401	7:0	Default : 0x09	Access : R/W
00h (1401h)	-	7:4	Reserved.	
	SAR_8CH_EN	3	1: SAR 8 channel. 0: SAR 4 channel.	
	SAR_SEL	2	SAR selection.	

**PM_SAR Register (Bank = 14)**

Index (Absolute)	Mnemonic	Bit	Description	
01h (1402h)	SAR_FREERUN	1	SAR atop freerun mode. 0: Controlled by digital (default). 1: Freerun.	
	SARADC_PD	0	SAR atop power down. 1: Power down. 0: Enable SAR atop.	
02h (1404h)	REG1402	7:0	Default : 0x00	Access : R/W
	CKSAMP_PRD[7:0]	7:0	CKSAMP_PRD.	
02h (1404h)	REG1404	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
02h (1405h)	GCR_SAR_CH8_MUXSEL[2:0]	2:0	SAR CH8 input MUX selection.]	
	REG1405	7:0	Default : 0x00	Access : R/W
10h (1420h)	-	7:1	Reserved.	
	GCR_SAR_CH8_EN	0	0: SAR channel = CH0~CH7 decided by GCR_SAR_CHSEL. 1: SAR channel = CH8.	
10h (1420h)	REG1420	7:0	Default : 0x00	Access : R/W
	PM_DMY[7:0]	7:0		
11h (1422h)	REG1422	7:0	Default : 0x3F	Access : R/W
	-	7:6	Reserved.	
11h (1423h)	SAR_AISEL[5:0]	5:0	Pad GPIO/Ain switch: 1: Analog input. 0: GPIO.	
	REG1423	7:0	Default : 0x3F	Access : R/W
11h (1423h)	-	7:6	Reserved.	
	OEN_SAR_GPIO[5:0]	5:0	Output enable for GPIO pad. 0: Enable. 1: Disable.	
12h (1424h)	REG1424	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
12h (1425h)	I_SAR_GPIO[5:0]	5:0	Output data for GPIO pad.	
	REG1425	7:0	Default : 0x00	Access : RO
12h (1425h)	-	7:6	Reserved.	
	C_SAR_GPIO[5:0]	5:0	Input data for GPIO pad.	
13h	REG1426	7:0	Default : 0x00	Access : R/W

**PM_SAR Register (Bank = 14)**

Index (Absolute)	Mnemonic	Bit	Description	
(1426h)	SAR_TEST[7:0]	7:0	SAR ADC test mode control.	
13h (1427h)	REG1427	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_TEST[9:8]	1:0	See description of '1426h'.	
14h (1428h)	REG1428	7:0	Default : 0xFF	Access : R/W
	SAR_INT_MASK[7:0]	7:0	Interrupt mask for sar_int. 0: Enable. 1: Disable.	
14h (1429h)	REG1429	7:0	Default : 0x01	Access : R/W
	-	7:1	Reserved.	
	SAR_INT_MASK[8]	0	See description of '1428h'.	
15h (142Ah)	REG142A	7:0	Default : 0x00	Access : WO
	SAR_INT_CLR[7:0]	7:0	Interrupt clear for sar_int.	
15h (142Bh)	REG142B	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	SAR_INT_CLR[8]	0	See description of '142Ah'.	
16h (142Ch)	REG142C	7:0	Default : 0x00	Access : R/W
	SAR_INT_FORCE[7:0]	7:0	Force interrupt for sar_int.	
16h (142Dh)	REG142D	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SAR_INT_FORCE[8]	0	See description of '142Ch'.	
17h (142Eh)	REG142E	7:0	Default : 0x00	Access : RO
	SAR_INT_STATUS[7:0]	7:0	Status of sar_int.	
17h (142Fh)	REG142F	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	SAR_INT_STATUS[8]	0	See description of '142Eh'.	
18h (1430h)	REG1430	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_RDY	1	SAR ready signal.	
	CMP_OUT	0	SAR compare out signal.	
19h (1432h)	REG1432	7:0	Default : 0x1F	Access : R/W
	SAR_CH8_REF_V_SEL	7	Channel 8 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH7_REF_V_SEL	6	Channel 7 reference voltage select (0: 2.0V, 1: 3.3V).	

**PM_SAR Register (Bank = 14)**

Index (Absolute)	Mnemonic	Bit	Description	
20h (1440h)	SAR_CH6_REF_V_SEL	5	Channel 6 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH5_REF_V_SEL	4	Channel 5 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH4_REF_V_SEL	3	Channel 4 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH3_REF_V_SEL	2	Channel 3 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH2_REF_V_SEL	1	Channel 2 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH1_REF_V_SEL	0	Channel 1 reference voltage select (0: 2.0V, 1: 3.3V).	
20h (1441h)	REG1440	7:0	Default : 0x00	Access : R/W
	SAR_CH1_UPB[7:0]	7:0	Channel 1 upper bound.	
20h (1441h)	REG1441	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH1_UPB[9:8]	1:0	See description of '1440h'.	
21h (1442h)	REG1442	7:0	Default : 0x00	Access : R/W
	SAR_CH2_UPB[7:0]	7:0	Channel 2 upper bound.	
21h (1443h)	REG1443	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH2_UPB[9:8]	1:0	See description of '1442h'.	
22h (1444h)	REG1444	7:0	Default : 0x00	Access : R/W
	SAR_CH3_UPB[7:0]	7:0	Channel 3 upper bound.	
22h (1445h)	REG1445	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH3_UPB[9:8]	1:0	See description of '1444h'.	
23h (1446h)	REG1446	7:0	Default : 0x00	Access : R/W
	SAR_CH4_UPB[7:0]	7:0	Channel 4 upper bound.	
23h (1447h)	REG1447	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH4_UPB[9:8]	1:0	See description of '1446h'.	
24h (1448h)	REG1448	7:0	Default : 0x00	Access : R/W
	SAR_CH5_UPB[7:0]	7:0	Channel 5 upper bound.	
24h (1449h)	REG1449	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH5_UPB[9:8]	1:0	See description of '1448h'.	
25h (144Ah)	REG144A	7:0	Default : 0x00	Access : R/W
	SAR_CH6_UPB[7:0]	7:0	Channel 6 upper bound.	

**PM_SAR Register (Bank = 14)**

Index (Absolute)	Mnemonic	Bit	Description	
25h (144Bh)	REG144B	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH6_UPB[9:8]	1:0	See description of '144Ah'.	
26h (144Ch)	REG144C	7:0	Default : 0x00	Access : R/W
	SAR_CH7_UPB[7:0]	7:0	Channel 7 upper bound.	
26h (144Dh)	REG144D	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH7_UPB[9:8]	1:0	See description of '144Ch'.	
27h (144Eh)	REG144E	7:0	Default : 0x00	Access : R/W
	SAR_CH8_UPB[7:0]	7:0	Channel 8 upper bound.	
27h (144Fh)	REG144F	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH8_UPB[9:8]	1:0	See description of '144Eh'.	
30h (1460h)	REG1460	7:0	Default : 0x00	Access : R/W
	SAR_CH1_LOB[7:0]	7:0	Channel 1 lower bound.	
30h (1461h)	REG1461	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH1_LOB[9:8]	1:0	See description of '1460h'.	
31h (1462h)	REG1462	7:0	Default : 0x00	Access : R/W
	SAR_CH2_LOB[7:0]	7:0	Channel 2 lower bound.	
31h (1463h)	REG1463	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH2_LOB[9:8]	1:0	See description of '1462h'.	
32h (1464h)	REG1464	7:0	Default : 0x00	Access : R/W
	SAR_CH3_LOB[7:0]	7:0	Channel 3 lower bound.	
32h (1465h)	REG1465	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH3_LOB[9:8]	1:0	See description of '1464h'.	
33h (1466h)	REG1466	7:0	Default : 0x00	Access : R/W
	SAR_CH4_LOB[7:0]	7:0	Channel 4 lower bound.	
33h (1467h)	REG1467	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH4_LOB[9:8]	1:0	See description of '1466h'.	

**PM_SAR Register (Bank = 14)**

Index (Absolute)	Mnemonic	Bit	Description	
34h (1468h)	REG1468	7:0	Default : 0x00	Access : R/W
	SAR_CH5_LOB[7:0]	7:0	Channel 5 lower bound.	
34h (1469h)	REG1469	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH5_LOB[9:8]	1:0	See description of '1468h'.	
35h (146Ah)	REG146A	7:0	Default : 0x00	Access : R/W
	SAR_CH6_LOB[7:0]	7:0	Channel 6 lower bound.	
35h (146Bh)	REG146B	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH6_LOB[9:8]	1:0	See description of '146Ah'.	
36h (146Ch)	REG146C	7:0	Default : 0x00	Access : R/W
	SAR_CH7_LOB[7:0]	7:0	Channel 7 lower bound.	
36h (146Dh)	REG146D	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH7_LOB[9:8]	1:0	See description of '146Ch'.	
37h (146Eh)	REG146E	7:0	Default : 0x00	Access : R/W
	SAR_CH8_LOB[7:0]	7:0	Channel 8 lower bound.	
37h (146Fh)	REG146F	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH8_LOB[9:8]	1:0	See description of '146Eh'.	
40h (1480h)	REG1480	7:0	Default : 0x00	Access : RO
	SAR_ADC_CH1_DATA[7:0]	7:0	SAR ADC output 1.	
40h (1481h)	REG1481	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_ADC_CH1_DATA[9:8]	1:0	See description of '1480h'.	
41h (1482h)	REG1482	7:0	Default : 0x00	Access : RO
	SAR_ADC_CH2_DATA[7:0]	7:0	SAR ADC output 2.	
41h (1483h)	REG1483	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_ADC_CH2_DATA[9:8]	1:0	See description of '1482h'.	
42h (1484h)	REG1484	7:0	Default : 0x00	Access : RO
	SAR_ADC_CH3_DATA[7:0]	7:0	SAR ADC output 3.	
42h	REG1485	7:0	Default : 0x00	Access : RO

**PM_SAR Register (Bank = 14)**

Index (Absolute)	Mnemonic	Bit	Description
(1485h)	-	7:2	Reserved.
	SAR_ADC_CH3_DATA[9:8]	1:0	See description of '1484h'.
43h (1486h)	REG1486	7:0	Default : 0x00
	SAR_ADC_CH4_DATA[7:0]	7:0	SAR ADC output 4.
43h (1487h)	REG1487	7:0	Default : 0x00
	-	7:2	Reserved.
	SAR_ADC_CH4_DATA[9:8]	1:0	See description of '1486h'.
44h (1488h)	REG1488	7:0	Default : 0x00
	SAR_ADC_CH5_DATA[7:0]	7:0	SAR ADC output 5.
44h (1489h)	REG1489	7:0	Default : 0x00
	-	7:2	Reserved.
	SAR_ADC_CH5_DATA[9:8]	1:0	See description of '1488h'.
45h (148Ah)	REG148A	7:0	Default : 0x00
	SAR_ADC_CH6_DATA[7:0]	7:0	SAR ADC output 6.
45h (148Bh)	REG148B	7:0	Default : 0x00
	-	7:2	Reserved.
	SAR_ADC_CH6_DATA[9:8]	1:0	See description of '148Ah'.
46h (148Ch)	REG148C	7:0	Default : 0x00
	SAR_ADC_CH7_DATA[7:0]	7:0	SAR ADC output 7.
46h (148Dh)	REG148D	7:0	Default : 0x00
	-	7:2	Reserved.
	SAR_ADC_CH7_DATA[9:8]	1:0	See description of '148Ch'.
47h (148Eh)	REG148E	7:0	Default : 0x00
	SAR_ADC_CH8_DATA[7:0]	7:0	SAR ADC output 8.
47h (148Fh)	REG148F	7:0	Default : 0x00
	-	7:2	Reserved.
	SAR_ADC_CH8_DATA[9:8]	1:0	See description of '148Eh'.
50h (14A0h)	REG14A0	7:0	Default : 0x0C
	SMCARD_INT_TIME_CNT_H[3:0]	7:4	Smcard power_good interrupt time count for high pulse.
	SMCARD_INT_LEVEL	3	Select smcard power_good interrupt level. 1'b0: active low. 1'b1: active high.
	SMCARD_INT_SEL[2:0]	2:0	Select smcard power_good interrupt from:

**PM_SAR Register (Bank = 14)**

Index (Absolute)	Mnemonic	Bit	Description	
			3'b000: channel 1. 3'b001: channel 2. 3'b010: channel 3. 3'b011: channel 4. 3'b100: VPLUG_IN_PWRGD of pm_sar_atop.	
50h (14A1h)	REG14A1	7:0	Default : 0x00	Access : RO, R/W
	-	7	Reserved.	
	SMCARD_INT	6	Smcard power_good post interrupt time.	
	SMCARD_INT_PULSE	5	Smcard power_good pre interrupt time count.	
	SMCARD_INT_TIME_CNT_EN	4	Smcard power_good interrupt time count enable.	
	SMCARD_INT_TIME_CNT_L[3:0]	3:0	Smcard power_good interrupt time count for low pulse.	
51h (14A2h)	REG14A2	7:0	Default : 0x0C	Access : R/W
	FCIE_INT_TIME_CNT_H[3:0]	7:4	Fcie power_good interrupt time count for high pulse.	
	FCIE_INT_LEVEL	3	Select fcie power_good interrupt level. 1'b0: active low. 1'b1: active high.	
	FCIE_INT_SEL[2:0]	2:0	Select fcie power_good interrupt from: 3'b000: channel 1. 3'b001: channel 2. 3'b010: channel 3. 3'b011: channel 4. 3'b100: VPLUG_IN_PWRGD of pm_sar_atop.	
51h (14A3h)	REG14A3	7:0	Default : 0x00	Access : RO, R/W
	-	7	Reserved.	
	FCIE_INT	6	Fcie power_good post interrupt time.	
	FCIE_INT_PULSE	5	Fcie power_good pre interrupt time count.	
	FCIE_INT_TIME_CNT_EN	4	Fcie power_good interrupt time count enable.	
	FCIE_INT_TIME_CNT_L[3:0]	3:0	Fcie power_good interrupt time count for low pulse.	
60h (14C0h)	REG14C0	7:0	Default : 0x02	Access : R/W
	-	7:3	Reserved.	
	SAR_INT_DIRECT2TOP_SEL[2:0]	2:0	Select sar_channel interrupt direct connection to intr_ctrl_top. 3'd0: channel 1.	



PM_SAR Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
			3'd1: channel 2. 3'd2: channel 3. 3'd3: channel 4. 3'd4: channel 5. 3'd5: channel 6. 3'd6: channel 7. 3'd7: channel 8.	
70h (14E0h)	REG14E0	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	TSEN_PROCESS_CODE[3:0]	3:0	Pm_sar_atop tsensor process code.	

PM_SAR Register (Bank = 14)

PM_SAR Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
00h (1401h)	REG1401	7:0	Default : 0x00	Access : R/W, WO
	-	7	Reserved.	
	SAR_LOAD_EN	6	Enable load SAR code.	
	-	5	Reserved.	
	SAR_SW_RST	4	Software reset (active high) for sar_top.	
	-	3:0	Reserved.	

QSPI Register (Bank = 17)

QSPI Register (Bank = 17)

Index (Absolute)	Mnemonic	Bit	Description	
00h (1700h)	REG1700	7:0	Default : 0x00	Access : R/W
	MASK_GRANT[7:0]	7:0		
01h (1702h)	REG1702	7:0	Default : 0x00	Access : R/W
	MASK_TIME_OUT_CTRL[7:0]	7:0		
02h (1705h)	REG1705	7:0	Default : 0x00	Access : RO
	MASK_TIME_OUT_STATUS[7]	7:0		

**QSPI Register (Bank = 17)**

Index (Absolute)	Mnemonic	Bit	Description	
	:0]			
03h (1706h)	REG1706	7:0	Default : 0x00	Access : R/W
	MASK_TIME_OUT_LEN[7:0]	7:0		
03h (1707h)	REG1707	7:0	Default : 0x00	Access : R/W
	MASK_TIME_OUT_LEN[15:8]]	7:0	See description of '1706h'.	
04h (1708h)	REG1708	7:0	Default : 0x00	Access : R/W
	MASK_TIME_OUT_LEN[23:1] 6]	7:0	See description of '1706h'.	
04h (1709h)	REG1709	7:0	Default : 0x10	Access : R/W
	MASK_TIME_OUT_LEN[31:2] 4]	7:0	See description of '1706h'.	
05h (170Ah)	REG170A	7:0	Default : 0x00	Access : RO
	MASK_TIME_OUT_CNT[7:0]	7:0		
05h (170Bh)	REG170B	7:0	Default : 0x00	Access : RO
	MASK_TIME_OUT_CNT[15:8]]	7:0	See description of '170Ah'.	
06h (170Ch)	REG170C	7:0	Default : 0x00	Access : RO
	MASK_TIME_OUT_CNT[23:1] 6]	7:0	See description of '170Ah'.	
06h (170Dh)	REG170D	7:0	Default : 0x00	Access : RO
	MASK_TIME_OUT_CNT[31:2] 4]	7:0	See description of '170Ah'.	
07h (170Eh)	REG170E	7:0	Default : 0x00	Access : R/W
	SPI_ARB_CTRL[7:0]	7:0	[0]: Non_pm_ack timeout_en.	
07h (170Fh)	REG170F	7:0	Default : 0x00	Access : RO
	SPI_ARB_STATUS[7:0]	7:0	[0]: Reg_non_pm_ack timeout_flag.	
08h (1710h)	REG1710	7:0	Default : 0xFF	Access : R/W
	NON_PM_ACK_TIMEOUT_LE N[7:0]	7:0		
08h (1711h)	REG1711	7:0	Default : 0x01	Access : R/W
	NON_PM_ACK_TIMEOUT_LE N[15:8]	7:0	See description of '1710h'.	
09h (1712h)	REG1712	7:0	Default : 0x00	Access : RO
	NON_PM_ACK_TIMEOUT_CN	7:0		

**QSPI Register (Bank = 17)**

Index (Absolute)	Mnemonic	Bit	Description	
	T[7:0]			
09h (1713h)	REG1713	7:0	Default : 0x00	Access : RO
	NON_PM_ACK_TIMEOUT_CN T[15:8]	7:0	See description of '1712h'.	
0Ah (1714h)	REG1714	7:0	Default : 0x02	Access : R/W
	SPI_SW_MODE[7:0]	7:0	[0]: CS SW mode enable. [1]: CS SW control 0: CS = 0, 1: CS = 1.	
40h (1780h)	REG1780	7:0	Default : 0x04	Access : R/W
	-	7:3	Reserved.	
	DELAY_TREE_SEL[2:0]	2:0	Value of the delay tree.	
50h (17A0h)	REG17A0	7:0	Default : 0x00	Access : R/W
	CMD_111_M0[7:0]	7:0	User-defined command for 1-1-1 normal read mode.	
50h (17A1h)	REG17A1	7:0	Default : 0x00	Access : R/W
	CMD_111_M1[7:0]	7:0	User-defined command for 1-1-1 fast read mode.	
51h (17A2h)	REG17A2	7:0	Default : 0x00	Access : R/W
	CMD_112[7:0]	7:0	User-defined command for 1-1-2 read mode.	
51h (17A3h)	REG17A3	7:0	Default : 0x00	Access : R/W
	CMD_122[7:0]	7:0	User-defined command for 1-2-2 read mode.	
52h (17A4h)	REG17A4	7:0	Default : 0x00	Access : R/W
	CMD_114[7:0]	7:0	User-defined command for 1-1-4 read mode.	
52h (17A5h)	REG17A5	7:0	Default : 0x00	Access : R/W
	CMD_144[7:0]	7:0	User-defined command for 1-4-4 read mode.	
53h (17A6h)	REG17A6	7:0	Default : 0x00	Access : R/W
	CMD_444_M0[7:0]	7:0	User-defined command for 4-4-4 read mode (dummy cycle = 4).	
53h (17A7h)	REG17A7	7:0	Default : 0x00	Access : R/W
	CMD_444_M1[7:0]	7:0	User-defined command for 4-4-4 read mode (dummy cycle = 6).	
54h (17A8h)	REG17A8	7:0	Default : 0x00	Access : R/W
	DUMMY_CYC_VAL[7:0]	7:0	User-defined dummy cycle value.	
54h (17A9h)	REG17A9	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	WRAP_VAL[3:0]	3:0	User-defined wrap value for SPI NAND.	

**QSPI Register (Bank = 17)**

Index (Absolute)	Mnemonic	Bit	Description	
58h (17B0h)	REG17B0	7:0	Default : 0x00	Access : R/W
	2_CMD_111_M0[7:0]	7:0	User-defined command for 1-1-1 normal read mode for CS1.	
58h (17B1h)	REG17B1	7:0	Default : 0x00	Access : R/W
	2_CMD_111_M1[7:0]	7:0	User-defined command for 1-1-1 fast read mode for CS1.	
59h (17B2h)	REG17B2	7:0	Default : 0x00	Access : R/W
	2_CMD_112[7:0]	7:0	User-defined command for 1-1-2 read mode for CS1.	
59h (17B3h)	REG17B3	7:0	Default : 0x00	Access : R/W
	2_CMD_122[7:0]	7:0	User-defined command for 1-2-2 read mode for CS1.	
5Ah (17B4h)	REG17B4	7:0	Default : 0x00	Access : R/W
	2_CMD_114[7:0]	7:0	User-defined command for 1-1-4 read mode for CS1.	
5Ah (17B5h)	REG17B5	7:0	Default : 0x00	Access : R/W
	2_CMD_144[7:0]	7:0	User-defined command for 1-4-4 read mode for CS1.	
5Bh (17B6h)	REG17B6	7:0	Default : 0x00	Access : R/W
	2_CMD_444_M0[7:0]	7:0	User-defined command for 4-4-4 read mode for CS1 (dummy cycle = 4).	
5Bh (17B7h)	REG17B7	7:0	Default : 0x00	Access : R/W
	2_CMD_444_M1[7:0]	7:0	User-defined command for 4-4-4 read mode for CS1 (dummy cycle = 6).	
5Ch (17B8h)	REG17B8	7:0	Default : 0x00	Access : R/W
	2_DUMMY_CYC_VAL[7:0]	7:0	User-defined dummy cycle value for CS1.	
5Ch (17B9h)	REG17B9	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	2_WRAP_VAL[3:0]	3:0	User-defined wrap value for SPI NAND.	
60h (17C0h)	REG17C0	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SECOND_CKG_SPI[6:0]	6:0	Bit[3:0]: user-defined dummy cycle number for CS1. Bit[4]: user-defined dummy cycle mode enable for CS1. 0: Disable. 1: Enable.	
60h (17C1h)	REG17C1	7:0	Default : 0x00	Access : R/W
	SECOND_CFG_QSPI[7:0]	7:0	Bit[8]: CMD_Bypass_Mode for CS1. Bit[11]: 3/4 byte address mode. 0: 3-byte. 1: 4-byte.	

**QSPI Register (Bank = 17)**

Index (Absolute)	Mnemonic	Bit	Description	
61h (17C2h)	REG17C2	7:0	Default : 0x1A	Access : R/W
	SECOND_CSZ_SETUP[3:0]	7:4	CSZ setup time for CS1 (relative to SCK). 4'h0: 1 SPI clock cycle. 4'h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
	SECOND_CSZ_HIGH[3:0]	3:0	CSZ deselect time for CS1 (SCZ = high). 4'h0: 1 SPI clock cycle. 4'h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
61h (17C3h)	REG17C3	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	SECOND_CSZ_HOLD[3:0]	3:0	CSZ hold time for CS1 (relative to SCK). 4'h0: 1 SPI clock cycle. 4'h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
62h (17C4h)	REG17C4	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	SECOND_MODE_SEL[3:0]	3:0	Second SPI model select for CS1. 0x0: Normal mode (1-1-1), (SPI command is 0x03). 0x1: Enable fast read mode (1-1-1), (SPI command is 0x0B). 0x2: Enable (1-1-2) mode, (SPI command is 0x3B). 0x3: Enable (1-2-2) mode, (SPI command is 0xBB). 0xa: Enable (1-1-4) mode, (SPI command is 0x6B). 0xb: Enable (1-4-4) mode, (SPI command is 0xEB). 0xc: Enable (4-4-4) mode with 4 dummy cycles, (SPI command is 0x0B). 0xd: Enable (4-4-4) mode with 6 dummy cycles, (SPI command is 0xEB).	
63h (17C6h)	REG17C6	7:0	Default : 0x00	Access : R/W
	SECOND_REPLACED_CMD[7:0]	7:0	The second replaced command for CS1.	
64h (17C8h)	REG17C8	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CLK_DIV_CNT_EN	3	SPI receive div. counter enable.	
	CLK_DIV_CNT_SEL[2:0]	2:0	SPI receive div. counter output mux select.	
66h	REG17CC	7:0	Default : 0xFF	Access : R/W

**QSPI Register (Bank = 17)**

Index (Absolute)	Mnemonic	Bit	Description	
(17CCh)	TIMEOUT_CNT_VALUE[7:0]	7:0	Timeout counter value.	
66h (17CDh)	REG17CD	7:0	Default : 0xFF	Access : R/W
	TIMEOUT_CNT_VALUE[15:8]	7:0	See description of '17CCh'.	
67h (17CEh)	REG17CE	7:0	Default : 0xFF	Access : R/W
	TIMEOUT_CNT_VALUE[23:16]	7:0	See description of '17CCh'.	
67h (17CFh)	REG17CF	7:0	Default : 0x40	Access : R/W
	TIMEOUT_CNT_EN	7	Timeout counter enable.	
	TIMEOUT_CNT_RST	6	Timeout counter reset.	
	-	5:0	Reserved.	
68h (17D0h)	REG17D0	7:0	Default : 0x00	Access : R/W
	CSZ_REPLACE_VAL[3:0]	7:4	CSZ signal replaced by register value. B0: CS0 replace value. B1: CS1 replace value. B2: CS2 replace value. B3: CS3 replace value.	
	CSZ_REPLACE_EN[3:0]	3:0	Enable function for CSZ signal replacement by register value. B0: CS0 replace enable. B1: CS1 replace enable. B2: CS2 replace enable. B3: CS3 replace enable.	
6Dh (17DAh)	REG17DA	7:0	Default : 0x1A	Access : R/W
	FSP_CSZ_SETUP[3:0]	7:4	CSZ setup time for FSP (relative to SCK). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
	FSP_CSZ_HIGH[3:0]	3:0	CSZ deselect time for FSP (SCZ = high). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
6Dh (17DBh)	REG17DB	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	FSP_CSZ_HOLD[3:0]	3:0	CSZ hold time for FSP (relative to SCK). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	

**QSPI Register (Bank = 17)**

Index (Absolute)	Mnemonic	Bit	Description	
6Eh (17DCh)	REG17DC	7:0	Default : 0x1A	Access : R/W
	FSP2_CSZ_SETUP[3:0]	7:4	CSZ setup time for FSP2 (relative to SCK). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
	FSP2_CSZ_HIGH[3:0]	3:0	CSZ deselect time for FSP2 (SCZ = high). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
6Eh (17DDh)	REG17DD	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	FSP2_CSZ_HOLD[3:0]	3:0	CSZ hold time for FSP2 (relative to SCK). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
70h (17E0h)	REG17E0	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CKG_SPI[6:0]	6:0	Bit[3:0]: user-defined dummy cycle number. Bit[4]: user-defined dummy cycle mode enable. 0: Disable. 1: Enable. Bit[5]: Force to disable address continue at FSP mode. 0: Disable. 1: Enable.	
70h (17E1h)	REG17E1	7:0	Default : 0x00	Access : R/W
	CFG_QSPI[7:0]	7:0	Bit[8]: CMD_Bypass_Mode. Bit[9]: disable address continue. Bit[10]: wait FSP done. Bit[11]: 3/4 byte address mode. 0: 3-byte. 1: 4-byte.	
71h (17E2h)	REG17E2	7:0	Default : 0x1A	Access : R/W
	CSZ_SETUP[3:0]	7:4	CSZ setup time (relative to SCK). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
	CSZ_HIGH[3:0]	3:0	CSZ deselect time (SCZ = high). 4'h0: 1 SPI clock cycle.	

**QSPI Register (Bank = 17)**

Index (Absolute)	Mnemonic	Bit	Description	
			4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
71h (17E3h)	REG17E3	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CSZ_HOLD[3:0]	3:0	CSZ hold time (relative to SCK). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
72h (17E4h)	REG17E4	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	MODE_SEL[3:0]	3:0	SPI model select (command-address-data). 0x0: Normal mode (1-1-1), (SPI command is 0x03). 0x1: Enable fast read mode (1-1-1), (SPI command is 0x0B). 0x2: Enable (1-1-2) mode, (SPI command is 0x3B). 0x3: Enable (1-2-2) mode, (SPI command is 0xBB). 0xa: Enable (1-1-4) mode, (SPI command is 0x6B). 0xb: Enable (1-4-4) mode, (SPI command is 0xEB). 0xc: Enable (4-4-4) mode with 4 dummy cycles, (SPI command is 0x0B). 0xd: Enable (4-4-4) mode with 6 dummy cycles, (SPI command is 0xEB).	
73h (17E6h)	REG17E6	7:0	Default : 0x00	Access : R/W
	REPLACED_CMD[7:0]	7:0	The replaced command.	
74h (17E8h)	REG17E8	7:0	Default : 0x00	Access : R/W
	SPARE_0[7:0]	7:0	Bit[0]: wrap mode for CS0 flash, for SW to write when the flash enters into wrap mode. 0: Not wrap mode. 1: Wrap mode. Bit[1]: wrap 16 bytes for CS0 flash, for SW to write. 0: Not 16 byte. 1: 16 byte. Bit[2]: wrap 32 bytes for CS0 flash, for SW to write. 0: Not 32 byte. 1: 32 byte. Bit[3]: wrap 64 bytes for CS0 flash, for SW to write. 0: Not 64 byte. 1: 64 byte.	

**QSPI Register (Bank = 17)**

Index (Absolute)	Mnemonic	Bit	Description	
			Bit[4]: wrap 128 bytes for CS0 flash, for SW to write. 0: Not 128 byte. 1: 128 byte. Bit[7:5]: reserved, keep the data as default value. Bit[8]: wrap mode for CS1 flash, for SW to write when the flash enters into wrap mode. 0: Not wrap mode. 1: Wrap mode. Bit[9]: wrap 16 bytes for CS1 flash, for SW to write. 0: Not 16 byte. 1: 16 byte. Bit[10]: wrap 32 bytes for CS1 flash, for SW to write. 0: Not 32 byte. 1: 32 byte. Bit[11]: wrap 64 bytes for CS1 flash, for SW to write. 0: Not 64 byte. 1: 64 byte. Bit[12]: wrap 128 bytes for CS1 flash, for SW to write. 0: Not 128 byte. 1: 128 byte. Bit[15:13]: reserved, keep the data as default value.	
74h (17E9h)	REG17E9	7:0	Default : 0x00	Access : R/W
	SPARE_0[15:8]	7:0	See description of '17E8h'.	
76h (17ECh)	REG17EC	7:0	Default : 0x00	Access : RO
	DEBUG_BUS_0[7:0]	7:0	DEBUG_BUS_0.	
76h (17EDh)	REG17ED	7:0	Default : 0x00	Access : RO
	DEBUG_BUS_0[15:8]	7:0	See description of '17ECh'.	
77h (17EEh)	REG17EE	7:0	Default : 0x00	Access : RO
	DEBUG_BUS_1[7:0]	7:0	DEBUG_BUS_1.	
77h (17EFh)	REG17EF	7:0	Default : 0x00	Access : RO
	DEBUG_BUS_1[15:8]	7:0	See description of '17EEh'.	
78h (17F0h)	REG17F0	7:0	Default : 0x00	Access : RO
	DEBUG_BUS_2[7:0]	7:0	DEBUG_BUS_2.	
78h (17F1h)	REG17F1	7:0	Default : 0x00	Access : RO
	DEBUG_BUS_2[15:8]	7:0	See description of '17F0h'.	
79h (17F2h)	REG17F2	7:0	Default : 0x00	Access : RO
	DEBUG_BUS_3[7:0]	7:0	DEBUG_BUS_3.	

**QSPI Register (Bank = 17)**

Index (Absolute)	Mnemonic	Bit	Description
79h (17F3h)	REG17F3	7:0	Default : 0x00 Access : RO
	DEBUG_BUS_3[15:8]	7:0	See description of '17F2h'.
7Ah (17F4h)	REG17F4	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	CHIP_SELECT[1:0]	1:0	00: Select external #1 SPI Flash. 01: Select external #2 SPI Flash. 10: Select external #3 SPI Flash. 11: Reserved.
7Bh (17F6h)	REG17F6	7:0	Default : 0x00 Access : RO
	-	7:1	Reserved.
	SWITCH_CS_BUSY	0	1: Switch SPI CS is busy (In this stage, access to SPI Flash is forbidden). 0: Switch SPI CS is done.
7Ch (17F8h)	REG17F8	7:0	Default : 0xFF Access : R/W
	FUNC_SETTING_DEF1[7:0]	7:0	Bit[0]: reserved. Bit[1]: use comb. CSZ setting (setup and high). 0: Disable. 1: Enable. Bit[2]: reserved. Bit[4:3]: Embedded flash size. 00: 64Mb. 01: 128Mb. 10: 16Mb. 11: 32Mb. Bit[15:5]: reserved, keep the data as default value.
7Ch (17F9h)	REG17F9	7:0	Default : 0xFF Access : R/W
	FUNC_SETTING_DEF1[15:8]	7:0	See description of '17F8h'.
7Dh (17FAh)	REG17FA	7:0	Default : 0x00 Access : R/W
	FUNC_SETTING_DEF0[7:0]	7:0	Bit[0]: use index to support 4-byte address. 0: Disable. 1: Enable. Bit[1]: one burst data over two flash enable. 0: Disable. 1: Enable. Bit[2]: 4-byte address mode enable. 0: Disable. 1: Enable. Bit[3]: use user-defined command.



QSPI Register (Bank = 17)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Use default command. 1: Use user-defined command. Bit[4]: use user-defined dummy cycle value at command bypass mode. 0: Use 0xa5. 1: Use user-defined value. Bit[5]: incremental command at flash wrap mode support enable. 0: Disable. 1: Enable. Bit[6]: wrap command at flash non-wrap mode support enable. 0: Disable. 1: Enable. Bit[7]: reserved, keep the data as default value. Bit[8]: SPI IO pin mode after FSP read. 0: Output mode. 1: Input mode. Bit[9]: CS select by address enable. Bit[10]: reserved. Bit[11]: addr_2byte_en. Bit[12]: force_dummy_cyc_en. Bit[13]: addr_over_write_en. Bit[15:12]: reserved, keep the data as default value.	
7Dh (17FBh)	REG17FB	7:0	Default : 0x00	Access : R/W
	FUNC_SETTING_DEF0[15:8]	7:0	See description of '17FAh'.	
7Fh (17FEh)	REG17FE	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	ENDIA	0	For 32-bit CPU read data.	

PWM Register (Bank = 1A)

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1A00h)	REG1A00	7:0	Default : 0x00	Access : R/W
	PWM0_SHIFT[7:0]	7:0	PWM0 rising point shift counter.	
00h	REG1A01	7:0	Default : 0x00	Access : R/W



PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
(1A01h)	PWM0_SHIFT[15:8]	7:0	See description of '1A00h'.	
01h (1A02h)	REG1A02	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM0_SHIFT[17:16]	1:0	See description of '1A00h'.	
02h (1A04h)	REG1A04	7:0	Default : 0x00	Access : R/W
	PWM0_DUTY[7:0]	7:0	PWM0 duty.	
02h (1A05h)	REG1A05	7:0	Default : 0x00	Access : R/W
	PWM0_DUTY[15:8]	7:0	See description of '1A04h'.	
03h (1A06h)	REG1A06	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM0_DUTY[17:16]	1:0	See description of '1A04h'.	
04h (1A08h)	REG1A08	7:0	Default : 0x00	Access : R/W
	PWM0_PERIOD[7:0]	7:0	PWM0 period.	
04h (1A09h)	REG1A09	7:0	Default : 0x00	Access : R/W
	PWM0_PERIOD[15:8]	7:0	See description of '1A08h'.	
05h (1A0Ah)	REG1A0A	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM0_PERIOD[17:16]	1:0	See description of '1A08h'.	
06h (1A0Ch)	REG1A0C	7:0	Default : 0x00	Access : R/W
	PWM0_DIV[7:0]	7:0	PWM0 divider.	
06h (1A0Dh)	REG1A0D	7:0	Default : 0x00	Access : R/W
	PWM0_DIV[15:8]	7:0	See description of '1A0Ch'.	
07h (1A0Eh)	REG1A0E	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	PWM0_POLARITY	4	PWM0 polarity.	
	PWM0_SHIFT_GAT	3	PWM0 enable shift counter gating.	
	PWM0_DIFF_P_EN	2	Enable multiple differential pulse width mode.	
	PWM0_DBEN	1	PWM0 double buffer enable.	
	PWM0_VDBEN_SW	0	PWM0 double buffer enable by software. 1: Enable, 0: Disable.	
08h (1A10h)	REG1A10	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT2[7:0]	7:0	PWM0 rising point shift2 counter.	
08h	REG1A11	7:0	Default : 0xFF	Access : R/W

**PWM Register (Bank = 1A)**

Index (Absolute)	Mnemonic	Bit	Description	
(1A11h)	PWM0_SHIFT2[15:8]	7:0	See description of '1A10h'.	
09h (1A12h)	REG1A12	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY2[7:0]	7:0	PWM0 duty2.	
09h (1A13h)	REG1A13	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY2[15:8]	7:0	See description of '1A12h'.	
0Ah (1A14h)	REG1A14	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT3[7:0]	7:0	PWM0 rising point shift3 counter.	
0Ah (1A15h)	REG1A15	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT3[15:8]	7:0	See description of '1A14h'.	
0Bh (1A16h)	REG1A16	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY3[7:0]	7:0	PWM0 duty3.	
0Bh (1A17h)	REG1A17	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY3[15:8]	7:0	See description of '1A16h'.	
0Ch (1A18h)	REG1A18	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT4[7:0]	7:0	PWM0 rising point shift4 counter.	
0Ch (1A19h)	REG1A19	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT4[15:8]	7:0	See description of '1A18h'.	
0Dh (1A1Ah)	REG1A1A	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY4[7:0]	7:0	PWM0 duty4.	
0Dh (1A1Bh)	REG1A1B	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY4[15:8]	7:0	See description of '1A1Ah'.	
10h (1A20h)	REG1A20	7:0	Default : 0x00	Access : R/W
	GROUP0_ROUND_NUMBER[7:0]	7:0	Round number for group0.	
10h (1A21h)	REG1A21	7:0	Default : 0x00	Access : R/W
	GROUP0_ROUND_NUMBER[15:8]	7:0	See description of '1A20h'.	
11h (1A22h)	REG1A22	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM0_DELAY_COUNT[7:0]	7:0	GROUP0_PWM0_DELAY_COUNT.	
11h (1A23h)	REG1A23	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM0_DELAY_COUNT[15:8]	7:0	See description of '1A22h'.	
12h	REG1A24	7:0	Default : 0x00	Access : R/W

**PWM Register (Bank = 1A)**

Index (Absolute)	Mnemonic	Bit	Description	
(1A24h)	-	7:2	Reserved.	
	GROUP0_PWM0_DELAY_CO UNT[17:16]	1:0	See description of '1A22h'.	
13h (1A26h)	REG1A26	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM1_DELAY_CO UNT[7:0]	7:0	GROUP0_PWM1_DELAY_COUNT.	
13h (1A27h)	REG1A27	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM1_DELAY_CO UNT[15:8]	7:0	See description of '1A26h'.	
14h (1A28h)	REG1A28	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP0_PWM1_DELAY_CO UNT[17:16]	1:0	See description of '1A26h'.	
15h (1A2Ah)	REG1A2A	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM2_DELAY_CO UNT[7:0]	7:0	GROUP0_PWM2_DELAY_COUNT.	
15h (1A2Bh)	REG1A2B	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM2_DELAY_CO UNT[15:8]	7:0	See description of '1A2Ah'.	
16h (1A2Ch)	REG1A2C	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP0_PWM2_DELAY_CO UNT[17:16]	1:0	See description of '1A2Ah'.	
17h (1A2Eh)	REG1A2E	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM3_DELAY_CO UNT[7:0]	7:0	GROUP0_PWM3_DELAY_COUNT.	
17h (1A2Fh)	REG1A2F	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM3_DELAY_CO UNT[15:8]	7:0	See description of '1A2Eh'.	
18h (1A30h)	REG1A30	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP0_PWM3_DELAY_CO UNT[17:16]	1:0	See description of '1A2Eh'.	
20h (1A40h)	REG1A40	7:0	Default : 0x00	Access : R/W
	PWM1_SHIFT[7:0]	7:0	PWM1 rising point shift counter.	



PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
20h (1A41h)	REG1A41	7:0	Default : 0x00	Access : R/W
	PWM1_SHIFT[15:8]	7:0	See description of '1A40h'.	
21h (1A42h)	REG1A42	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM1_SHIFT[17:16]	1:0	See description of '1A40h'.	
22h (1A44h)	REG1A44	7:0	Default : 0x00	Access : R/W
	PWM1_DUTY[7:0]	7:0	PWM1 duty.	
22h (1A45h)	REG1A45	7:0	Default : 0x00	Access : R/W
	PWM1_DUTY[15:8]	7:0	See description of '1A44h'.	
23h (1A46h)	REG1A46	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM1_DUTY[17:16]	1:0	See description of '1A44h'.	
24h (1A48h)	REG1A48	7:0	Default : 0x00	Access : R/W
	PWM1_PERIOD[7:0]	7:0	PWM1 period.	
24h (1A49h)	REG1A49	7:0	Default : 0x00	Access : R/W
	PWM1_PERIOD[15:8]	7:0	See description of '1A48h'.	
25h (1A4Ah)	REG1A4A	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM1_PERIOD[17:16]	1:0	See description of '1A48h'.	
26h (1A4Ch)	REG1A4C	7:0	Default : 0x00	Access : R/W
	PWM1_DIV[7:0]	7:0	PWM1 divider.	
26h (1A4Dh)	REG1A4D	7:0	Default : 0x00	Access : R/W
	PWM1_DIV[15:8]	7:0	See description of '1A4Ch'.	
27h (1A4Eh)	REG1A4E	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	PWM1_POLARITY	4	PWM1 polarity.	
	PWM1_SHIFT_GAT	3	PWM1 enable shift counter gating.	
	PWM1_DIFF_P_EN	2	Enable multiple differential pulse width mode.	
	PWM1_DBEN	1	PWM1 double buffer enable.	
	PWM1_VDBEN_SW	0	PWM1 double buffer enable by software. 1: Enable, 0: Disable.	
28h (1A50h)	REG1A50	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT2[7:0]	7:0	PWM1 rising point shift2 counter.	



PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
28h (1A51h)	REG1A51	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT2[15:8]	7:0	See description of '1A50h'.	
29h (1A52h)	REG1A52	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY2[7:0]	7:0	PWM1 duty2.	
29h (1A53h)	REG1A53	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY2[15:8]	7:0	See description of '1A52h'.	
2Ah (1A54h)	REG1A54	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT3[7:0]	7:0	PWM1 rising point shift3 counter.	
2Ah (1A55h)	REG1A55	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT3[15:8]	7:0	See description of '1A54h'.	
2Bh (1A56h)	REG1A56	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY3[7:0]	7:0	PWM1 duty3.	
2Bh (1A57h)	REG1A57	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY3[15:8]	7:0	See description of '1A56h'.	
2Ch (1A58h)	REG1A58	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT4[7:0]	7:0	PWM1 rising point shift4 counter.	
2Ch (1A59h)	REG1A59	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT4[15:8]	7:0	See description of '1A58h'.	
2Dh (1A5Ah)	REG1A5A	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY4[7:0]	7:0	PWM1 duty4.	
2Dh (1A5Bh)	REG1A5B	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY4[15:8]	7:0	See description of '1A5Ah'.	
30h (1A60h)	REG1A60	7:0	Default : 0x00	Access : R/W
	GROUP1_ROUND_NUMBER[7:0]	7:0	Round number for group1.	
30h (1A61h)	REG1A61	7:0	Default : 0x00	Access : R/W
	GROUP1_ROUND_NUMBER[15:8]	7:0	See description of '1A60h'.	
31h (1A62h)	REG1A62	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM0_DELAY_COUNT[7:0]	7:0	GROUP1_PWM0_DELAY_COUNT.	
31h (1A63h)	REG1A63	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM0_DELAY_COUNT[15:8]	7:0	See description of '1A62h'.	

**PWM Register (Bank = 1A)**

Index (Absolute)	Mnemonic	Bit	Description	
32h (1A64h)	REG1A64	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP1_PWM0_DELAY_CO UNT[17:16]	1:0	See description of '1A62h'.	
33h (1A66h)	REG1A66	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM1_DELAY_CO UNT[7:0]	7:0	GROUP1_PWM1_DELAY_COUNT.	
33h (1A67h)	REG1A67	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM1_DELAY_CO UNT[15:8]	7:0	See description of '1A66h'.	
34h (1A68h)	REG1A68	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP1_PWM1_DELAY_CO UNT[17:16]	1:0	See description of '1A66h'.	
35h (1A6Ah)	REG1A6A	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM2_DELAY_CO UNT[7:0]	7:0	GROUP1_PWM2_DELAY_COUNT.	
35h (1A6Bh)	REG1A6B	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM2_DELAY_CO UNT[15:8]	7:0	See description of '1A6Ah'.	
36h (1A6Ch)	REG1A6C	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP1_PWM2_DELAY_CO UNT[17:16]	1:0	See description of '1A6Ah'.	
37h (1A6Eh)	REG1A6E	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM3_DELAY_CO UNT[7:0]	7:0	GROUP1_PWM3_DELAY_COUNT.	
37h (1A6Fh)	REG1A6F	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM3_DELAY_CO UNT[15:8]	7:0	See description of '1A6Eh'.	
38h (1A70h)	REG1A70	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP1_PWM3_DELAY_CO UNT[17:16]	1:0	See description of '1A6Eh'.	
40h	REG1A80	7:0	Default : 0x00	Access : R/W



PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
(1A80h)	PWM2_SHIFT[7:0]	7:0	PWM2 rising point shift counter.	
40h (1A81h)	REG1A81	7:0	Default : 0x00	Access : R/W
	PWM2_SHIFT[15:8]	7:0	See description of '1A80h'.	
41h (1A82h)	REG1A82	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM2_SHIFT[17:16]	1:0	See description of '1A80h'.	
42h (1A84h)	REG1A84	7:0	Default : 0x00	Access : R/W
	PWM2_DUTY[7:0]	7:0	PWM2 duty.	
42h (1A85h)	REG1A85	7:0	Default : 0x00	Access : R/W
	PWM2_DUTY[15:8]	7:0	See description of '1A84h'.	
43h (1A86h)	REG1A86	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM2_DUTY[17:16]	1:0	See description of '1A84h'.	
44h (1A88h)	REG1A88	7:0	Default : 0x00	Access : R/W
	PWM2_PERIOD[7:0]	7:0	PWM2 period.	
44h (1A89h)	REG1A89	7:0	Default : 0x00	Access : R/W
	PWM2_PERIOD[15:8]	7:0	See description of '1A88h'.	
45h (1A8Ah)	REG1A8A	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM2_PERIOD[17:16]	1:0	See description of '1A88h'.	
46h (1A8Ch)	REG1A8C	7:0	Default : 0x00	Access : R/W
	PWM2_DIV[7:0]	7:0	PWM2 divider.	
46h (1A8Dh)	REG1A8D	7:0	Default : 0x00	Access : R/W
	PWM2_DIV[15:8]	7:0	See description of '1A8Ch'.	
47h (1A8Eh)	REG1A8E	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	PWM2_POLARITY	4	PWM2 polarity.	
	PWM2_SHIFT_GAT	3	PWM2 enable shift counter gating.	
	PWM2_DIFF_P_EN	2	Enable multiple differential pulse width mode.	
	PWM2_DBEN	1	PWM2 double buffer enable.	
	PWM2_VDBEN_SW	0	PWM2 double buffer enable by software. 1: Enable, 0: Disable.	
48h	REG1A90	7:0	Default : 0xFF	Access : R/W

**PWM Register (Bank = 1A)**

Index (Absolute)	Mnemonic	Bit	Description	
(1A90h)	PWM2_SHIFT2[7:0]	7:0	PWM2 rising point shift2 counter.	
48h (1A91h)	REG1A91	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT2[15:8]	7:0	See description of '1A90h'.	
49h (1A92h)	REG1A92	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY2[7:0]	7:0	PWM2 duty2.	
49h (1A93h)	REG1A93	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY2[15:8]	7:0	See description of '1A92h'.	
4Ah (1A94h)	REG1A94	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT3[7:0]	7:0	PWM2 rising point shift3 counter.	
4Ah (1A95h)	REG1A95	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT3[15:8]	7:0	See description of '1A94h'.	
4Bh (1A96h)	REG1A96	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY3[7:0]	7:0	PWM2 duty3.	
4Bh (1A97h)	REG1A97	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY3[15:8]	7:0	See description of '1A96h'.	
4Ch (1A98h)	REG1A98	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT4[7:0]	7:0	PWM2 rising point shift4 counter.	
4Ch (1A99h)	REG1A99	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT4[15:8]	7:0	See description of '1A98h'.	
4Dh (1A9Ah)	REG1A9A	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY4[7:0]	7:0	PWM2 duty4.	
4Dh (1A9Bh)	REG1A9B	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY4[15:8]	7:0	See description of '1A9Ah'.	
50h (1AA0h)	REG1AA0	7:0	Default : 0x00	Access : R/W
	GROUP2_ROUND_NUMBER[7:0]	7:0	Round number for group2.	
50h (1AA1h)	REG1AA1	7:0	Default : 0x00	Access : R/W
	GROUP2_ROUND_NUMBER[15:8]	7:0	See description of '1AA0h'.	
51h (1AA2h)	REG1AA2	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM0_DELAY_COUNT[7:0]	7:0	GROUP2_PWM0_DELAY_COUNT.	
51h (1AA3h)	REG1AA3	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM0_DELAY_CO	7:0	See description of '1AA2h'.	

**PWM Register (Bank = 1A)**

Index (Absolute)	Mnemonic	Bit	Description	
	UNT[15:8]			
52h (1AA4h)	REG1AA4	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP2_PWM0_DELAY_CO UNT[17:16]	1:0	See description of '1AA2h'.	
53h (1AA6h)	REG1AA6	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM1_DELAY_CO UNT[7:0]	7:0	GROUP2_PWM1_DELAY_COUNT.	
53h (1AA7h)	REG1AA7	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM1_DELAY_CO UNT[15:8]	7:0	See description of '1AA6h'.	
54h (1AA8h)	REG1AA8	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP2_PWM1_DELAY_CO UNT[17:16]	1:0	See description of '1AA6h'.	
55h (1AAAh)	REG1AAA	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM2_DELAY_CO UNT[7:0]	7:0	GROUP2_PWM2_DELAY_COUNT.	
55h (1AABh)	REG1AAB	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM2_DELAY_CO UNT[15:8]	7:0	See description of '1AAAa'.	
56h (1AACh)	REG1AAC	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP2_PWM2_DELAY_CO UNT[17:16]	1:0	See description of '1AAAa'.	
60h (1AC0h)	REG1AC0	7:0	Default : 0x00	Access : R/W
	PWM3_SHIFT[7:0]	7:0	PWM3 rising point shift counter.	
60h (1AC1h)	REG1AC1	7:0	Default : 0x00	Access : R/W
	PWM3_SHIFT[15:8]	7:0	See description of '1AC0h'.	
61h (1AC2h)	REG1AC2	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM3_SHIFT[17:16]	1:0	See description of '1AC0h'.	
62h (1AC4h)	REG1AC4	7:0	Default : 0x00	Access : R/W
	PWM3_DUTY[7:0]	7:0	PWM3 duty.	

**PWM Register (Bank = 1A)**

Index (Absolute)	Mnemonic	Bit	Description	
62h (1AC5h)	REG1AC5	7:0	Default : 0x00	Access : R/W
	PWM3_DUTY[15:8]	7:0	See description of '1AC4h'.	
63h (1AC6h)	REG1AC6	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM3_DUTY[17:16]	1:0	See description of '1AC4h'.	
64h (1AC8h)	REG1AC8	7:0	Default : 0x00	Access : R/W
	PWM3_PERIOD[7:0]	7:0	PWM3 period.	
64h (1AC9h)	REG1AC9	7:0	Default : 0x00	Access : R/W
	PWM3_PERIOD[15:8]	7:0	See description of '1AC8h'.	
65h (1ACAh)	REG1ACA	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM3_PERIOD[17:16]	1:0	See description of '1AC8h'.	
66h (1ACCh)	REG1ACC	7:0	Default : 0x00	Access : R/W
	PWM3_DIV[7:0]	7:0	PWM3 divider.	
66h (1ACDh)	REG1ACD	7:0	Default : 0x00	Access : R/W
	PWM3_DIV[15:8]	7:0	See description of '1ACCh'.	
67h (1ACEh)	REG1ACE	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	PWM3_POLARITY	4	PWM3 polarity.	
	PWM3_SHIFT_GAT	3	PWM3 enable shift counter gating.	
	PWM3_DIFF_P_EN	2	Enable multiple differential pulse width mode.	
	PWM3_DBEN	1	PWM3 double buffer enable.	
	PWM3_VDBEN_SW	0	PWM3 double buffer enable by software. 1: Enable, 0: Disable.	
68h (1AD0h)	REG1AD0	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT2[7:0]	7:0	PWM3 rising point shift2 counter.	
68h (1AD1h)	REG1AD1	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT2[15:8]	7:0	See description of '1AD0h'.	
69h (1AD2h)	REG1AD2	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY2[7:0]	7:0	PWM3 duty2.	
69h (1AD3h)	REG1AD3	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY2[15:8]	7:0	See description of '1AD2h'.	
6Ah	REG1AD4	7:0	Default : 0xFF	Access : R/W



PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
(1AD4h)	PWM3_SHIFT3[7:0]	7:0	PWM3 rising point shift3 counter.	
6Ah (1AD5h)	REG1AD5	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT3[15:8]	7:0	See description of '1AD4h'.	
6Bh (1AD6h)	REG1AD6	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY3[7:0]	7:0	PWM3 duty3.	
6Bh (1AD7h)	REG1AD7	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY3[15:8]	7:0	See description of '1AD6h'.	
6Ch (1AD8h)	REG1AD8	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT4[7:0]	7:0	PWM3 rising point shift4 counter.	
6Ch (1AD9h)	REG1AD9	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT4[15:8]	7:0	See description of '1AD8h'.	
6Dh (1ADAh)	REG1ADA	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY4[7:0]	7:0	PWM3 duty4.	
6Dh (1ADBh)	REG1ADB	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY4[15:8]	7:0	See description of '1ADAh'.	
71h (1AE2h)	REG1AE2	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	HOLD_MODE[2:0]	2:0	[0] 1: Group0 hold mode enable. 0: Group0 hold mode disable. [1] 1: Group1 hold mode enable. 0: Group1 hold mode disable. [2] 1: Group2 hold mode enable. 0: Group2 hold mode disable.	
72h (1AE4h)	REG1AE4	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	STOP_MODE[2:0]	2:0	[0] 1: Group0 stop mode enable. 0: Group0 stop mode disable. [1] 1: Group1 stop mode enable. 0: Group1 stop mode disable. [2] 1: Group2 stop mode enable. 0: Group2 stop mode disable.	
73h (1AE6h)	REG1AE6	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PWM_ENABLE[2:0]	2:0	[0] 1: PWM group0 enable, 0: group0 disable. [1] 1: PWM group1 enable, 0: group1 disable.	

**PWM Register (Bank = 1A)**

Index (Absolute)	Mnemonic	Bit	Description	
			[2] 1: PWM group2 enable, 0: group2 disable.	
74h (1AE8h)	REG1AE8	7:0	Default : 0x00	Access : R/W
	SYNC_MODE_EN[7:0]	7:0	[0] 1: PWM0 sync mode enable. [1] 1: PWM1 sync mode enable. ... [10] 1: PWM10 sync mode enable. for PWM10~0.	
74h (1AE9h)	REG1AE9	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SYNC_MODE_EN[10:8]	2:0	See description of '1AE8h'.	
75h (1AEAh)	REG1AEA	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	PWM_INT[1:0]	1:0	[0]: PWM group0 hold int. [1]: PWM group0 round int.	
7Eh (1AFCh)	REG1AFC	7:0	Default : 0x00	Access : RO
	PWM_OUT[7:0]	7:0	PWM output.	
7Eh (1AFDh)	REG1AFD	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	PWM_OUT[10:8]	2:0	See description of '1AFCh'.	
7Fh (1AFEh)	REG1AFE	7:0	Default : 0x00	Access : R/W
	PWM7_SW_RST	7	PWM7 software reset.	
	PWM6_SW_RST	6	PWM6 software reset.	
	PWM5_SW_RST	5	PWM5 software reset.	
	PWM4_SW_RST	4	PWM4 software reset.	
	PWM3_SW_RST	3	PWM3 software reset.	
	PWM2_SW_RST	2	PWM2 software reset.	
	PWM1_SW_RST	1	PWM1 software reset.	
	PWM0_SW_RST	0	PWM0 software reset.	
7Fh (1AFFh)	REG1AFF	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	GROUP2_SW_RST	5	Group2 software reset.	
	GROUP1_SW_RST	4	Group1 software reset.	
	GROUP0_SW_RST	3	Group0 software reset.	
	PWM10_SW_RST	2	PWM10 software reset.	



PWM Register (Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description
	PWM9_SW_RST	1	PWM9 software reset.
	PWM8_SW_RST	0	PWM8 software reset.

TIMER0 Register (Bank = 30)

TIMER0 Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
00h (3000h)	REG3000	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	TIMER_TRIG	1	Set: Enable timer to count one time (from 0 to max, then stop). Clear: By resetting itself or by setting reg_timer_en.	
	TIMER_EN	0	Set: Enable timer counting to be rolled (from 0 to max, then rolled). Clear: By resetting itself or by setting reg_timer_trig.	
00h (3001h)	REG3001	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	TIMER_INT_EN	0	Set: Enable interrupt. Clear: By resetting itself.	
01h (3002h)	REG3002	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	TIMER_HIT	0	Assert: When counter is enabled and matches reg_timer_max. Deassert: By writing 1 or by setting reg_timer_en, reg_timer_once, and reg_timer_max.	
02h (3004h)	REG3004	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
02h (3005h)	REG3005	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[15:8]	7:0	See description of '3004h'.	
03h (3006h)	REG3006	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[23:16]	7:0	See description of '3004h'.	
03h (3007h)	REG3007	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[31:24]	7:0	See description of '3004h'.	
04h	REG3008	7:0	Default : 0x00	Access : RO



TIMER0 Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
(3008h)	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
04h (3009h)	REG3009	7:0	Default : 0x00	Access : RO
	TIMER_CAP[15:8]	7:0	See description of '3008h'.	
05h (300Ah)	REG300A	7:0	Default : 0x00	Access : RO
	TIMER_CAP[23:16]	7:0	See description of '3008h'.	
05h (300Bh)	REG300B	7:0	Default : 0x00	Access : RO
	TIMER_CAP[31:24]	7:0	See description of '3008h'.	
06h (300Ch)	REG300C	7:0	Default : 0x00	Access : R/W
	TIMER_DEVIDE[7:0]	7:0	Timer divide counter number. Default = 12M (216(clk_xiu)/18). 8'b0000: timer counter = clk_xiu/1. 8'b0001: timer counter = clk_xiu/2. 8'b0010: timer counter = clk_xiu/3. ... 8'b1111: timer counter = clk_xiu/16.	

TIMER1 Register (Bank = 30)

TIMER1 Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
00h (3000h)	REG3000	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	TIMER_TRIG	1	Set: Enable timer to count one time (from 0 to max, then stop). Clear: By resetting itself or by setting reg_timer_en.	
	TIMER_EN	0	Set: Enable timer counting to be rolled (from 0 to max, then rolled). Clear: By resetting itself or by setting reg_timer_trig.	
00h (3001h)	REG3001	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	TIMER_INT_EN	0	Set: Enable interrupt. Clear: By resetting itself.	
01h (3002h)	REG3002	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	

**TIMER1 Register (Bank = 30)**

Index (Absolute)	Mnemonic	Bit	Description	
	TIMER_HIT	0	Assert: When counter is enabled and matches reg_timer_max. Deassert: By writing 1 or by setting reg_timer_en, reg_timer_once, and reg_timer_max.	
02h (3004h)	REG3004	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
02h (3005h)	REG3005	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[15:8]	7:0	See description of '3004h'.	
03h (3006h)	REG3006	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[23:16]	7:0	See description of '3004h'.	
03h (3007h)	REG3007	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[31:24]	7:0	See description of '3004h'.	
04h (3008h)	REG3008	7:0	Default : 0x00	Access : RO
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
04h (3009h)	REG3009	7:0	Default : 0x00	Access : RO
	TIMER_CAP[15:8]	7:0	See description of '3008h'.	
05h (300Ah)	REG300A	7:0	Default : 0x00	Access : RO
	TIMER_CAP[23:16]	7:0	See description of '3008h'.	
05h (300Bh)	REG300B	7:0	Default : 0x00	Access : RO
	TIMER_CAP[31:24]	7:0	See description of '3008h'.	
06h (300Ch)	REG300C	7:0	Default : 0x00	Access : R/W
	TIMER_DEVIDE[7:0]	7:0	Timer divide counter number. Default = 12M (216(clk_xiu)/18). 8'b0000: timer counter = clk_xiu/1. 8'b0001: timer counter = clk_xiu/2. 8'b0010: timer counter = clk_xiu/3. ... 8'b1111: timer counter = clk_xiu/16.	



TIMER2 Register (Bank = 30)

TIMER2 Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (3000h)	REG3000	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	TIMER_TRIG	1	Set: Enable timer to count one time (from 0 to max, then stop). Clear: By resetting itself or by setting reg_timer_en.	
	TIMER_EN	0	Set: Enable timer counting to be rolled (from 0 to max, then rolled). Clear: By resetting itself or by setting reg_timer_trig.	
00h (3001h)	REG3001	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	TIMER_INT_EN	0	Set: Enable interrupt. Clear: By resetting itself.	
01h (3002h)	REG3002	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	TIMER_HIT	0	Assert: When counter is enabled and matches reg_timer_max. Deassert: By writing 1 or by setting reg_timer_en, reg_timer_once, and reg_timer_max.	
02h (3004h)	REG3004	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
02h (3005h)	REG3005	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[15:8]	7:0	See description of '3004h'.	
03h (3006h)	REG3006	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[23:16]	7:0	See description of '3004h'.	
03h (3007h)	REG3007	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[31:24]	7:0	See description of '3004h'.	
04h (3008h)	REG3008	7:0	Default : 0x00	Access : RO
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
04h (3009h)	REG3009	7:0	Default : 0x00	Access : RO
	TIMER_CAP[15:8]	7:0	See description of '3008h'.	
05h (300Ah)	REG300A	7:0	Default : 0x00	Access : RO
	TIMER_CAP[23:16]	7:0	See description of '3008h'.	
05h	REG300B	7:0	Default : 0x00	Access : RO



TIMER2 Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
(300Bh)	TIMER_CAP[31:24]	7:0	See description of '3008h'.	
06h (300Ch)	REG300C	7:0	Default : 0x00	Access : R/W
	TIMER_DEVIDE[7:0]	7:0	Timer divide counter number. Default = 12M (216(clk_xiu)/18). 8'b0000: timer counter = clk_xiu/1. 8'b0001: timer counter = clk_xiu/2. 8'b0010: timer counter = clk_xiu/3. ... 8'b1111: timer counter = clk_xiu/16.	

WDT Register (Bank = 30)

WDT Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (3000h)	REG3000	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	WDT_CLR	0	Write '1' to re-start WDT.	
02h (3004h)	REG3004	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	WDT_RST_FLAG	0	Assert: WDT reset has occurred. Write "1" to clear.	
02h (3005h)	REG3005	7:0	Default : 0x09	Access : R/W
	WDT_RST_LEN[7:0]	7:0	Length of WDT reset. 0: One xtal clock. 1: Two xtal clocks 2.....	
03h (3006h)	REG3006	7:0	Default : 0xFF	Access : R/W
	WDT_INT[7:0]	7:0	WDT interrupt period; Interrupt asserts when "WDT counter [31:16]" is equal to WDT_INT and "WDT counter[15:0]" is equal to 0x0000.	
03h (3007h)	REG3007	7:0	Default : 0xFF	Access : R/W
	WDT_INT[15:8]	7:0	See description of '3006h'.	
04h (3008h)	REG3008	7:0	Default : 0xFF	Access : R/W
	WDT_MAX[7:0]	7:0	WDT period maximum value. WDT enable if WDT_MAX is not equal to 0x00000000.	



WDT Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
04h (3009h)	REG3009	7:0	Default : 0xFF	Access : R/W
	WDT_MAX[15:8]	7:0	See description of '3008h'.	
05h (300Ah)	REG300A	7:0	Default : 0xFF	Access : R/W
	WDT_MAX[23:16]	7:0	See description of '3008h'.	
05h (300Bh)	REG300B	7:0	Default : 0xFF	Access : R/W
	WDT_MAX[31:24]	7:0	See description of '3008h'.	

RTCPWC Register (Bank = 34)

RTCPWC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
00h (3400h)	REG3400	7:0	Default : 0x00	Access : R/W
	DIG2RTC_SW0_RD	7	1: Get RTC SW0 value from "rtc2dig_rddata[31:0]" (gating by iso_en).	
	DIG2RTC_SW1_WR	6	1: Use "dig2rtc_wrdata[31:0]" to set SW1 base(gating by iso_en).	
	DIG2RTC_SW0_WR	5	1: Use "dig2rtc_wrdata[31:0]" to set SW0 base(gating by iso_en).	
	DIG2RTC_ALARM_WR	4	1: Use "dig2rtc_wrdata[31:0]" to set Alarm counter(gating by iso_en).	
	DIG2RTC_CNT_RST_WR	3	1: Reset RTC Counter value to 0(gating by iso_en).	
	DIG2RTC_BASE_RD	2	1: Get RTC base value from "rtc2dig_rddata[31:0]"(gating by iso_en).	
	DIG2RTC_BASE_WR	1	1: Use "dig2rtc_wrdata[31:0]" to set RTC Base(gating by iso_en).	
	-	0	Reserved.	
00h (3401h)	REG3401	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DIG2RTC_SW1_RD	0	1: Get RTC SW1 value from "rtc2dig_rddata[31:0]" (gating by iso_en).	
01h (3402h)	REG3402	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DIG2RTC_INT_CLR	3	1: Clear rtc2dig_int (Alarm interrupt)(gating by iso_en).	

**RTCPWC Register (Bank = 34)**

Index (Absolute)	Mnemonic	Bit	Description	
03h (3406h)	DIG2RTC_ALARM_EN	2	1: Set Alarm enable to 1, which also can read from "rtc2dig_alarm_en"(gating by iso_en).	
	DIG2RTC_ALARM_RD	1	1: Get RTC Alarm value from "rtc2dig_rddata[31:0]"(gating by iso_en).	
	DIG2RTC_CNT_RD	0	1: Get RTC counter value from "rtc2dig_rddata[31:0]"(gating by iso_en).	
03h (3406h)	REG3406	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	DIG2RTC_ISO_CTRL[2:0]	2:0	Bit 2-0 ISO_EN control signal. Input "000 -> 001 > 011 -> 111 -> 101 -> 001 -> 000" to enable ISO_EN for 1ms.	
04h (3408h)	REG3408	7:0	Default : 0x00	Access : R/W
	DIG2RTC_WRDATA[7:0]	7:0	DIG2RTC_WRDATA. According to current value of "dig2rtc_base_wr" & "dig2rtc_alarm_wr" & "dig2rtc_sw0_wr" & "dig2rtc_sw1_wr", to write data into corresponding counter.	
04h (3409h)	REG3409	7:0	Default : 0x00	Access : R/W
	DIG2RTC_WRDATA[15:8]	7:0	See description of '3408h'.	
05h (340Ah)	REG340A	7:0	Default : 0x00	Access : R/W
	DIG2RTC_WRDATA[23:16]	7:0	See description of '3408h'.	
05h (340Bh)	REG340B	7:0	Default : 0x00	Access : R/W
	DIG2RTC_WRDATA[31:24]	7:0	See description of '3408h'.	
06h (340Ch)	REG340C	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DIG2RTC_SET	0	1: Set "rtc2dig_valid" to 1, which is direct bypass to Analog part.	
07h (340Eh)	REG340E	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	RTC2DIG_VALID	0	Get value from "dig2rtc_set", bypass from Analog Part.	
08h (3410h)	REG3410	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	RTC2DIG_ISO_CTRL_ACK	3	ISO control ack signal. SW can read this bit to indicate the ISO control is correct or not. "000(S0) -> 001 (S1) > 011 (S2) -> 111 (S3) -> 101 (S4)	

**RTCPWC Register (Bank = 34)**

Index (Absolute)	Mnemonic	Bit	Description	
09h (3412h)			-> 001 (S5) -> 000 (S0)" Ack signal will be 1, when under S1/S3/S5 state.	
	-	2	Reserved.	
	RTC2DIG_INT	1	Alarm interrupt , which can be clear by "dig2rtc_int_clr"	
	RTC2DIG_ALARM_EN	0	Get value from "dig2rtc_alarm_en", read for debug usage. 1: Means the Alarm function is enable.	
09h (3412h)	REG3412	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA[7:0]	7:0	RTC read data. According the current value of "dig2rtc_base_rd", "dig2rtc_alarm_rd", "dig2rtc_sw0_rd", "dig2rtc_sw1_rd" to decide the read data type.	
09h (3413h)	REG3413	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA[15:8]	7:0	See description of '3412h'.	
0Ah (3414h)	REG3414	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA[23:16]	7:0	See description of '3412h'.	
0Ah (3415h)	REG3415	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA[31:24]	7:0	See description of '3412h'.	
0Bh (3416h)	REG3416	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	RTC2DIG_CNT_UPDATING	0	RTC counter updating period (1Hz clock edge) indication. 0: RTC counter value is ready to read. 1: RTC counter is under updating (1ms width enclosing 1Hz clock edge), when SW get 1 in this bit, please read the counter value again to get valid data.	
0Ch (3418h)	REG3418	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA_CNT[7:0]	7:0	RTC read data for time counter(latch rtc2dig_rddata). According the current value of "dig2rtc_cnt_rd" to decide the read data type.	
0Ch (3419h)	REG3419	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA_CNT[15: 8]	7:0	See description of '3418h'.	
0Dh (341Ah)	REG341A	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA_CNT[23: 16]	7:0	See description of '3418h'.	
0Dh (341Bh)	REG341B	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA_CNT[31: 32]	7:0	See description of '3418h'.	



RTCPWC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
	24]			
0Eh (341Ch)	REG341C	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	DIG2RTC_CNT_RD_TRIG	0	Rtc2dig_rddata_cnt and cnt_updating trigger signal. 0: RTC counter and cnt_updating would't update. 1: Generate a pluse to latch data before read ,including signal rtc2dig_rddata[31:0] and rtc2dig_cnt updating.	
0Fh (341Eh)	REG341E	7:0	Default : 0x05	Access : R/W
	-	7:3	Reserved.	
	DIG2PWC_EMGCY_OFF_EN	2	Set 1 to Enable PWC Power-Key 1 emergency shut-down (gating by iso_en).	
	DIG2PWC_ALARM_ON_EN	1	Set 1 to Enable RTC alarm to power-on system via PWC function (gating by iso_en).	
	DIG2PWC_PWR_EN_CTRL	0	Software control of PWC Power Enable; Set to 0 and initiate an isolation control cycle to start Power-Off sequence(gating by iso_en).	
10h (3420h)	REG3420	7:0	Default : 0xFF	Access : R/W
	DIG2PWC_OPT_7_0[7:0]	7:0	Software control of PWC Powerkey 0-7(gating by iso_en). 1: Enable function. 0: Disable function.	
10h (3421h)	REG3421	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SEL_32K_CLEAN_JITTER	2	Register for poc_atop/rtc_xtal.	
	SEL_32K_COMP_DRV	1	Register for poc_atop/rtc_xtal.	
	PMTEST_INT	0	Replace PAD_PMTEST, when PAD_PMTEST not bound.	
11h (3422h)	REG3422	7:0	Default : 0x00	Access : RO
	PWC2DIG_FLAG_7_0[7:0]	7:0	PWC power-on flag. User can check the status to know which key/event trigger power-on. [2:0]. 3'b000: power-key 1 power-on. 3'b001: power-key 2 power-on. 3'b010: power-key 3 power-on. 3'b011: power-key 4 power-on. 3'b100: power-key 5 power-on. 3'b101: Alarm power-on.	

**RTCPWC Register (Bank = 34)**

Index (Absolute)	Mnemonic	Bit	Description	
12h (3424h)	REG3424	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	PWC2DIG_PWRKEY_5	5	Power key-5 status.	
	PWC2DIG_PWRKEY_4	4	Power key-4 status.	
	PWC2DIG_PWRKEY_3	3	Power key-3 status.	
	PWC2DIG_PWRKEY_2	2	Power key-2 status.	
	PWC2DIG_PWRKEY_1	1	Power key-1 status.	
	PWC2DIG_PWR_GOOD	0	Power good status.	
13h (3426h)	REG3426	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	PWC2DIG_RESET_N	2	PWR reset status.	
	32K_OK	1	Flag XTAL 32k OK.	
	PWC2DIG_PWR_EN_STATE	0	Power enable status.	
14h (3428h)	REG3428	7:0	Default : 0x00	Access : RO
	POC_TESTBUS[7:0]	7:0	[0]: Pwr_on_st. [1]: Pwr_off_trig. [2]: Pwr_on_fail. [3]: Pwr_on_done. [4]: Pwc_off_cs. [5]: Pwc_on_seq_cs. [6]: Pwc_on_cs. [7]: Pwr_en. [8]: Gr_RST. [9]: Hw_RST_reboot. [10]: Pwrkey1_deb. [11]: Pwrkey2_deb. [12]: 1'b0. [13]: Pwrkey4_deb. [14]: Pwrkey5_deb. [15]: 1'b0.	
14h (3429h)	REG3429	7:0	Default : 0x00	Access : RO
	POC_TESTBUS[15:8]	7:0	See description of '3428h'.	
15h (342Ah)	REG342A	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	RTC_TESTBUS[5:0]	5:0	[0]: ISO_EN. [1]: Clk_1hz_p.	

**RTCPWC Register (Bank = 34)**

Index (Absolute)	Mnemonic	Bit	Description
			[2]: Clk_1hz. [3]: Clk_8hz. [4]: Clk_128hz. [5]: Clk_1khz.



NONPM CH4 REGISTER TABLE

CHIPTOP Register (Bank = 101E)

CHIPTOP Register (Bank = 101E)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (101E00h)	REG101E00	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	CKG_ALLDFT	0	MIU clock selects DFT clock. MPLL_SYN clock selects DFT clock. MIU_REC clock selects DFT clock. GE clock selects DFT clock.	
01h (101E03h)	REG101E03	7:0	Default : 0x02	Access : R/W
	-	7:6	Reserved.	
	SETL	5	Digital pads set low.	
	SETH	4	Digital pads set high.	
	-	3:2	Reserved.	
	FT_MODE	1	FT mode. 1: Enable FT mode. 0: Disable FT mode.	
	-	0	Reserved.	
03h (101E06h)	REG101E06	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	UART0_MODE[2:0]	6:4	UART0 Mode.	
	-	3	Reserved.	
	FUART_MODE[2:0]	2:0	FUART Mode.	
03h (101E07h)	REG101E07	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	UART2_MODE[2:0]	6:4	UART2 Mode.	
	-	3	Reserved.	
	UART1_MODE[2:0]	2:0	UART1 Mode.	
07h (101E0Eh)	REG101E0E	7:0	Default : 0x00	Access : R/W
	PWM2_MODE[1:0]	7:6	PWM2 Mode.	
	PWM1_MODE[2:0]	5: 3	PWM1 Mode.	
	PWM0_MODE[2:0]	2:0	PWM0 Mode.	
07h (101E0Fh)	REG101EOF	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	

**CHIPTOP Register (Bank = 101E)**

Index (Absolute)	Mnemonic	Bit	Description	
	PWM3_MODE[2:0]	3:1	PWM3 Mode.	
	PWM2_MODE[2]	0	See description of '101E0Eh'.	
08h (101E11h)	REG101E11	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SDIO_MODE[1:0]	1:0	SDIO Mode.	
09h (101E12h)	REG101E12	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	I2C1_MODE[2:0]	6:4	I2C1 Mode.	
	-	3	Reserved.	
	I2C0_MODE[2:0]	2:0	I2C0 Mode.	
0Ah (101E14h)	REG101E14	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PM_SPICZ2_MODE[1:0]	5:4	PM SPI CZ2 Mode.	
	-	3:1	Reserved.	
	IDAC_MODE	0	IDAC Mode.	
0Bh (101E16h)	REG101E16	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SATA_LED_MODE	0	SATA LED Mode.	
0Ch (101E18h)	REG101E18	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPI0_MODE[2:0]	2:0	SPI0 Mode.	
0Dh (101E1Ah)	REG101E1A	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	BT1120_MODE[1:0]	1:0	BT1120 Mode.	
0Dh (101E1Bh)	REG101E1B	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	TX_MIPI_MODE[1:0]	5:4	MIPI TX mode.	
	TTL_MODE[3:0]	3:0	TTL Mode.	
0Eh (101E1Ch)	REG101E1C	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	ETH0_MODE	0	ETH0 Mode.	
0Eh (101E1Dh)	REG101E1D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	



CHIPTOP Register (Bank = 101E)				
Index (Absolute)	Mnemonic	Bit	Description	
	ETH1_MODE[3:0]	3:0	ETH1 Mode.	
0Fh (101E1Eh)	REG101E1E	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	EJ_MODE[1:0]	1:0	EJ Mode.	
0Fh (101E1Fh)	REG101E1F	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	I2S_MODE[1:0]	5:4	I2S Mode.	
	-	3	Reserved.	
	DMIC_MODE[2:0]	2:0	DMIC Mode.	
12h (101E24h)	REG101E24	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	TEST_OUT_MODE[1:0]	5:4	Select TEST_OUT mode. 2'd0: TEST_OUT functions are not enabled. 2'd1: TEST_OUT[23:0] use FUART/SR/SPI0 pads. 2'd2: TEST_OUT[23:0] use I2C0/SD/USB/SAR/PM/ETH pads. 2'd3: TEST_OUT[15:0] use SR pads.	
	-	3:2	Reserved.	
	TEST_IN_MODE[1:0]	1:0	Select TEST IN mode. 2'd0: TEST_IN functions are not enabled. 2'd1: TEST_IN[23:0] use FUART/SR/SPI0 pads. 2'd2: TEST_IN[23:0] use I2C0/SD/USB/SAR/PM/ETH pads. 2'd3: TEST_IN[14:0] use SAR/ETH/FUART/SPI0/SD/USB pads.	
	REG101E39	7:0	Default : 0x00	Access : R/W
	BIST_MODE_EXT	7	BIST mode enable (disabled by default).	
	BIST_START_EXT	6	BIST mode start.	
1Ch (101E39h)	-	5	Reserved.	
	FORCE_ALLSRAM_ON	4	Force all of the whole chip SRAM to power-on.	
	-	3:0	Reserved.	
	REG101E3A	7:0	Default : 0x00	Access : RO
1Dh (101E3Ah)	BIST_DONE[7:0]	7:0	Indicate SRAM done. [0]: Dig_gp. [1]: Pm_gp. [2]: Sc_gp.	

**CHIPTOP Register (Bank = 101E)**

Index (Absolute)	Mnemonic	Bit	Description	
			[3]: Dec_gp. [4]~[14]: N/A. [15]: All.	
1Dh (101E3Bh)	REG101E3B	7:0	Default : 0x00	Access : RO
	BIST_DONE[15:8]	7:0	See description of '101E3Ah'.	
1Eh (101E3Ch)	REG101E3C	7:0	Default : 0x00	Access : RO
	BIST_FAIL[7:0]	7:0	Indicate SRAM fail. [0]: Dig_gp. [1]: Pm_gp. [2]: Sc_gp. [3]: Dec_gp. [4]~[14]: N/A. [15]: All.	
1Eh (101E3Dh)	REG101E3D	7:0	Default : 0x00	Access : RO
	BIST_FAIL[15:8]	7:0	See description of '101E3Ch'.	
20h (101E40h)	REG101E40	7:0	Default : 0xFF	Access : R/W
	CHIPTOP_DUMMY_0[7:0]	7:0	Dummy registers for CHIPTOP.	
20h (101E41h)	REG101E41	7:0	Default : 0xFF	Access : R/W
	CHIPTOP_DUMMY_0[15:8]	7:0	See description of '101E40h'.	
21h (101E42h)	REG101E42	7:0	Default : 0x00	Access : R/W
	CHIPTOP_DUMMY_1[7:0]	7:0	Dummy registers for CHIPTOP. [0]: Clk_MIU_xd2MIU ICG control. 0: Disable. 1: Enable.	
21h (101E43h)	REG101E43	7:0	Default : 0x00	Access : R/W
	CHIPTOP_DUMMY_1[15:8]	7:0	See description of '101E42h'.	
22h (101E44h)	REG101E44	7:0	Default : 0xFF	Access : R/W
	CHIPTOP_DUMMY_2[7:0]	7:0	Dummy registers for CHIPTOP.	
22h (101E45h)	REG101E45	7:0	Default : 0xFF	Access : R/W
	CHIPTOP_DUMMY_2[15:8]	7:0	See description of '101E44h'.	
23h (101E46h)	REG101E46	7:0	Default : 0x00	Access : R/W
	CHIPTOP_DUMMY_3[7:0]	7:0	Dummy registers for CHIPTOP.	
23h (101E47h)	REG101E47	7:0	Default : 0x00	Access : R/W
	CHIPTOP_DUMMY_3[15:8]	7:0	See description of '101E46h'.	
30h	REG101E60	7:0	Default : 0x00	Access : R/W

**CHIPTOP Register (Bank = 101E)**

Index (Absolute)	Mnemonic	Bit	Description	
(101E60h)	GPIO_DRV[7:0]	7:0	GPIO pad control.	
30h (101E61h)	REG101E61	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	GPIO_DRV[14: 8]	6:0	See description of '101E60h'.	
31h (101E62h)	REG101E62	7:0	Default : 0xFF	Access : R/W
31h (101E63h)	GPIO_PE[7:0]	7:0	GPIO pad control.	
31h (101E63h)	REG101E63	7:0	Default : 0x7F	Access : R/W
	-	7	Reserved.	
	GPIO_PE[14: 8]	6:0	See description of '101E62h'.	
32h (101E64h)	REG101E64	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SD_DRV[6:0]	6:0	SD pad control.	
32h (101E65h)	REG101E65	7:0	Default : 0x7F	Access : R/W
	-	7	Reserved.	
	SD_PE[6:0]	6:0	SD pad control.	
35h (101E6Ah)	REG101E6A	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	UART0_DRV[1:0]	5:4	UART0 pad control.	
	FUART_DRV[3:0]	3:0	FUART pad control.	
35h (101E6Bh)	REG101E6B	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	UART1_DRV[1:0]	1:0	UART1 pad control.	
36h (101E6Ch)	REG101E6C	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	HDMITX_DRV[1:0]	1:0	HDMI pad control.	
37h (101E6Eh)	REG101E6E	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SATA_GPIO_DRV	0	SATA GPIO pad control.	
38h (101E70h)	REG101E70	7:0	Default : 0xFF	Access : R/W
	TTL_IE[7:0]	7:0	TTL pad control.	
38h (101E71h)	REG101E71	7:0	Default : 0xFF	Access : R/W
	TTL_IE[15:8]	7:0	See description of '101E70h'.	
39h	REG101E72	7:0	Default : 0xFF	Access : R/W



CHIPTOP Register (Bank = 101E)				
Index (Absolute)	Mnemonic	Bit	Description	
(101E72h)	TTL_IE[23:16]	7:0	See description of '101E70h'.	
39h (101E73h)	REG101E73	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TTL_IE[27:24]	3:0	See description of '101E70h'.	
3Ah	REG101E74	7:0	Default : 0xFF	Access : R/W
(101E74h)	TTL_PE[7:0]	7:0	TTL pad control.	
3Ah (101E75h)	REG101E75	7:0	Default : 0xFF	Access : R/W
	TTL_PE[15:8]	7:0	See description of '101E74h'.	
3Bh (101E76h)	REG101E76	7:0	Default : 0xFF	Access : R/W
	TTL_PE[23:16]	7:0	See description of '101E74h'.	
	REG101E77	7:0	Default : 0x0F	Access : R/W
(101E77h)	-	7:4	Reserved.	
	TTL_PE[27:24]	3:0	See description of '101E74h'.	
	REG101E78	7:0	Default : 0xFF	Access : R/W
(101E78h)	TTL_PS[7:0]	7:0	TTL pad control.	
3Ch (101E79h)	REG101E79	7:0	Default : 0xFF	Access : R/W
	TTL_PS[15:8]	7:0	See description of '101E78h'.	
3Dh (101E7Ah)	REG101E7A	7:0	Default : 0xFF	Access : R/W
	TTL_PS[23:16]	7:0	See description of '101E78h'.	
3Dh (101E7Bh)	REG101E7B	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TTL_PS[27:24]	3:0	See description of '101E78h'.	
3Eh (101E7Ch)	REG101E7C	7:0	Default : 0x00	Access : R/W
	TTL_DRV[7:0]	7:0	TTL pad control.	
3Eh (101E7Dh)	REG101E7D	7:0	Default : 0x00	Access : R/W
	TTL_DRV[15:8]	7:0	See description of '101E7Ch'.	
3Fh (101E7Eh)	REG101E7E	7:0	Default : 0x00	Access : R/W
	TTL_DRV[23:16]	7:0	See description of '101E7Ch'.	
3Fh (101E7Fh)	REG101E7F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TTL_DRV[27:24]	3:0	See description of '101E7Ch'.	
40h (101E80h)	REG101E80	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	

**CHIPTOP Register (Bank = 101E)**

Index (Absolute)	Mnemonic	Bit	Description	
	MCU_BRIDGE_EN_MODE[1:0]	1:0	Clock MCU gating control. 00: Use MCU_bridge_en (HW saving mode 0). 01: Use MCU_bridge_en_d (HW saving mode 1, preferred). 10: SW saving power mode. 11: Always enable (default).	
44h (101E88h)	REG101E88	7:0	Default : 0xFF	Access : R/W
	RIU_WCLK_MASK[7:0]	7:0	RIU write clock mask. [0]: Sc_gp. [1]: Vhe_gp. [2]: HeMCU_gp. [3]: Mipi_gp. [4]: Mcu_if_gp. [5]: Others.	
44h (101E89h)	REG101E89	7:0	Default : 0xFF	Access : R/W
	RIU_WCLK_MASK[15:8]	7:0	See description of '101E88h'.	
45h (101E8Ah)	REG101E8A	7:0	Default : 0xFF	Access : R/W
	RESERVED3[7:0]	7:0	Reserved.	
45h (101E8Bh)	REG101E8B	7:0	Default : 0xFF	Access : R/W
	RESERVED3[15:8]	7:0	See description of '101E8Ah'.	
46h (101E8Ch)	REG101E8C	7:0	Default : 0xFF	Access : R/W
	RESERVED4[7:0]	7:0	Reserved.	
46h (101E8Dh)	REG101E8D	7:0	Default : 0xFF	Access : R/W
	RESERVED4[15:8]	7:0	See description of '101E8Ch'.	
47h (101E8Eh)	REG101E8E	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	BOND_OV_EN[4:0]	4:0	Bonding overwrite enable.	
47h (101E8Fh)	REG101E8F	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	BOND_OV[4:0]	4:0	Bonding overwrite value.	
48h (101E90h)	REG101E90	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	BOND_IN[4:0]	4:0	Bonding value.	
50h (101EA1h)	REG101EA1	7:0	Default : 0x80	Access : R/W
	ALLPAD_IN	7	1: Set all pads (except PM) as input.	

**CHIPTOP Register (Bank = 101E)**

Index (Absolute)	Mnemonic	Bit	Description	
	-	6:0	Reserved.	
53h (101EA6h)	REG101EA6	7:0	Default : 0x10	Access : R/W
	UART_SEL1[3:0]	7:4	Select controller for PAD_FUART_RX and PAD_FUART_TX.	
	UART_SEL0[3:0]	3:0	Select controller for PAD_PM_UART_RX and PAD_PM_UART_TX. 0000: N/A. 0001: FUART. 0010: UART0. 0011: UART1. 0100: UART2. 0101: UART_DEC. Note: For PAD_PM_UART_RX and PAD_PM_UART_TX, please refer to the "reg_hk51_uart0_en" and "reg_uart_rx_enable" in pm_sleep registers. (a). "reg_hk51_uart0_en" == 0. (b). "reg_uart_rx_enable" == 1.	
53h (101EA7h)	REG101EA7	7:0	Default : 0x32	Access : R/W
	UART_SEL3[3:0]	7:4	Select controller for PAD_UART1_RX and PAD_UART1_TX.	
	UART_SEL2[3:0]	3:0	Select controller for PAD_UART0_RX and PAD_UART0_TX.	
54h (101EA8h)	REG101EA8	7:0	Default : 0x54	Access : R/W
	UART_SEL5[3:0]	7:4	Select controller for PAD_PM_LCD1/LCD0.	
	UART_SEL4[3:0]	3:0	Select controller for PAD_UART2_RX and PAD_UART2_TX.	
55h (101EAAh)	REG101EAA	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	JTAG_SEL[3:0]	3:0	JTAG selection.	
55h (101EABh)	REG101EAB	7:0	Default : 0x00	Access : R/W
	UART_PAD_INVERSE[7:0]	7:0	Invert PAD UART TX/RX.	
56h (101EACH)	REG101EAC	7:0	Default : 0x00	Access : R/W
	UART_INNER_LOOPBACK[7:0]	7:0	Enable of inner loopback test for 3 sets of UART controller. [0]: N/A. [1]: FUART enable. [2]: UART0 enable. [3]: UART1 enable. [4]~[7]: N/A.	
56h	REG101EAD	7:0	Default : 0x00	Access : R/W

**CHIPTOP Register (Bank = 101E)**

Index (Absolute)	Mnemonic	Bit	Description	
(101EADh)	UART_OUTER_LOOPBACK[7:0]	7:0	Enable of outer loopback test for 4 sets of UART pad. [0]: PM_UART enable. [1]: FUART enable. [2]: UART0 enable. [3]: UART1 enable. [4]~[7]: N/A.	
57h (101EAEh)	REG101EAE	7:0	Default : 0x00	Access : R/W
	FORCE_RX_DISABLE[7:0]	7:0	Disable RX signals from PADs.	
57h (101EAFh)	REG101EAF	7:0	Default : 0x00	Access : R/W
	FORCE_RX_DISABLE[15:8]	7:0	See description of '101EAEh'.	
58h (101EB0h)	REG101EB0	7:0	Default : 0x00	Access : R/W
	FPGA_MIU_OPTION[7:0]	7:0	FPGA_MIU_OPTION.	
58h (101EB1h)	REG101EB1	7:0	Default : 0x00	Access : R/W
	FPGA_MIU_OPTION[15:8]	7:0	See description of '101EB0h'.	
65h (101ECAh)	REG101ECA	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	CHIP_CONFIG_STAT[4:0]	4:0	CHIP_CONFIG status.	
65h (101ECBh)	REG101ECB	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	POWERGOOD_AVDD	4	POWERGOOD_AVDD status.	
	-	3:2	Reserved.	
	IN_SEL_DBUS	1	IN_SEL_DBUS.	
	IN_SEL_SBUS	0	IN_SEL_SBUS.	
69h (101ED3h)	REG101ED3	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	BOOT_FROM_SDRAM	3	Boot from SDRAM. 1: Enable boot from SDRAM. 0: Disable boot from SDRAM.	
	-	2:0	Reserved.	
6Ah (101ED4h)	REG101ED4	7:0	Default : 0x00	Access : R/W
	BOOT_FROM_SDRAM_OFFSET[7:0]	7:0	The booting address of SDRAM.	
6Ah (101ED5h)	REG101ED5	7:0	Default : 0x00	Access : R/W
	BOOT_FROM_SDRAM_OFFSET[15:8]	7:0	See description of '101ED4h'.	



CHIPTOP Register (Bank = 101E)				
Index (Absolute)	Mnemonic	Bit	Description	
6Bh (101ED6h)	REG101ED6	7:0	Default : 0x00	Access : R/W
	BOOT_FROM_SDRAM_OFFSET[23:16]	7:0	See description of '101ED4h'.	
6Bh (101ED7h)	REG101ED7	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	BOOT_FROM_SDRAM_OFFSET[25:24]	1:0	See description of '101ED4h'.	
70h (101EE1h)	REG101EE1	7:0	Default : 0x00	Access : R/W
	CLK_CALC_EN	7	CLK_CALC_EN. 1: Enable. 0: Disable.	
	-	6: 3	Reserved.	
	ROSC_OUT_SEL[2:0]	2:0	Ring OSC output select. 000: Select delay chain 0. 001: Select delay chain 1. 010: Select delay chain 2. 011: Select delay chain 3. 100: Select delay chain 4. 101: Select delay chain 5. 110: Select delay chain 6. 111: Select delay chain 7.	
	REG101EE2	7:0	Default : 0x00	Access : RO
71h (101EE2h)	CALC_CNT_REPORT[7:0]	7:0	CALC_CNT_REPORT.	
	REG101EE3	7:0	Default : 0x00	Access : RO
71h (101EE3h)	CALC_CNT_REPORT[15:8]	7:0	See description of '101EE2h'.	
	REG101EE6	7:0	Default : 0xFF	Access : R/W
73h (101EE6h)	RESERVED[7:0]	7:0	Reserved.	
	REG101EE7	7:0	Default : 0xFF	Access : R/W
73h (101EE7h)	RESERVED[15:8]	7:0	See description of '101EE6h'.	
	REG101EE8	7:0	Default : 0x00	Access : R/W
74h (101EE8h)	RESERVED[23:16]	7:0	See description of '101EE6h'.	
	REG101EE9	7:0	Default : 0x00	Access : R/W
74h (101EE9h)	RESERVED[31:24]	7:0	See description of '101EE6h'.	
	REG101EEA	7:0	Default : 0x00	Access : R/W
75h (101EEAh)	TEST_RB	7	Setting for the data arrangement on test bus.	



CHIPTOP Register (Bank = 101E)			
Index (Absolute)	Mnemonic	Bit	Description
	TEST_GB	6	Setting for the data arrangement on test bus.
	TEST_RG	5	Setting for the data arrangement on test bus.
	-	4	Reserved.
	SWAPTEST12BIT	3	Swap MSB 12 bits with LSB 12 bits of test bus.
	CLK_OUT_SEL[2:0]	2:0	Select TEST_CLK_OUT source. 3'd0: TEST_CLK_OUT = TEST_BUS_GB[0]. 3'd1: TEST_CLK_OUT = TEST_BUS_GB[1]. 3'd2: TEST_CLK_OUT = TEST_BUS_GB[2]. 3'd3: TEST_CLK_OUT = TEST_BUS_GB[3]. 3'd4: TEST_CLK_OUT = TEST_BUS_GB[4]. 3'd5: TEST_CLK_OUT = TEST_BUS_GB[5]. 3'd6: TEST_CLK_OUT = TEST_BUS_GB[6]. 3'd7: TEST_CLK_OUT = TEST_BUS_GB[7].
75h (101EEBh)	REG101EEB	7:0	Default : 0x00 Access : R/W
	ROSC_IN_SEL	7	Select the input source of ring oscillator in CHIP_CONF. 1: Close-loop (enable ring oscillator). 0: Open-loop (input from external digital input).
	TESTBUS_EN	6	Enable test bus output (disabled by default).
	TESTCLK_MODE	5	TESTCLK_MODE used in TEST_CTRL.
	-	4: 2	Reserved.
	SEL_CLK_TEST_OUT[1:0]	1:0	Select CLK_TEST_OUT. 2'd0: Select CLK_TEST_OUT[47:0]. 2'd1: Select CLK_TEST_OUT[95:48]. 2'd2: Select CLK_TEST_OUT[143:96]. 2'd3: Reserved.
76h (101EECh)	REG101EEC	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SINGLE_CLK_OUT_SEL[2:0]	2:0	Select single CLK_OUT. 3'd1: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT. 3'd2: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d4. 3'd3: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d8. 3'd4: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d16. 3'd5: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d32.



CHIPTOP Register (Bank = 101E)

Index (Absolute)	Mnemonic	Bit	Description	
			3'd6: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d64. Others: No TEST_CLK_OUT.	
77h (101EEEh)	REG101EEE	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	TEST_BUS24B_SEL[5:0]	5:0	Select TEST_BUS[23:0] source. 6'd2: TEST_BUS = ANA_MISC_TEST_OUT. 6'd3: TEST_BUS = MIU_TEST_OUT. 6'd4: TEST_BUS = DIAMOND_TOP_WP_TEST_OUT. 6'd6: TEST_BUS = UTMI_P1_TEST_OUT. 6'd7: TEST_BUS = UTMI_P2_TEST_OUT. 6'd8: TEST_BUS = AUSDM_TEST_OUT. 6'd9: TEST_BUS = DIG_PM_TEST_OUT. 6'd10: TEST_BUS = MCU_IF_TEST_OUT. 6'd11: TEST_BUS = UTMI_P3_TEST_OUT. 6'd16: TEST_BUS = SC_GP_TEST_OUT. 6'd17: TEST_BUS = DEC_GP_TEST_OUT. 6'd25: TEST_BUS = CLKGEN_TEST_OUT. 6'd26: TEST_BUS = CLKGEN_TEST_OUT2. Others: No TEST_OUT.	
7Bh (101EF6h)	REG101EF6	7:0	Default : 0x00	Access : R/W
	CHIPTOP_RESERVED[7:0]	7:0		
7Bh (101EF7h)	REG101EF7	7:0	Default : 0x00	Access : R/W
	CHIPTOP_RESERVED[15:8]	7:0	See description of '101EF6h'.	
7Ch (101EF8h)	REG101EF8	7:0	Default : 0xFF	Access : R/W
	CHK_CLK_HEMCU_FREQ_C MP_DATA[7:0]	7:0		
7Ch (101EF9h)	REG101EF9	7:0	Default : 0xFF	Access : R/W
	CHK_CLK_HEMCU_FREQ_C MP_DATA[15:8]	7:0	See description of '101EF8h'.	
7Dh (101EFAh)	REG101EFA	7:0	Default : 0x03	Access : R/W
	-	7:4	Reserved.	
	256BUS_2X_DIV_EN[3:0]	3:0	256bus MIU 2x div enable.	
7Eh (101EFCh)	REG101EFC	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	MIU2X_DIV_RSTZ[3:0]	3:0	Clk_MIU2x_div sw rstz. [0]: MIU0.	



CHIPTOP Register (Bank = 101E)

Index (Absolute)	Mnemonic	Bit	Description
			[3:1]: Reserved.

PADTOP Register (Bank = 103C)

PADTOP Register (Bank = 103C)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (103C00h)	REG103C00	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_0	5		
	GPIO_OUT_0	4		
	-	3:1	Reserved.	
	GPIO_IN_0	0		
01h (103C02h)	REG103C02	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_1	5		
	GPIO_OUT_1	4		
	-	3:1	Reserved.	
	GPIO_IN_1	0		
02h (103C04h)	REG103C04	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_2	5		
	GPIO_OUT_2	4		
	-	3:1	Reserved.	
	GPIO_IN_2	0		
03h (103C06h)	REG103C06	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_3	5		
	GPIO_OUT_3	4		
	-	3:1	Reserved.	
	GPIO_IN_3	0		
04h (103C08h)	REG103C08	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	



PADTOP Register (Bank = 103C)				
Index (Absolute)	Mnemonic	Bit	Description	
05h (103C0Ah)	GPIO_OEN_4	5		
	GPIO_OUT_4	4		
	-	3:1	Reserved.	
	GPIO_IN_4	0		
06h (103C0Ch)	REG103C0A	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_5	5		
	GPIO_OUT_5	4		
	-	3:1	Reserved.	
	GPIO_IN_5	0		
07h (103C0Eh)	REG103C0C	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_6	5		
	GPIO_OUT_6	4		
	-	3:1	Reserved.	
	GPIO_IN_6	0		
08h (103C10h)	REG103C0E	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_7	5		
	GPIO_OUT_7	4		
	-	3:1	Reserved.	
	GPIO_IN_7	0		
09h (103C12h)	REG103C10	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_8	5		
	GPIO_OUT_8	4		
	-	3:1	Reserved.	
	GPIO_IN_8	0		
0Ah (103C14h)	REG103C12	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_9	5		
	GPIO_OUT_9	4		
	-	3:1	Reserved.	



PADTOP Register (Bank = 103C)				
Index (Absolute)	Mnemonic	Bit	Description	
0Ah (103C14h)	GPIO_IN_9	0		
	REG103C14	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_10	5		
	GPIO_OUT_10	4		
	-	3:1	Reserved.	
	GPIO_IN_10	0		
0Bh (103C16h)	REG103C16	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_11	5		
	GPIO_OUT_11	4		
	-	3:1	Reserved.	
	GPIO_IN_11	0		
0Ch (103C18h)	REG103C18	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_12	5		
	GPIO_OUT_12	4		
	-	3:1	Reserved.	
	GPIO_IN_12	0		
0Dh (103C1Ah)	REG103C1A	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_13	5		
	GPIO_OUT_13	4		
	-	3:1	Reserved.	
	GPIO_IN_13	0		
0Eh (103C1Ch)	REG103C1C	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_14	5		
	GPIO_OUT_14	4		
	-	3:1	Reserved.	
	GPIO_IN_14	0		
14h (103C28h)	REG103C28	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	

**PADTOP Register (Bank = 103C)**

Index (Absolute)	Mnemonic	Bit	Description	
15h (103C2Ah)	FUART_GPIO_OEN_0	5		
	FUART_GPIO_OUT_0	4		
	-	3:1	Reserved.	
	FUART_GPIO_IN_0	0		
16h (103C2Ch)	REG103C2A	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	FUART_GPIO_OEN_1	5		
	FUART_GPIO_OUT_1	4		
	-	3:1	Reserved.	
	FUART_GPIO_IN_1	0		
17h (103C2Eh)	REG103C2C	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	FUART_GPIO_OEN_2	5		
	FUART_GPIO_OUT_2	4		
	-	3:1	Reserved.	
	FUART_GPIO_IN_2	0		
18h (103C30h)	REG103C2E	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	UART0_GPIO_OEN_0	5		
	UART0_GPIO_OUT_0	4		
	-	3:1	Reserved.	
	UART0_GPIO_IN_0	0		
19h (103C32h)	REG103C30	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	UART0_GPIO_OEN_1	5		
	UART0_GPIO_OUT_1	4		
	-	3:1	Reserved.	



PADTOP Register (Bank = 103C)				
Index (Absolute)	Mnemonic	Bit	Description	
1Ah (103C34h)	UART0_GPIO_IN_1	0		
	REG103C34	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	UART1_GPIO_OEN_0	5		
	UART1_GPIO_OUT_0	4		
	-	3:1	Reserved.	
	UART1_GPIO_IN_0	0		
1Bh (103C36h)	REG103C36	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	UART1_GPIO_OEN_1	5		
	UART1_GPIO_OUT_1	4		
	-	3:1	Reserved.	
	UART1_GPIO_IN_1	0		
	REG103C40	7:0	Default : 0x20	Access : RO, R/W
20h (103C40h)	-	7:6	Reserved.	
	TTL_GPIO_OEN_0	5		
	TTL_GPIO_OUT_0	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_0	0		
	REG103C42	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
21h (103C42h)	TTL_GPIO_OEN_1	5		
	TTL_GPIO_OUT_1	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_1	0		
	REG103C44	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_2	5		
22h (103C44h)	TTL_GPIO_OUT_2	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_2	0		
	REG103C46	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	

**PADTOP Register (Bank = 103C)**

Index (Absolute)	Mnemonic	Bit	Description	
24h (103C48h)	TTL_GPIO_OEN_3	5		
	TTL_GPIO_OUT_3	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_3	0		
25h (103C4Ah)	REG103C48	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_4	5		
	TTL_GPIO_OUT_4	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_4	0		
26h (103C4Ch)	REG103C4A	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_5	5		
	TTL_GPIO_OUT_5	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_5	0		
27h (103C4Eh)	REG103C4C	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_6	5		
	TTL_GPIO_OUT_6	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_6	0		
28h (103C50h)	REG103C4E	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_7	5		
	TTL_GPIO_OUT_7	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_7	0		
28h (103C50h)	REG103C50	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_8	5		
	TTL_GPIO_OUT_8	4		
	-	3:1	Reserved.	



PADTOP Register (Bank = 103C)				
Index (Absolute)	Mnemonic	Bit	Description	
	TTL_GPIO_IN_8	0		
29h (103C52h)	REG103C52	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_9	5		
	TTL_GPIO_OUT_9	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_9	0		
2Ah (103C54h)	REG103C54	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_10	5		
	TTL_GPIO_OUT_10	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_10	0		
2Bh (103C56h)	REG103C56	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_11	5		
	TTL_GPIO_OUT_11	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_11	0		
2Ch (103C58h)	REG103C58	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_12	5		
	TTL_GPIO_OUT_12	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_12	0		
2Dh (103C5Ah)	REG103C5A	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_13	5		
	TTL_GPIO_OUT_13	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_13	0		
2Eh (103C5Ch)	REG103C5C	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	

**PADTOP Register (Bank = 103C)**

Index (Absolute)	Mnemonic	Bit	Description	
2Fh (103C5Eh)	TTL_GPIO_OEN_14	5		
	TTL_GPIO_OUT_14	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_14	0		
30h (103C60h)	REG103C5E	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_15	5		
	TTL_GPIO_OUT_15	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_15	0		
31h (103C62h)	REG103C60	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_16	5		
	TTL_GPIO_OUT_16	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_16	0		
32h (103C64h)	REG103C62	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_17	5		
	TTL_GPIO_OUT_17	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_17	0		
33h (103C66h)	REG103C64	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_18	5		
	TTL_GPIO_OUT_18	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_18	0		
34h (103C68h)	REG103C66	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_19	5		
	TTL_GPIO_OUT_19	4		
	-	3:1	Reserved.	



PADTOP Register (Bank = 103C)				
Index (Absolute)	Mnemonic	Bit	Description	
34h (103C68h)	TTL_GPIO_IN_19	0		
	REG103C68	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_20	5		
	TTL_GPIO_OUT_20	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_20	0		
35h (103C6Ah)	REG103C6A	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_21	5		
	TTL_GPIO_OUT_21	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_21	0		
36h (103C6Ch)	REG103C6C	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_22	5		
	TTL_GPIO_OUT_22	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_22	0		
37h (103C6Eh)	REG103C6E	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_23	5		
	TTL_GPIO_OUT_23	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_23	0		
38h (103C70h)	REG103C70	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_24	5		
	TTL_GPIO_OUT_24	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_24	0		
39h (103C72h)	REG103C72	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	



PADTOP Register (Bank = 103C)				
Index (Absolute)	Mnemonic	Bit	Description	
3Ah (103C74h)	TTL_GPIO_OEN_25	5		
	TTL_GPIO_OUT_25	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_25	0		
3Bh (103C76h)	REG103C74	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_26	5		
	TTL_GPIO_OUT_26	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_26	0		
40h (103C80h)	REG103C76	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	TTL_GPIO_OEN_27	5		
	TTL_GPIO_OUT_27	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_27	0		
41h (103C82h)	REG103C80	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	IDAC_GPIO_OEN_0	5		
	IDAC_GPIO_OUT_0	4		
	-	3:1	Reserved.	
	IDAC_GPIO_IN_0	0		
42h (103C84h)	REG103C82	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	IDAC_GPIO_OEN_1	5		
	IDAC_GPIO_OUT_1	4		
	-	3:1	Reserved.	
	IDAC_GPIO_IN_1	0		
43h (103C84h)	REG103C84	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	HDMI_GPIO_OEN_0	5		
	HDMI_GPIO_OUT_0	4		
	-	3:1	Reserved.	



PADTOP Register (Bank = 103C)				
Index (Absolute)	Mnemonic	Bit	Description	
43h (103C86h)	HDMI_GPIO_IN_0	0		
	REG103C86	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	HDMI_GPIO_OEN_1	5		
	HDMI_GPIO_OUT_1	4		
	-	3:1	Reserved.	
	HDMI_GPIO_IN_1	0		
44h (103C88h)	REG103C88	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	HDMI_GPIO_OEN_2	5		
	HDMI_GPIO_OUT_2	4		
	-	3:1	Reserved.	
	HDMI_GPIO_IN_2	0		
	REG103C8A	7:0	Default : 0x20	Access : RO, R/W
45h (103C8Ah)	-	7:6	Reserved.	
	SATA_GPIO_OEN_0	5		
	SATA_GPIO_OUT_0	4		
	-	3:1	Reserved.	
	SATA_GPIO_IN_0	0		
	REG103CA0	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
50h (103CA0h)	SD_GPIO_OEN_0	5		
	SD_GPIO_OUT_0	4		
	-	3:1	Reserved.	
	SD_GPIO_IN_0	0		
	REG103CA2	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	SD_GPIO_OEN_1	5		
51h (103CA2h)	SD_GPIO_OUT_1	4		
	-	3:1	Reserved.	
	SD_GPIO_IN_1	0		
	REG103CA4	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	

**PADTOP Register (Bank = 103C)**

Index (Absolute)	Mnemonic	Bit	Description	
53h (103CA6h)	SD_GPIO_OEN_2	5		
	SD_GPIO_OUT_2	4		
	-	3:1	Reserved.	
	SD_GPIO_IN_2	0		
54h (103CA8h)	REG103CA6	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	SD_GPIO_OEN_3	5		
	SD_GPIO_OUT_3	4		
	-	3:1	Reserved.	
	SD_GPIO_IN_3	0		
55h (103CAAh)	REG103CA8	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	SD_GPIO_OEN_4	5		
	SD_GPIO_OUT_4	4		
	-	3:1	Reserved.	
	SD_GPIO_IN_4	0		
56h (103CACh)	REG103CAA	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	SD_GPIO_OEN_5	5		
	SD_GPIO_OUT_5	4		
	-	3:1	Reserved.	
	SD_GPIO_IN_5	0		
56h (103CACh)	REG103CAC	7:0	Default : 0x20	Access : RO, R/W
	-	7:6	Reserved.	
	SD_GPIO_OEN_6	5		
	SD_GPIO_OUT_6	4		
	-	3:1	Reserved.	
	SD_GPIO_IN_6	0		



FUART Register (Bank = 1102)

FUART Register (Bank = 1102)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (110200h)	REG110200	7:0	Default : 0x00	Access : R/W
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; note that writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; note that any incoming data are lost when FIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
02h (110204h)	REG110204	7:0	Default : 0x00	Access : R/W
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16 * divisor).	
04h (110208h)	REG110208	7:0	Default : 0x00	Access : R/W
	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00": FIFO empty; "01": 2 characters in the FIFO; "10": FIFO 1/4 full; "11": FIFO 1/2 full. Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/2 full; "11": FIFO 2 less than full.	

**FUART Register (Bank = 1102)**

Index (Absolute)	Mnemonic	Bit	Description	
		2.	Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "110": character timeout. "011": Receiver Line Status. "010": Receiver Data Available. "001": Transmitter Holding Register empty. "000": Modem Status.	
06h (11020Ch)	REG11020C	7:0	Default : 0x03	Access : R/W
	LCR_DL_ACCESS	7	Divisor Latch Access. 1: The divisor latches can be accessed.	
	LCR_BREAK_CTRL	6	Break control bit.	
	-	5	Reserved.	
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.	
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.	
	LCR_STOP_BITS	2	Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise.	
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits.	
08h (110210h)	REG110210	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.	
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. Out2 -> DCD.	
	MCR_OUT2	3	In loopback mode, connect to Data Carrier Detect (DCD) signal input.	
	MCR_OUT1	2	In loopback mode, connect to Ring Indicator (RI) signal input.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0".	

**FUART Register (Bank = 1102)**

Index (Absolute)	Mnemonic	Bit	Description	
	MCR_DTR	0	Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0".	
0Ah (110214h)	REG110214	7:0	Default : 0x00	Access : RO
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO. Generate a Transmitter Holding Register Empty interrupt.	
	LSR_BI	4	Break Interrupt bit.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
0Ch (110218h)	REG110218	7:0	Default : 0x00	Access : RO
	MSR_DCD_COMP	7	Complement of "DCD" or equal to "OUT2" in loopback.	
	MSR_RI_COMP	6	Complement of "RI" or equal to "OUT1" in loopback.	
	MSR_DSR_COMP	5	Complement of "DSR" or equal to "DTR" in loopback.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	MSR_DDCD	3	Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading.	
	MSR_TERI	2	Trailing Edge of Ring Indictor (TERI) detector. The "RI" line has changed its state from low to high. Clear when reading.	
	MSR_DDSR	1	Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator.	



FUART Register (Bank = 1102)

Index (Absolute)	Mnemonic	Bit	Description	
			"1": the "CTS" line has changed its state. Clear when reading.	
0Eh (11021Ch)	REG11021C	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	USR_RFF	4	Rx FIFO Full.	
	USR_RFNE	3	Rx FIFO Not Empty.	
	USR_TFE	2	Tx FIFO Empty.	
	USR_TFNF	1	Tx FIFO Not Full.	
	USR_BUSY	0	UART Busy.	
10h (110220h)	REG110220	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	TFL[5:0]	5:0	Tx FIFO level.	
12h (110224h)	REG110224	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	RFL[5:0]	5:0	Rx FIFO level.	

UART0 Register (Bank = 1108)

UART0 Register (Bank = 1108)

Index (Absolute)	Mnemonic	Bit	Description	
00h (110800h)	REG110800	7:0	Default : 0x00	Access : R/W
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; note that writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; note that any incoming data are lost when FIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
02h (110804h)	REG110804	7:0	Default : 0x00	Access : R/W
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and	

**UART0 Register (Bank = 1108)**

Index (Absolute)	Mnemonic	Bit	Description
			Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16 * divisor).
04h (110808h)	REG110808	7:0	Default : 0x00
	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00": FIFO empty; "01": 2 characters in the FIFO; "10": FIFO 1/4 full; "11": FIFO 1/2 full. Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/2 full; "11": FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "110": character timeout. "011": Receiver Line Status. "010": Receiver Data Available. "001": Transmitter Holding Register empty. "000": Modem Status.
06h (11080Ch)	REG11080C	7:0	Default : 0x03
	LCR_DL_ACCESS	7	Divisor Latch Access; 1: The divisor latches can be accessed.
	LCR_BREAK_CTRL	6	Break control bit.
	-	5	Reserved.
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.

**UART0 Register (Bank = 1108)**

Index (Absolute)	Mnemonic	Bit	Description
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.
	LCR_STOP_BITS	2	Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise.
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits.
08h (110810h)	REG110810	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. Out2 -> DCD.
	MCR_OUT2	3	In loopback mode, connect to Data Carrier Detect (DCD) signal input.
	MCR_OUT1	2	In loopback mode, connect to Ring Indicator (RI) signal input.
	MCR_RTS	1	Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0".
	MCR_DTR	0	Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0".
0Ah (110814h)	REG110814	7:0	Default : 0x00 Access : RO
	LSR_ERROR	7	Receiver FIFO Error bit.
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO. Generate a Transmitter Holding Register Empty interrupt.
	LSR_BI	4	Break Interrupt bit.
	LSR_FE	3	1: Framing Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.
	LSR_PE	2	1: Parity Error indicator.



UART0 Register (Bank = 1108)

Index (Absolute)	Mnemonic	Bit	Description	
			Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
0Ch (110818h)	REG110818	7:0	Default : 0x00	Access : RO
	MSR_DCD_COMP	7	Complement of "DCD" or equal to "OUT2" in loopback.	
	MSR_RI_COMP	6	Complement of "RI" or equal to "OUT1" in loopback.	
	MSR_DSR_COMP	5	Complement of "DSR" or equal to "DTR" in loopback.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	MSR_DDCD	3	Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading.	
	MSR_TERI	2	Trailing Edge of Ring Indicator (TERI) detector. The "RI" line has changed its state from low to high. Clear when reading.	
	MSR_DDSR	1	Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading.	
0Eh (11081Ch)	REG11081C	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	USR_RFF	4	Rx FIFO Full.	
	USR_RFNE	3	Rx FIFO Not Empty.	
	USR_TFE	2	Tx FIFO Empty.	
	USR_TFNF	1	Tx FIFO Not Full.	
	USR_BUSY	0	UART Busy.	
10h (110820h)	REG110820	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	TFL[5:0]	5:0	Tx FIFO level.	
12h (110824h)	REG110824	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	



UART0 Register (Bank = 1108)

Index (Absolute)	Mnemonic	Bit	Description
	RFL[5:0]	5:0	Rx FIFO level.

UART1 Register (Bank = 1109)

UART1 Register (Bank = 1109)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (110900h)	REG110900	7:0	Default : 0x00	Access : R/W
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; note that writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; note that any incoming data are lost when FIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
02h (110904h)	REG110904	7:0	Default : 0x00	Access : R/W
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16 * divisor).	
04h (110908h)	REG110908	7:0	Default : 0x00	Access : R/W
	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00": FIFO empty; "01": 2 characters in the FIFO;	

**UART1 Register (Bank = 1109)**

Index (Absolute)	Mnemonic	Bit	Description
			"10": FIFO 1/4 full; "11": FIFO 1/2 full. Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/2 full; "11": FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "110": character timeout. "011": Receiver Line Status. "010": Receiver Data Available. "001": Transmitter Holding Register empty. "000": Modem Status.
06h (11090Ch)	REG11090C	7:0	Default : 0x03
	LCR_DL_ACCESS	7	Divisor Latch Access. 1: The divisor latches can be accessed.
	LCR_BREAK_CTRL	6	Break control bit.
	-	5	Reserved.
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.
	LCR_STOP_BITS	2	Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise.
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits.
08h (110910h)	REG110910	7:0	Default : 0x00
	-	7:6	Reserved.
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. Out2 -> DCD.

**UART1 Register (Bank = 1109)**

Index (Absolute)	Mnemonic	Bit	Description	
0Ah (110914h)	MCR_OUT2	3	In loopback mode, connect to Data Carrier Detect (DCD) signal input.	
	MCR_OUT1	2	In loopback mode, connect to Ring Indicator (RI) signal input.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0".	
	MCR_DTR	0	Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0".	
0Ch (110918h)	REG110914	7:0	Default : 0x00	Access : RO
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO. Generate a Transmitter Holding Register Empty interrupt.	
	LSR BI	4	Break Interrupt bit.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
	REG110918	7:0	Default : 0x00	Access : RO
0Ch (110918h)	MSR_DCD_COMP	7	Complement of "DCD" or equal to "OUT2" in loopback.	
	MSR RI COMP	6	Complement of "RI" or equal to "OUT1" in loopback.	
	MSR_DSR_COMP	5	Complement of "DSR" or equal to "DTR" in loopback.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	MSR_DDCD	3	Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading.	
	MSR_TERI	2	Trailing Edge of Ring Indicator (TERI) detector.	



UART1 Register (Bank = 1109)

Index (Absolute)	Mnemonic	Bit	Description	
			The "RI" line has changed its state from low to high. Clear when reading.	
	MSR_DDSR	1	Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading.	
0Eh (11091Ch)	REG11091C	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	USR_RFF	4	Rx FIFO Full.	
	USR_RFNE	3	Rx FIFO Not Empty.	
	USR_TFE	2	Tx FIFO Empty.	
	USR_TFNF	1	Tx FIFO Not Full.	
	USR_BUSY	0	UART Busy.	
10h (110920h)	REG110920	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	TFL[5:0]	5:0	Tx FIFO level.	
12h (110924h)	REG110924	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	RFL[5:0]	5:0	Rx FIFO level.	

UART2 Register (Bank = 110A)

UART2 Register (Bank = 110A)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (110A00h)	REG110A00	7:0	Default : 0x00	Access : R/W
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; note that writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; note that any incoming data are lost when FIFO is full and an overrun error occurs.	



UART2 Register (Bank = 110A)				
Index (Absolute)	Mnemonic	Bit	Description	
			2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
02h (110A04h)	REG110A04	7:0	Default : 0x00	Access : R/W
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16 * divisor).	
04h (110A08h)	REG110A08	7:0	Default : 0x00	Access : R/W
	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00": FIFO empty; "01": 2 characters in the FIFO; "10": FIFO 1/4 full; "11": FIFO 1/2 full. Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/2 full; "11": FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "110": character timeout. "011": Receiver Line Status. "010": Receiver Data Available. "001": Transmitter Holding Register empty. "000": Modem Status.	
06h	REG110A0C	7:0	Default : 0x03	Access : R/W

**UART2 Register (Bank = 110A)**

Index (Absolute)	Mnemonic	Bit	Description
(110A0Ch)	LCR_DL_ACCESS	7	Divisor Latch Access. 1: The divisor latches can be accessed.
	LCR_BREAK_CTRL	6	Break control bit.
	-	5	Reserved.
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.
	LCR_STOP_BITS	2	Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise.
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits.
08h (110A10h)	REG110A10	7:0	Default : 0x00
	-	7:6	Reserved.
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. Out2 -> DCD.
	MCR_OUT2	3	In loopback mode, connect to Data Carrier Detect (DCD) signal input.
	MCR_OUT1	2	In loopback mode, connect to Ring Indicator (RI) signal input.
	MCR_RTS	1	Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0".
	MCR_DTR	0	Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0".
	REG110A14	7:0	Default : 0x00
	LSR_ERROR	7	Receiver FIFO Error bit.
0Ah (110A14h)	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO.



UART2 Register (Bank = 110A)			
Index (Absolute)	Mnemonic	Bit	Description
			Generate a Transmitter Holding Register Empty interrupt.
	LSR_BI	4	Break Interrupt bit.
	LSR_FE	3	1: Framing Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.
	LSR_PE	2	1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.
	LSR_DR	0	1: Received Data Ready indicator.
0Ch (110A18h)	REG110A18	7:0	Default : 0x00 Access : RO
	MSR_DCD_COMP	7	Complement of "DCD" or equal to "OUT2" in loopback.
	MSR_RI_COMP	6	Complement of "RI" or equal to "OUT1" in loopback.
	MSR_DSR_COMP	5	Complement of "DSR" or equal to "DTR" in loopback.
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.
	MSR_DDCD	3	Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading.
	MSR_TERI	2	Trailing Edge of Ring Indicator (TERI) detector. The "RI" line has changed its state from low to high. Clear when reading.
	MSR_DDSR	1	Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading.
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading.
0Eh (110A1Ch)	REG110A1C	7:0	Default : 0x00 Access : RO
	-	7:5	Reserved.
	USR_RFF	4	Rx FIFO Full.
	USR_RFNE	3	Rx FIFO Not Empty.
	USR_TFE	2	Tx FIFO Empty.
	USR_TFNF	1	Tx FIFO Not Full.
	USR_BUSY	0	UART Busy.



UART2 Register (Bank = 110A)

Index (Absolute)	Mnemonic	Bit	Description	
10h (110A20h)	REG110A20	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	TFL[5:0]	5:0	Tx FIFO level.	
12h (110A24h)	REG110A24	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	RFL[5:0]	5:0	Rx FIFO level.	

MSPI0 Register (Bank = 1110)

MSPI0 Register (Bank = 1110)				
Index (Absolute)	Mnemonic	Bit	Description	
30h (111060h)	REG111060	7:0	Default : 0x00	Access : R/W
	DATA_LENGTH[7:0]	7:0	DMA mode read/write data length.	
30h (111061h)	REG111061	7:0	Default : 0x00	Access : R/W
	DATA_LENGTH[15:8]	7:0	See description of '111060h'.	
31h (111062h)	REG111062	7:0	Default : 0x00	Access : R/W
	DATA_LENGTH[23:16]	7:0	See description of '111060h'.	
32h (111064h)	REG111064	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DMA_ENABLE	0	DMA mode enable. 1: Enable. 0: Disable.	
33h (111066h)	REG111066	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DMA_RW	0	DMA mode read/write. 0: DMA write only mode. 1: DMA read only mode.	
34h (111068h)	REG111068	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	READ_FROM LSB	0	Read data from LSB. 0: Close read from LSB. 1: Open read from LSB.	
40h	REG111080	7:0	Default : 0x00	Access : R/W



MSPI0 Register (Bank = 1110)				
Index (Absolute)	Mnemonic	Bit	Description	
(111080h)	MSPI_WD0[7:0]	7:0	Write buffer0.	
40h (111081h)	REG111081	7:0	Default : 0x00	Access : R/W
	MSPI_WD1[7:0]	7:0	Write buffer1.	
41h (111082h)	REG111082	7:0	Default : 0x00	Access : R/W
	MSPI_WD2[7:0]	7:0	Write buffer2.	
41h (111083h)	REG111083	7:0	Default : 0x00	Access : R/W
	MSPI_WD3[7:0]	7:0	Write buffer3.	
42h (111084h)	REG111084	7:0	Default : 0x00	Access : R/W
	MSPI_WD4[7:0]	7:0	Write buffer4.	
42h (111085h)	REG111085	7:0	Default : 0x00	Access : R/W
	MSPI_WD5[7:0]	7:0	Write buffer5.	
43h (111086h)	REG111086	7:0	Default : 0x00	Access : R/W
	MSPI_WD6[7:0]	7:0	Write buffer6.	
43h (111087h)	REG111087	7:0	Default : 0x00	Access : R/W
	MSPI_WD7[7:0]	7:0	Write buffer7.	
44h (111088h)	REG111088	7:0	Default : 0x00	Access : RO
	MSPI_RD0[7:0]	7:0	Read buffer0.	
44h (111089h)	REG111089	7:0	Default : 0x00	Access : RO
	MSPI_RD1[7:0]	7:0	Read buffer1.	
45h (11108Ah)	REG11108A	7:0	Default : 0x00	Access : RO
	MSPI_RD2[7:0]	7:0	Read buffer2.	
45h (11108Bh)	REG11108B	7:0	Default : 0x00	Access : RO
	MSPI_RD3[7:0]	7:0	Read buffer3.	
46h (11108Ch)	REG11108C	7:0	Default : 0x00	Access : RO
	MSPI_RD4[7:0]	7:0	Read buffer4.	
46h (11108Dh)	REG11108D	7:0	Default : 0x00	Access : RO
	MSPI_RD5[7:0]	7:0	Read buffer5.	
47h (11108Eh)	REG11108E	7:0	Default : 0x00	Access : RO
	MSPI_RD6[7:0]	7:0	Read buffer6.	
47h (11108Fh)	REG11108F	7:0	Default : 0x00	Access : RO
	MSPI_RD7[7:0]	7:0	Read buffer7.	
48h (111090h)	REG111090	7:0	Default : 0x00	Access : R/W
	MSPI_WBF_SIZE[7:0]	7:0	Set how many bytes will be transferred.	

**MSPI0 Register (Bank = 1110)**

Index (Absolute)	Mnemonic	Bit	Description
			Max size is 8 bytes. Min size is 0 byte.
48h (111091h)	REG111091	7:0	Default : 0x00 Access : R/W
	MSPI_RBF_SIZE[7:0]	7:0	Set how many bytes will be received. Max size is 8 bytes. Min size is 0 byte.
49h (111092h)	REG111092	7:0	Default : 0x00 Access : R/W
	MSPI_CTRL[7:0]	7:0	Control Register. Bit[7]: Clock Polarity, CPOL. 0: The SCK is set to 0 in idle state. 1: The SCK is set to 1 in idle state. Bit[6]: Clock Phase, CPHA. 0: Date is sampled when the SCK leaves the idle state. 1: Date is sampled when the SCK returns to idle state. Bit[5]: Reserved. Bit[4]: 3-wire mode. 0: Disable. 1: Enable. Bit[3]: Reserved. Bit[2]: Enable MSPI interrupt. 0: Disable. 1: Enable. Bit[1]: Reset. 0: Reset. 1: Not reset. Bit[0]: Enable MSPI. 0: Disable. 1: Enable.
49h (111093h)	REG111093	7:0	Default : 0x00 Access : R/W
	MSPI_CLOCK_RATE[7:0]	7:0	Bit[2:0] 3'b000: CPU_CLOCK/2. 3'b001: CPU_CLOCK/4. 3'b010: CPU_CLOCK/8. 3'b011: CPU_CLOCK/16. 3'b100: CPU_CLOCK/32. 3'b101: CPU_CLOCK/64. 3'b110: CPU_CLOCK/128. 3'b111: CPU_CLOCK/256. Bit[7:3]: Reserved.



MSPI0 Register (Bank = 1110)				
Index (Absolute)	Mnemonic	Bit	Description	
4Ah (111094h)	REG111094	7:0	Default : 0x00	Access : R/W
	TR_START_TIME[7:0]	7:0	The time from "reg_MSPI_trigger" to first SPI clock. 0x00: Delay 1 MSPI clock. 0x01: Delay 2 MSPI clocks. 0x0f: Delay 16 MSPI clocks. 0xff: Delay 256 MSPI clocks.	
4Ah (111095h)	REG111095	7:0	Default : 0x00	Access : R/W
	TR_END_TIME[7:0]	7:0	The time from last SPI clock to "reg_MSPI_done_flag". 0x00: Delay 1 MSPI clock. 0x01: Delay 2 MSPI clocks. 0x0f: Delay 16 MSPI clocks. 0xff: Delay 256 MSPI clocks.	
4Bh (111096h)	REG111096	7:0	Default : 0x00	Access : R/W
	TBYTE_INTERVAL_TIME[7:0]	7:0	The time between byte to byte transfers. 0x00: No delay. 0x01: Delay 1 MSPI clock. 0x0f: Delay 15 MSPI clocks. 0xff: Delay 255 MSPI clocks.	
4Bh (111097h)	REG111097	7:0	Default : 0x00	Access : R/W
	RW_TURN_AROUND_TIME[7:0]	7:0	The time between last write and first read. 0x00: No delay. 0x01: Delay 1 MSPI clock. 0x0f: Delay 15 MSPI clocks. 0xff: Delay 255 MSPI clocks.	
4Ch (111098h)	REG111098	7:0	Default : 0xFF	Access : R/W
	MSPI_WD2_BIT_SEL[1:0]	7:6	Bit Length selection for write buffer2.	
	MSPI_WD1_BIT_SEL[2:0]	5: 3	Bit Length selection for write buffer1.	
	MSPI_WD0_BIT_SEL[2:0]	2:0	Bit Length selection for write buffer0. The number of bits to be transferred in write buffer0. 3'b111: 8 bits. 3'b110: 7 bits. 3'b101: 6 bits. 3'b100: 5 bits. 3'b011: 4 bits. 3'b010: 3 bits. 3'b001: 2 bits. 3'b000: 1 bit.	
4Ch	REG111099	7:0	Default : 0x0F	Access : R/W



MSPI0 Register (Bank = 1110)				
Index (Absolute)	Mnemonic	Bit	Description	
(111099h)	-	7:4	Reserved.	
	MSPI_WD3_BIT_SEL[2:0]	3:1	Bit Length selection for write buffer3.	
	MSPI_WD2_BIT_SEL[2]	0	See description of '111098h'.	
4Dh (11109Ah)	REG11109A	7:0	Default : 0xFF	Access : R/W
	MSPI_WD6_BIT_SEL[1:0]	7:6	Bit Length selection for write buffer6.	
	MSPI_WD5_BIT_SEL[2:0]	5: 3	Bit Length selection for write buffer5.	
	MSPI_WD4_BIT_SEL[2:0]	2:0	Bit Length selection for write buffer4.	
4Dh (11109Bh)	REG11109B	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	MSPI_WD7_BIT_SEL[2:0]	3:1	Bit Length selection for write buffer7.	
	MSPI_WD6_BIT_SEL[2]	0	See description of '11109Ah'.	
4Eh (11109Ch)	REG11109C	7:0	Default : 0xFF	Access : R/W
	MSPI_RD2_BIT_SEL[1:0]	7:6	Bit Length selection for read buffer2.	
	MSPI_RD1_BIT_SEL[2:0]	5: 3	Bit Length selection for read buffer1.	
	MSPI_RD0_BIT_SEL[2:0]	2:0	Bit Length selection for read buffer0. The number of bits to be received in read buffer0. 3'b111: 8 bits. 3'b110: 7 bits. 3'b101: 6 bits. 3'b100: 5 bits. 3'b011: 4 bits. 3'b010: 3 bits. 3'b001: 2 bits. 3'b000: 1 bit.	
	REG11109D	7:0	Default : 0x0F	Access : R/W
4Eh (11109Dh)	-	7:4	Reserved.	
	MSPI_RD3_BIT_SEL[2:0]	3:1	Bit Length selection for read buffer3.	
	MSPI_RD2_BIT_SEL[2]	0	See description of '11109Ch'.	
	REG11109E	7:0	Default : 0xFF	Access : R/W
4Fh (11109Eh)	MSPI_RD6_BIT_SEL[1:0]	7:6	Bit Length selection for read buffer6.	
	MSPI_RD5_BIT_SEL[2:0]	5: 3	Bit Length selection for read buffer5.	
	MSPI_RD4_BIT_SEL[2:0]	2:0	Bit Length selection for read buffer4.	
	REG11109F	7:0	Default : 0x0F	Access : R/W
4Fh (11109Fh)	-	7:4	Reserved.	
	MSPI_RD7_BIT_SEL[2:0]	3:1	Bit Length selection for read buffer7.	

**MSPI0 Register (Bank = 1110)**

Index (Absolute)	Mnemonic	Bit	Description	
	MSPI_RD6_BIT_SEL[2]	0	See description of '11109Eh'.	
50h (1110A0h)	REG1110A0	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	LSB_FIRST	0	LSB of data transfer first.	
5Ah (1110B4h)	REG1110B4	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	MSPI_TRIGGER	0	Start data transfer.	
5Bh (1110B6h)	REG1110B6	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	MSPI_DONE_FLAG	0	Busy status, HW sets to one when transfer is completed. 1: Transfer done or interrupt pending. 0: Transfer busy or interrupt not pending.	
5Ch (1110B8h)	REG1110B8	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	MSPI_CLEAR_DONE_FLAG	0	SW needs to set this bit to clear done flag or interrupt.	
5Dh (1110BAh)	REG1110BA	7:0	Default : 0x00	Access : RO, R/W
	-	7:3	Reserved.	
	SPI_WP_C	2	Write-protect input for SPI flash.	
	SPI_WP_OEN	1	Write-protect output enable (oen) for SPI flash.	
	SPI_WP_I	0	Write-protect output for SPI flash.	
5Eh (1110BCh)	REG1110BC	7:0	Default : 0x00	Access : RO, R/W
	-	7:3	Reserved.	
	SPI_HOLD_C	2	Hold input for SPI flash.	
	SPI_HOLD_OEN	1	Hold output enable (oen) for SPI flash.	
	SPI_HOLD_I	0	Hold output for SPI flash.	
5Fh (1110BEh)	REG1110BE	7:0	Default : 0xFF	Access : R/W
	CHIP_SELECT8	7	Chip-select for SPI Device6. 0: Enable. 1: Disable.	
	CHIP_SELECT7	6	Chip-select for SPI Device5. 0: Enable. 1: Disable.	
	CHIP_SELECT6	5	Chip-select for SPI Device4. 0: Enable. 1: Disable.	

**MSPI0 Register (Bank = 1110)**

Index (Absolute)	Mnemonic	Bit	Description
	CHIP_SELECT5	4	Chip-select for SPI Device3. 0: Enable. 1: Disable.
	CHIP_SELECT4	3	Chip-select for SPI Device2. 0: Enable. 1: Disable.
	CHIP_SELECT3	2	Chip-select for SPI Device1. 0: Enable. 1: Disable.
	CHIP_SELECT2	1	Chip-select for SPI Device1. 0: Enable. 1: Disable.
	CHIP_SELECT1	0	Chip-select for SPI Device1. 0: Enable. 1: Disable.



MIIC0 Register (Bank = 1118)

MIIC0 Register (Bank = 1118)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (111800h)	REG111800	7:0	Default : 0x01	Access : R/W
	MIIC_CFG[7:0]	7:0	MIIC configuration register. Bit[7]: reg_error_det_en. 0: Disable. 1: Enable. Bit[6]: reg_oen_push_en. 0: Disable. 1: Enable. Bit[5]: Enable filter. 0: Disable. 1: Enable. Bit[4]: Enable timeout interrupt. 0: Disable. 1: Enable. Bit[3]: Enable clock stretching. 0: Disable. 1: Enable. Bit[2]: Interrupt enable. 0: Disable. 1: Enable. Bit[1]: Enable DMA. 0: Disable. 1: Enable. Bit[0]: Reset. 0: Reset. 1: Not reset.	
01h (111802h)	REG111802	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	CMD_START	0	MIIC command. [0]: Start.	
01h (111803h)	REG111803	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	CMD_STOP	0	MIIC command. [1]: Stop.	
02h (111804h)	REG111804	7:0	Default : 0x00	Access : R/W
	WDATA[7:0]	7:0	I2C write data.	
02h	REG111805	7:0	Default : 0x00	Access : RO



MIIC0 Register (Bank = 1118)				
Index (Absolute)	Mnemonic	Bit	Description	
(111805h)	-	7:1	Reserved.	
	WRITE_ACK	0	I2C ACK for write data from slave IIC.	
03h (111806h)	REG111806	7:0	Default : 0x00	Access : RO
	RDATA[7:0]	7:0	I2C read data.	
03h (111807h)	REG111807	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	ACK_BIT	1	I2C ACK for read data to slave IIC.	
	RDATA_EN	0	I2C read data trigger.	
04h (111808h)	REG111808	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	FLAG	0	MIIC interrupt flag.	
05h (11180Ah)	REG11180A	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	MIIC_STATE[4:0]	4:0	MIIC final state machine (debug only).	
05h (11180Bh)	REG11180B	7:0	Default : 0x00	Access : RO
	-	7	Reserved.	
	MIIC_INT_STATUS[6:0]	6:0	interrupt status. [0]: Ic_start_det_intr. [1]: Ic_stop_det_intr. [2]: Ic_rx_done_intr. [3]: Ic_tx_done_intr. [4]: Clock_stretching_intr. [5]: Scl_error_inte. [6]: Time_out_intr.	
06h (11180Ch)	REG11180C	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	SCLO	4	Pad_SCLO.	
	-	3:2	Reserved.	
	SDAI	1	Pad_SDAI.	
	SCLI	0	Pad_SCLI.	
08h (111810h)	REG111810	7:0	Default : 0x00	Access : R/W
	STOP_CNT[7:0]	7:0	This register sets the SCL and SDA count for stop.	
08h (111811h)	REG111811	7:0	Default : 0x00	Access : R/W
	STOP_CNT[15:8]	7:0	See description of '111810h'.	

**MIIC0 Register (Bank = 1118)**

Index (Absolute)	Mnemonic	Bit	Description	
09h (111812h)	REG111812	7:0	Default : 0x00	Access : R/W
	HCNT[7:0]	7:0	This register sets the SCL clock high-period count.	
09h (111813h)	REG111813	7:0	Default : 0x00	Access : R/W
	HCNT[15:8]	7:0	See description of '111812h'.	
0Ah (111814h)	REG111814	7:0	Default : 0x00	Access : R/W
	LCNT[7:0]	7:0	This register sets the SCL clock low-period count.	
0Ah (111815h)	REG111815	7:0	Default : 0x00	Access : R/W
	LCNT[15:8]	7:0	See description of '111814h'.	
0Bh (111816h)	REG111816	7:0	Default : 0x00	Access : R/W
	SDA_CNT[7:0]	7:0	This register sets the clock count between falling edge SCL and SDA.	
0Bh (111817h)	REG111817	7:0	Default : 0x00	Access : R/W
	SDA_CNT[15:8]	7:0	See description of '111816h'.	
0Ch (111818h)	REG111818	7:0	Default : 0x00	Access : R/W
	START_CNT[7:0]	7:0	This register sets the SCL and SDA count for start.	
0Ch (111819h)	REG111819	7:0	Default : 0x00	Access : R/W
	START_CNT[15:8]	7:0	See description of '111818h'.	
0Dh (11181Ah)	REG11181A	7:0	Default : 0x00	Access : R/W
	DATA_LAT_CNT[7:0]	7:0	This register sets the data latch timing.	
0Dh (11181Bh)	REG11181B	7:0	Default : 0x00	Access : R/W
	DATA_LAT_CNT[15:8]	7:0	See description of '11181Ah'.	
0Eh (11181Ch)	REG11181C	7:0	Default : 0x00	Access : R/W
	TIMEOUT_CNT[7:0]	7:0	This register sets timing delay of timeout interrupt occurred.	
0Eh (11181Dh)	REG11181D	7:0	Default : 0x00	Access : R/W
	TIMEOUT_CNT[15:8]	7:0	See description of '11181Ch'.	
0Fh (11181Eh)	REG11181E	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SCLI_DELAY[2:0]	2:0	Reserved.	
20h (111840h)	REG111840	7:0	Default : 0x1A	Access : RO, R/W
	-	7:6	Reserved.	
	MIU_NS	5	MIU secure bit.	
	MIU_PRIORITY	4	Set MIU priority.	

**MIIC0 Register (Bank = 1118)**

Index (Absolute)	Mnemonic	Bit	Description	
	MIU_RST	3	MIU software reset.	
	DMA_CFG[2:0]	2:0	DMA configuration register. Bit[2]: Interrupt enable. 0: Disable. 1: Enable. Bit[1]: DMA software Reset. 0: Reset. 1: Not reset.	
21h (111842h)	REG111842	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[7:0]	7:0	Get tx data or put rx data address in DRAM.	
21h (111843h)	REG111843	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[15:8]	7:0	See description of '111842h'.	
22h (111844h)	REG111844	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[23:16]	7:0	See description of '111842h'.	
22h (111845h)	REG111845	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[31:24]	7:0	See description of '111842h'.	
23h (111846h)	REG111846	7:0	Default : 0x00	Access : R/W
	MIU_SEL	7	MIIC channel select.	
	READ_CMD	6	MIIC transfer format. 1: Read. 0: Write.	
	STOP_DISABLE	5	MIIC transfer format. 1: S + data .. 0: S + data ...+ P.	
	-	4:0	Reserved.	
24h (111848h)	REG111848	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DMA_TRANSFER_DONE	0	SW needs to set this bit to clear transfer_done flag or interrupt in order to receive the subsequent DMA transfer_done flag or interrupt.	
25h (11184Ah)	REG11184A	7:0	Default : 0x00	Access : R/W
	CMD_DATA[7:0]	7:0	I2C Tx Data Buffer and Command.	
25h (11184Bh)	REG11184B	7:0	Default : 0x00	Access : R/W
	CMD_DATA[15:8]	7:0	See description of '11184Ah'.	
26h	REG11184C	7:0	Default : 0x00	Access : R/W



MIIC0 Register (Bank = 1118)				
Index (Absolute)	Mnemonic	Bit	Description	
(11184Ch)	CMD_DATA[23:16]	7:0	See description of '11184Ah'.	
26h (11184Dh)	REG11184D	7:0	Default : 0x00	Access : R/W
	CMD_DATA[31:24]	7:0	See description of '11184Ah'.	
27h (11184Eh)	REG11184E	7:0	Default : 0x00	Access : R/W
	CMD_DATA[39: 32]	7:0	See description of '11184Ah'.	
27h (11184Fh)	REG11184F	7:0	Default : 0x00	Access : R/W
	CMD_DATA[47:40]	7:0	See description of '11184Ah'.	
28h (111850h)	REG111850	7:0	Default : 0x00	Access : R/W
	CMD_DATA[55:48]	7:0	See description of '11184Ah'.	
28h (111851h)	REG111851	7:0	Default : 0x00	Access : R/W
	CMD_DATA[63: 56]	7:0	See description of '11184Ah'.	
29h (111852h)	REG111852	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CMD_LEN[3:0]	3:0	Transfer command register length (0~8).	
2Ah (111854h)	REG111854	7:0	Default : 0x00	Access : R/W
	DATA_LEN[7:0]	7:0	Transfer command register length.	
2Ah (111855h)	REG111855	7:0	Default : 0x00	Access : R/W
	DATA_LEN[15:8]	7:0	See description of '111854h'.	
2Bh (111856h)	REG111856	7:0	Default : 0x00	Access : R/W
	DATA_LEN[23:16]	7:0	See description of '111854h'.	
2Bh (111857h)	REG111857	7:0	Default : 0x00	Access : R/W
	DATA_LEN[31:24]	7:0	See description of '111854h'.	
2Ch (111858h)	REG111858	7:0	Default : 0x00	Access : RO
	DMA_TC[7:0]	7:0	DMA transfer count register for MIIC0 (debug only).	
2Ch (111859h)	REG111859	7:0	Default : 0x00	Access : RO
	DMA_TC[15:8]	7:0	See description of '111858h'.	
2Dh (11185Ah)	REG11185A	7:0	Default : 0x00	Access : RO
	DMA_TC[23:16]	7:0	See description of '111858h'.	
2Dh (11185Bh)	REG11185B	7:0	Default : 0x00	Access : RO
	DMA_TC[31:24]	7:0	See description of '111858h'.	
2Eh (11185Ch)	REG11185C	7:0	Default : 0x00	Access : R/W
	SAR[7:0]	7:0	I2C Slave Address. [9:0]: 10-bit mode slave address.	



MIICO Register (Bank = 1118)				
Index (Absolute)	Mnemonic	Bit	Description	
			[6:0]: Normal mode slave address.	
2Eh (11185Dh)	REG11185D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	10BIT_MODE	2	I2C Slave Address mode setting. 1: 10-bit mode slave address. 0: Normal mode slave address.	
	SAR[9: 8]	1:0	See description of '11185Ch'.	
2Fh (11185Eh)	REG11185E	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DMA_TRIGGER	0	DMA transfer trigger.	
2Fh (11185Fh)	REG11185F	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	RE_TRIGGER	0	DMA transfer RE_TRIGGER, for data transfer not complete.	
31h (111862h)	REG111862	7:0	Default : 0x00	Access : RO
	STATE[7:0]	7:0	DMA FSM (debug only).	
31h (111863h)	REG111863	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	MIU_LAST_DONE_Z	0	MIU last done z (debug only).	



MIIC1 Register (Bank = 1119)

MIIC1 Register (Bank = 1119)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (111900h)	REG111900	7:0	Default : 0x01	Access : R/W
	MIIC_CFG[7:0]	7:0	MIIC configuration register. Bit[7]: reg_error_det_en. 0: Disable. 1: Enable. Bit[6]: reg_oen_push_en. 0: Disable. 1: Enable. Bit[5]: Enable filter. 0: Disable. 1: Enable. Bit[4]: Enable timeout interrupt. 0: Disable. 1: Enable. Bit[3]: Enable clock stretching. 0: Disable. 1: Enable. Bit[2]: Interrupt enable. 0: Disable. 1: Enable. Bit[1]: Enable DMA. 0: Disable. 1: Enable. Bit[0]: Reset. 0: Reset. 1: Not reset.	
01h (111902h)	REG111902	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	CMD_START	0	MIIC command. [0]: Start.	
01h (111903h)	REG111903	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	CMD_STOP	0	MIIC command. [1]: Stop.	
02h (111904h)	REG111904	7:0	Default : 0x00	Access : R/W
	WDATA[7:0]	7:0	I2C write data.	
02h	REG111905	7:0	Default : 0x00	Access : RO



MIIC1 Register (Bank = 1119)				
Index (Absolute)	Mnemonic	Bit	Description	
(111905h)	-	7:1	Reserved.	
	WRITE_ACK	0	I2C ACK for write data from slave IIC.	
03h (111906h)	REG111906	7:0	Default : 0x00	Access : RO
	RDATA[7:0]	7:0	I2C read data.	
03h (111907h)	REG111907	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	ACK_BIT	1	I2C ACK for read data to slave IIC.	
	RDATA_EN	0	I2C read data trigger.	
04h (111908h)	REG111908	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	FLAG	0	MIIC interrupt flag.	
05h (11190Ah)	REG11190A	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	MIIC_STATE[4:0]	4:0	MIIC final state machine (debug only).	
05h (11190Bh)	REG11190B	7:0	Default : 0x00	Access : RO
	-	7	Reserved.	
	MIIC_INT_STATUS[6:0]	6:0	Interrupt status. [0]: Ic_start_det_intr. [1]: Ic_stop_det_intr. [2]: Ic_rx_done_intr. [3]: Ic_tx_done_intr. [4]: Clock_stretching_intr. [5]: Scl_error_inte. [6]: Time_out_intr.	
06h (11190Ch)	REG11190C	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	SCLO	4	Pad_SCLO.	
	-	3:2	Reserved.	
	SDAI	1	Pad_SDAI.	
	SCLI	0	Pad_SCLI.	
08h (111910h)	REG111910	7:0	Default : 0x00	Access : R/W
	STOP_CNT[7:0]	7:0	This register sets the SCL and SDA count for stop.	
08h (111911h)	REG111911	7:0	Default : 0x00	Access : R/W
	STOP_CNT[15:8]	7:0	See description of '111910h'.	

**MIIC1 Register (Bank = 1119)**

Index (Absolute)	Mnemonic	Bit	Description	
09h (111912h)	REG111912	7:0	Default : 0x00	Access : R/W
	HCNT[7:0]	7:0	This register sets the SCL clock high-period count.	
09h (111913h)	REG111913	7:0	Default : 0x00	Access : R/W
	HCNT[15:8]	7:0	See description of '111912h'.	
0Ah (111914h)	REG111914	7:0	Default : 0x00	Access : R/W
	LCNT[7:0]	7:0	This register sets the SCL clock low-period count.	
0Ah (111915h)	REG111915	7:0	Default : 0x00	Access : R/W
	LCNT[15:8]	7:0	See description of '111914h'.	
0Bh (111916h)	REG111916	7:0	Default : 0x00	Access : R/W
	SDA_CNT[7:0]	7:0	This register sets the clock count between falling edge SCL and SDA.	
0Bh (111917h)	REG111917	7:0	Default : 0x00	Access : R/W
	SDA_CNT[15:8]	7:0	See description of '111916h'.	
0Ch (111918h)	REG111918	7:0	Default : 0x00	Access : R/W
	START_CNT[7:0]	7:0	This register sets the SCL and SDA count for start.	
0Ch (111919h)	REG111919	7:0	Default : 0x00	Access : R/W
	START_CNT[15:8]	7:0	See description of '111918h'.	
0Dh (11191Ah)	REG11191A	7:0	Default : 0x00	Access : R/W
	DATA_LAT_CNT[7:0]	7:0	This register sets the data latch timing.	
0Dh (11191Bh)	REG11191B	7:0	Default : 0x00	Access : R/W
	DATA_LAT_CNT[15:8]	7:0	See description of '11191Ah'.	
0Eh (11191Ch)	REG11191C	7:0	Default : 0x00	Access : R/W
	TIMEOUT_CNT[7:0]	7:0	This register sets timing delay of timeout interrupt occurred.	
0Eh (11191Dh)	REG11191D	7:0	Default : 0x00	Access : R/W
	TIMEOUT_CNT[15:8]	7:0	See description of '11191Ch'.	
0Fh (11191Eh)	REG11191E	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SCLI_DELAY[2:0]	2:0	Reserved.	
20h (111940h)	REG111940	7:0	Default : 0x1A	Access : RO, R/W
	-	7:6	Reserved.	
	MIU_NS	5	MIU secure bit.	
	MIU_PRIORITY	4	Set MIU priority.	


MIIC1 Register (Bank = 1119)

Index (Absolute)	Mnemonic	Bit	Description	
	MIU_RST	3	MIU software reset.	
	DMA_CFG[2:0]	2:0	DMA configuration register. Bit[2]: Interrupt enable. 0: Disable. 1: Enable. Bit[1]: DMA software Reset. 0: Reset. 1: Not reset.	
21h (111942h)	REG111942	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[7:0]	7:0	Get tx data or put rx data address in DRAM.	
21h (111943h)	REG111943	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[15:8]	7:0	See description of '111942h'.	
22h (111944h)	REG111944	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[23:16]	7:0	See description of '111942h'.	
22h (111945h)	REG111945	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[31:24]	7:0	See description of '111942h'.	
23h (111946h)	REG111946	7:0	Default : 0x00	Access : R/W
	MIU_SEL	7	MIIC channel select.	
	READ_CMD	6	MIIC transfer format. 1: Read. 0: Write.	
	STOP_DISABLE	5	MIIC transfer format. 1: S + data .. 0: S + data ...+ P.	
	-	4:0	Reserved.	
24h (111948h)	REG111948	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DMA_TRANSFER_DONE	0	SW needs to set this bit to clear transfer_done flag or interrupt in order to receive the subsequent DMA transfer_done flag or interrupt.	
25h (11194Ah)	REG11194A	7:0	Default : 0x00	Access : R/W
	CMD_DATA[7:0]	7:0	I2C Tx Data Buffer and Command.	
25h (11194Bh)	REG11194B	7:0	Default : 0x00	Access : R/W
	CMD_DATA[15:8]	7:0	See description of '11194Ah'.	
26h	REG11194C	7:0	Default : 0x00	Access : R/W

**MIIC1 Register (Bank = 1119)**

Index (Absolute)	Mnemonic	Bit	Description	
(11194Ch)	CMD_DATA[23:16]	7:0	See description of '11194Ah'.	
26h (11194Dh)	REG11194D	7:0	Default : 0x00	Access : R/W
	CMD_DATA[31:24]	7:0	See description of '11194Ah'.	
27h (11194Eh)	REG11194E	7:0	Default : 0x00	Access : R/W
	CMD_DATA[39: 32]	7:0	See description of '11194Ah'.	
27h (11194Fh)	REG11194F	7:0	Default : 0x00	Access : R/W
	CMD_DATA[47:40]	7:0	See description of '11194Ah'.	
28h (111950h)	REG111950	7:0	Default : 0x00	Access : R/W
	CMD_DATA[55:48]	7:0	See description of '11194Ah'.	
28h (111951h)	REG111951	7:0	Default : 0x00	Access : R/W
	CMD_DATA[63: 56]	7:0	See description of '11194Ah'.	
29h (111952h)	REG111952	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CMD_LEN[3:0]	3:0	Transfer command register length (0~8).	
2Ah (111954h)	REG111954	7:0	Default : 0x00	Access : R/W
	DATA_LEN[7:0]	7:0	Transfer command register length.	
2Ah (111955h)	REG111955	7:0	Default : 0x00	Access : R/W
	DATA_LEN[15:8]	7:0	See description of '111954h'.	
2Bh (111956h)	REG111956	7:0	Default : 0x00	Access : R/W
	DATA_LEN[23:16]	7:0	See description of '111954h'.	
2Bh (111957h)	REG111957	7:0	Default : 0x00	Access : R/W
	DATA_LEN[31:24]	7:0	See description of '111954h'.	
2Ch (111958h)	REG111958	7:0	Default : 0x00	Access : RO
	DMA_TC[7:0]	7:0	DMA transfer count register for MIIC0 (debug only).	
2Ch (111959h)	REG111959	7:0	Default : 0x00	Access : RO
	DMA_TC[15:8]	7:0	See description of '111958h'.	
2Dh (11195Ah)	REG11195A	7:0	Default : 0x00	Access : RO
	DMA_TC[23:16]	7:0	See description of '111958h'.	
2Dh (11195Bh)	REG11195B	7:0	Default : 0x00	Access : RO
	DMA_TC[31:24]	7:0	See description of '111958h'.	
2Eh (11195Ch)	REG11195C	7:0	Default : 0x00	Access : R/W
	SAR[7:0]	7:0	I2C Slave Address. [9:0]: 10-bit mode slave address.	



MIIC1 Register (Bank = 1119)				
Index (Absolute)	Mnemonic	Bit	Description	
			[6:0]: Normal mode slave address.	
2Eh (11195Dh)	REG11195D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	10BIT_MODE	2	I2C Slave Address mode setting. 1: 10-bit mode slave address. 0: Normal mode slave address.	
	SAR[9: 8]	1:0	See description of '11195Ch'.	
2Fh (11195Eh)	REG11195E	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DMA_TRIGGER	0	DMA transfer trigger.	
2Fh (11195Fh)	REG11195F	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	RE_TRIGGER	0	DMA transfer RE_TRIGGER, for data transfer not complete.	
31h (111962h)	REG111962	7:0	Default : 0x00	Access : RO
	STATE[7:0]	7:0	DMA FSM (debug only).	
31h (111963h)	REG111963	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	MIU_LAST_DONE_Z	0	MIU last done z (debug only).	



REGISTER TABLE REVISION HISTORY

Date	Bank	Register
05/16/2019		<ul style="list-style-type: none">Created first version