ETH zürich

MemPool meets Systolic

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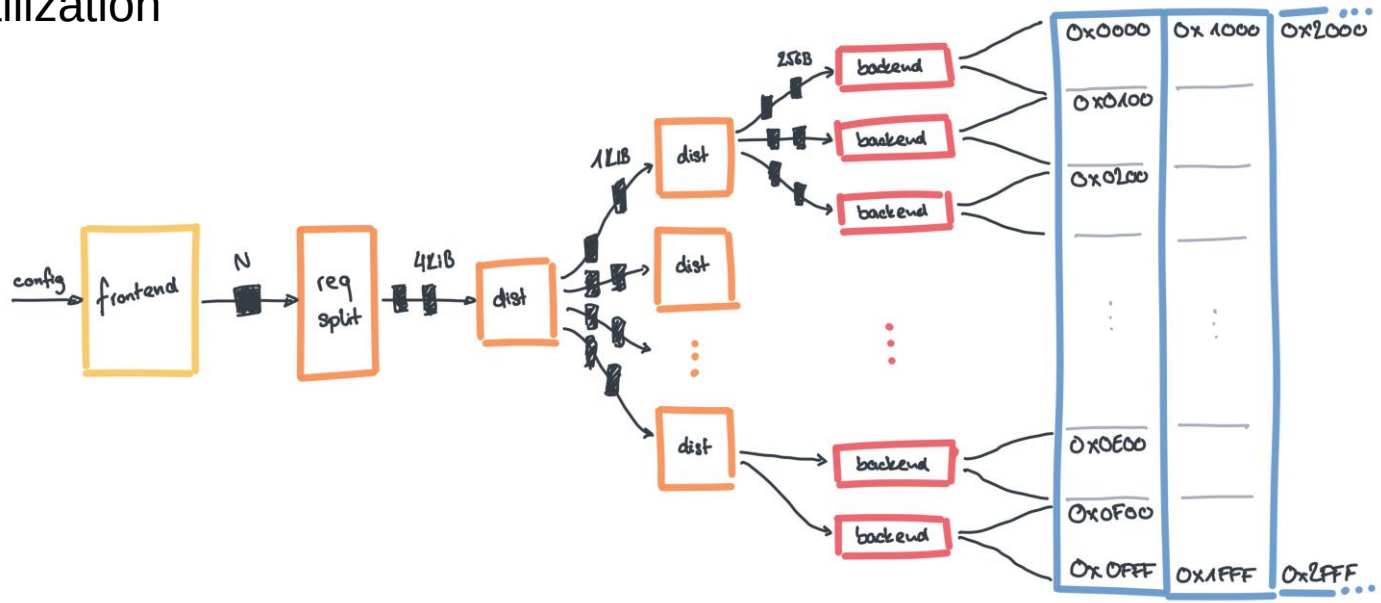
DMA and timing loops

- DMA fully integrated in MemPool's backend
  - All timing loops are fixed
  - Timing is not impacted
  - 2% area overhead introduced by DMA
- DMA benchmarking started
  - We can achieve up to 97% channel utilization



Timing loop issues

- Loops in handshaking
  - Snitch's register file write port ↔ TCDM adapter
  - Register file write could be optimized: Always ready
  - TCDM adapter needed an additional register to decouple input and output port
- This cuts a long path between Snitch and the interconnects

Systolic

- Presented our preliminary work at OSCAR
  - Workshop at ISCA
- Sergio has fixed several issues in the current implementation