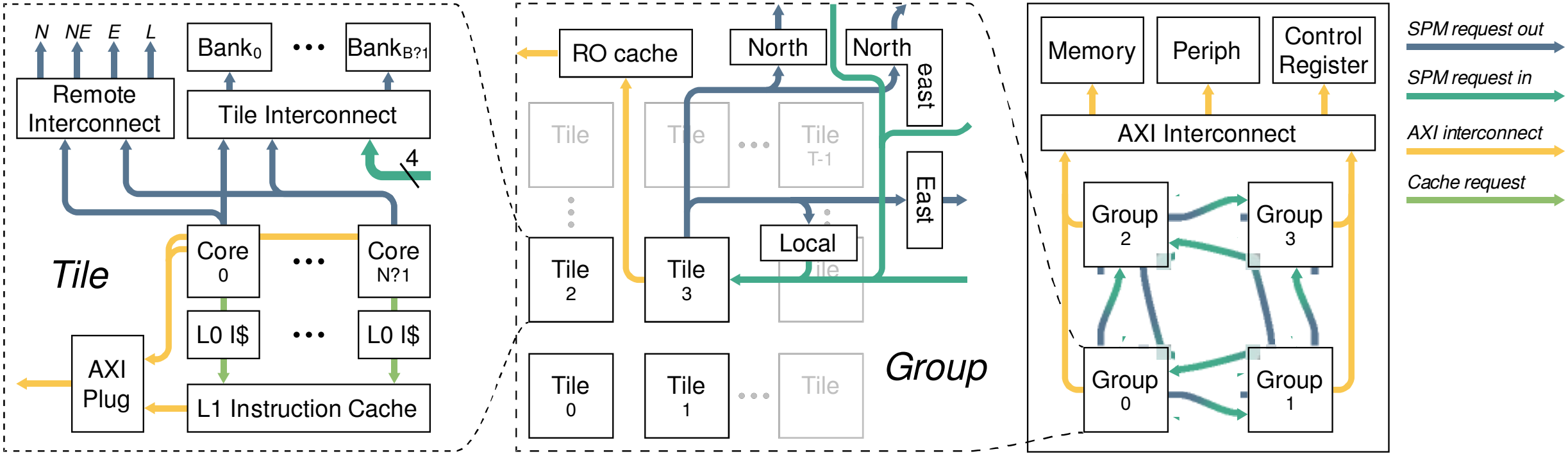
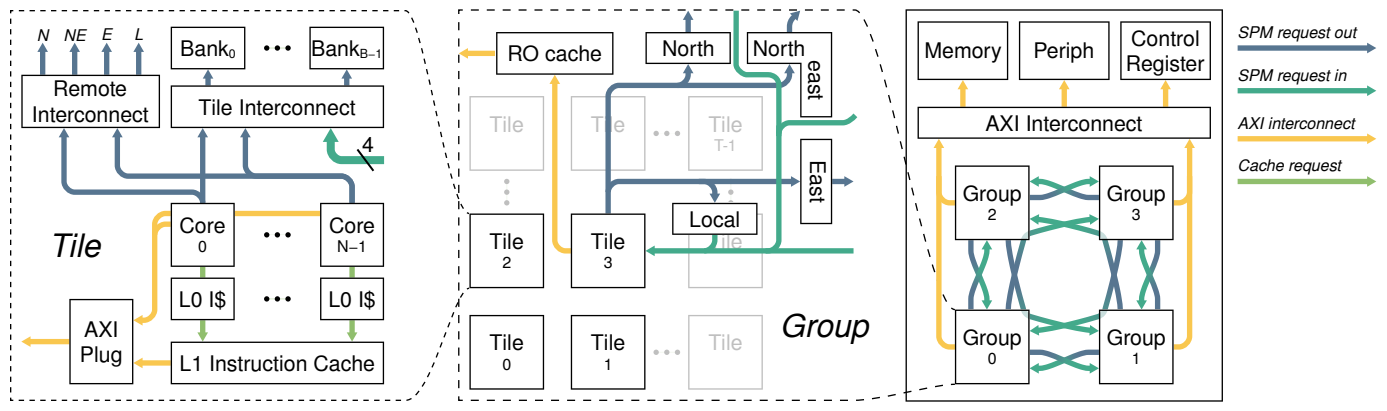
ETH zürich

MemPool meets Systolic

Samuel Riedel
Matheus Cavalcante
Prof. Luca Benini

MemPool Overview

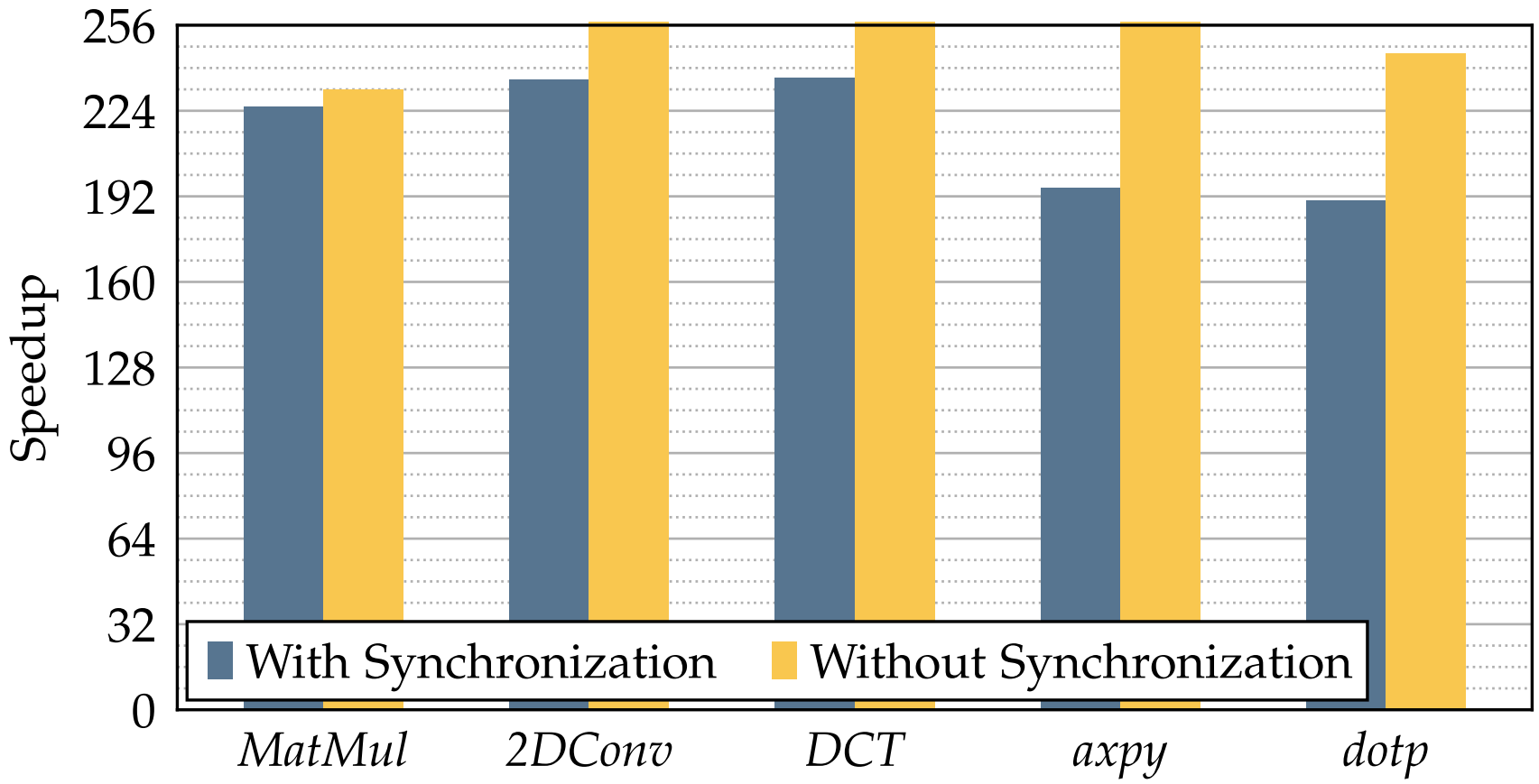



N
NE
E
L
Remote Interconnect
Bank0
BankB−1
Tile Interconnect
4
Tile
Core 0
Core N−1
L0 I$
L0 I$
AXI Plug
L1 Instruction Cache
RO cache
North
North east
East
Local
Tile 2
Tile 3
Tile 0
Tile 1
Tile T-1
Group
Memory
Periph
Control Register
AXI Interconnect
Group 2
Group 3
Group 0
Group 1
SPM request out
SPM request in
AXI interconnect
Cache request

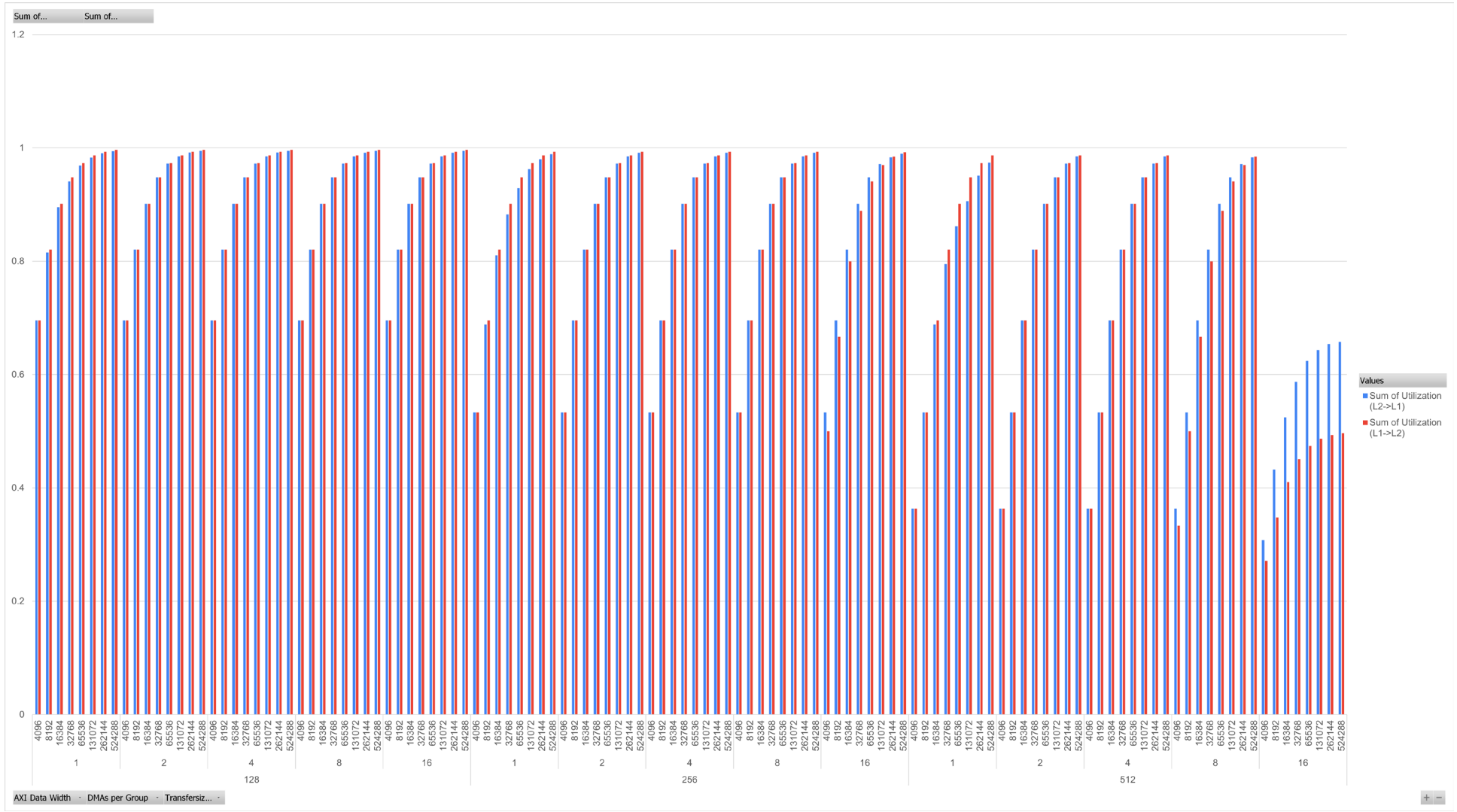
MemPool Overview

- 256 RV32IMAXpulpimg Snitch cores
  - Distributed across 4 groups of 16 tiles each
  - 4 cores per tile
- 1 MiB of L1 SRAM memory
  - Accessible in 5 cycles
- Hierarchical AXI interconnect and cache hierarchy for instructions

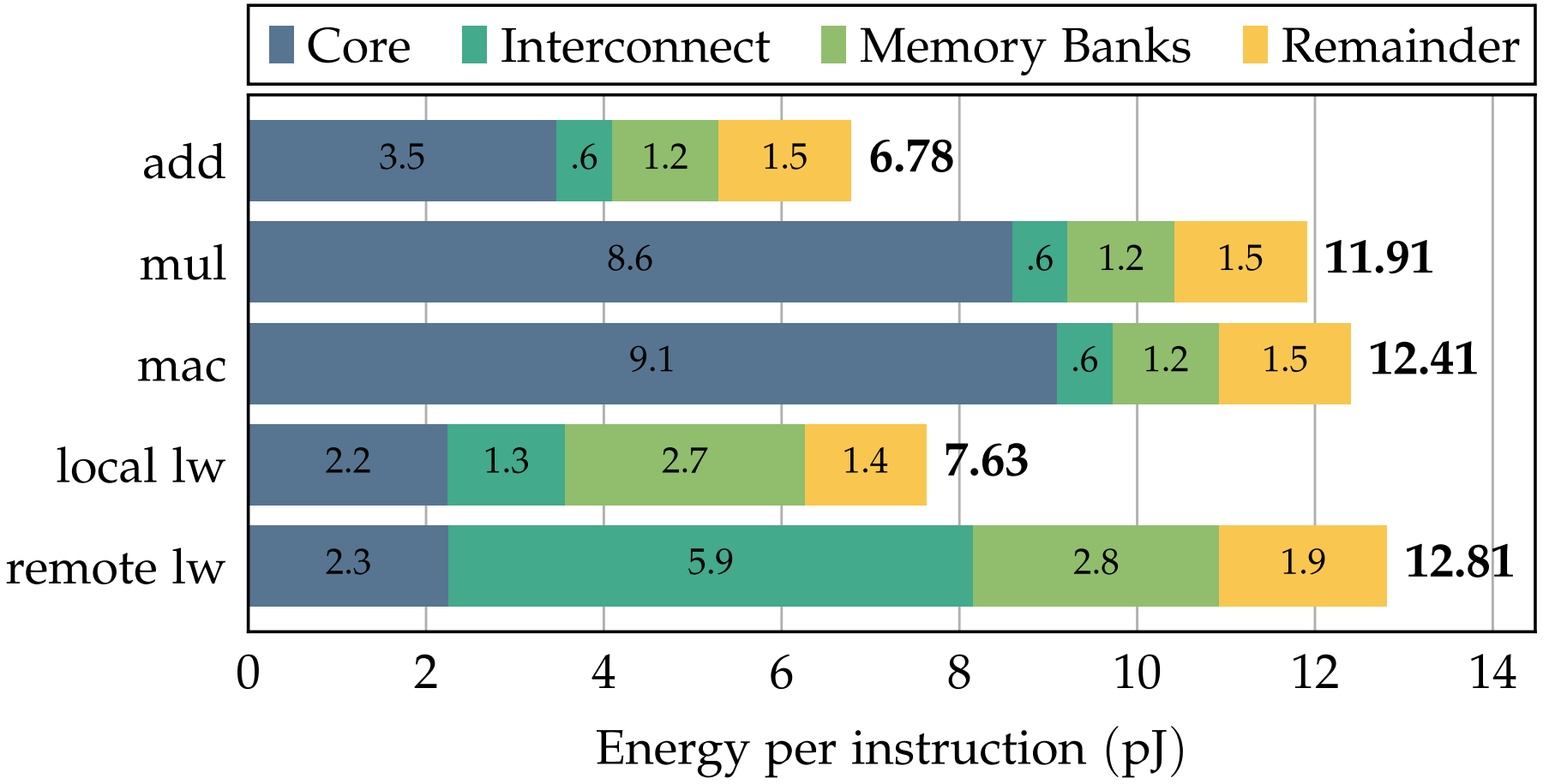
MemPool Scaling



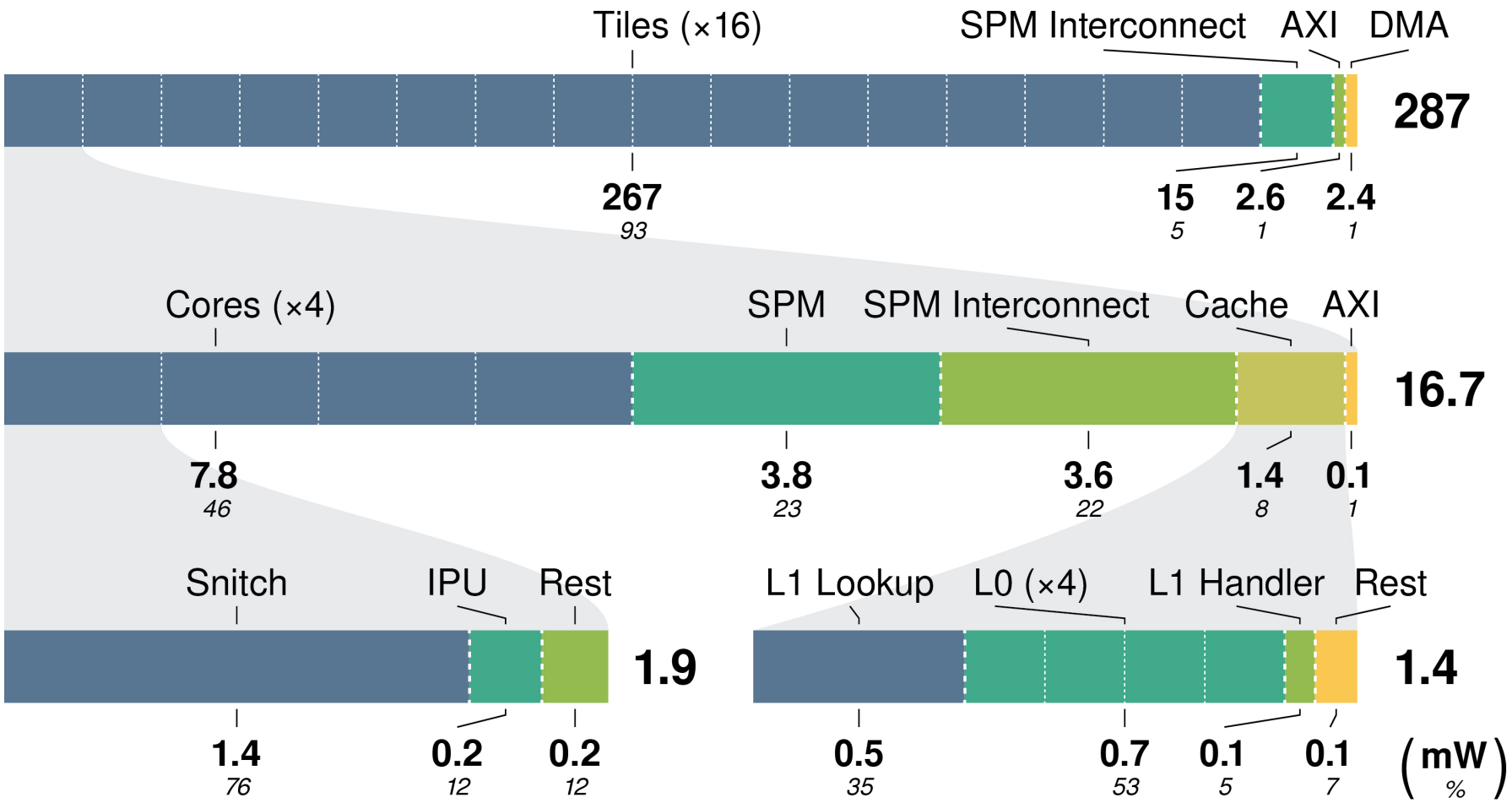
DMA Benchmarking



Instruction Energy



Power Breakdown



Systolic MemPool

- Cleaning up software queues implementation: Done
  - Improved parametrization
- Merging the Queue push/pop adapter: Done
  - Will be merged as a separate unit that can be instantiated for the systolic MemPool
- Work in progress:
  - Cleaning up the 2D convolution: Done
  - Benchmarking in progress