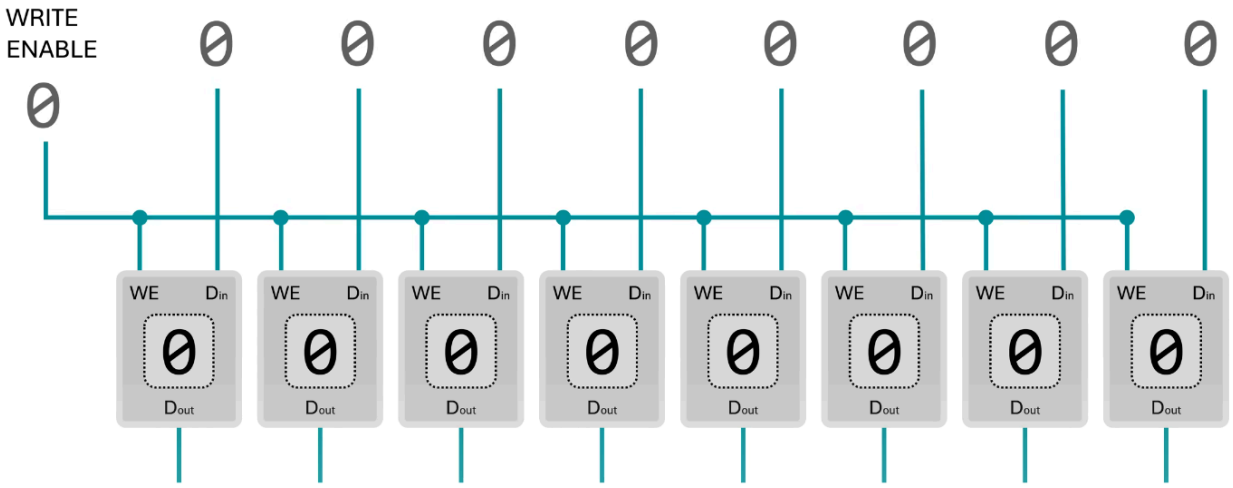
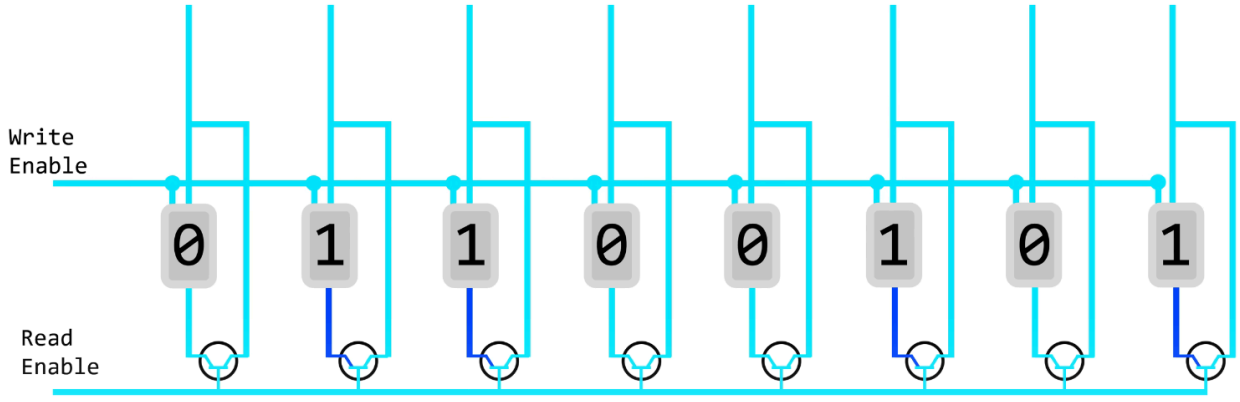
Chapter 3 - Simple CPU

Now that we have two of the core components understood from a transistor level - the RAM and the ALU, we are well on our way to build a minimal CPU. First, let's remind ourselves of the register structure that we came up with in the last chapter.

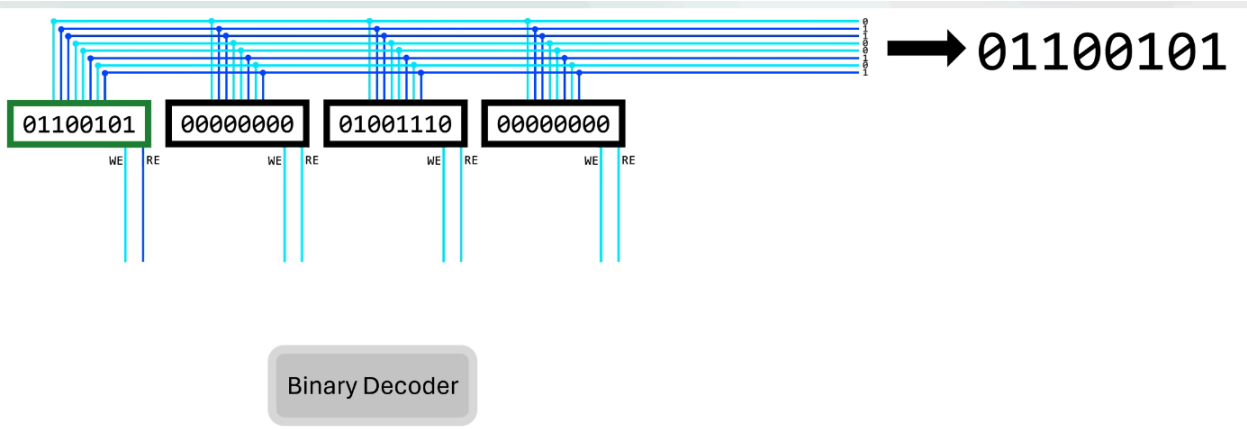


We can modify this in the same way we did the SRAM gated latches, by combining the data in and data out lines, and adding a read enable line.



This enables us with the same advantages as SRAM - we can write to and read from individual registers by using one data line and controlling which register it

reaches by using a decoder. The decoder does this by controlling the ‘write-enable’ and ‘read-enable’ lines on every register.



Binary Decoder