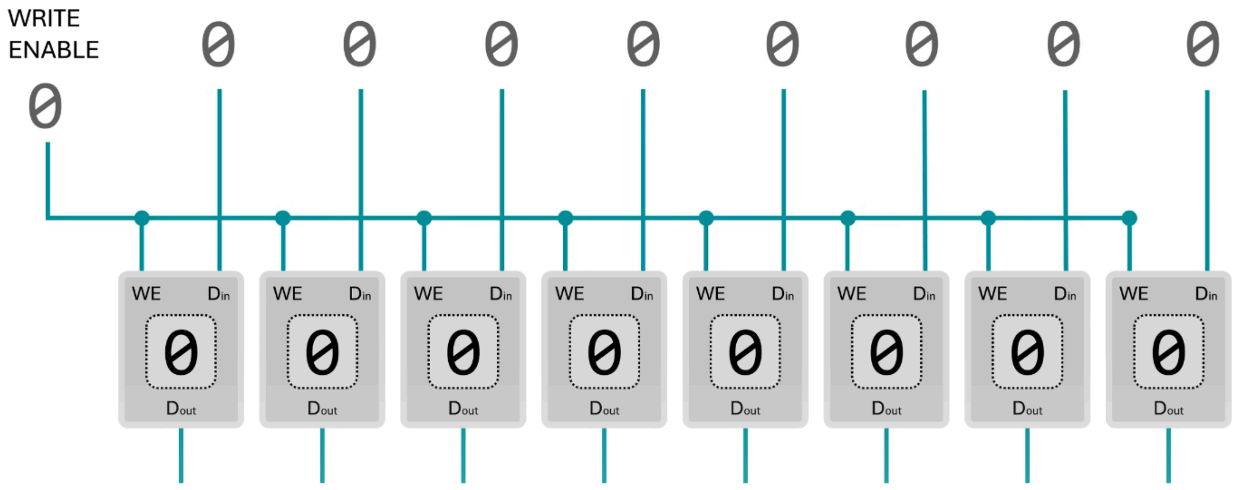
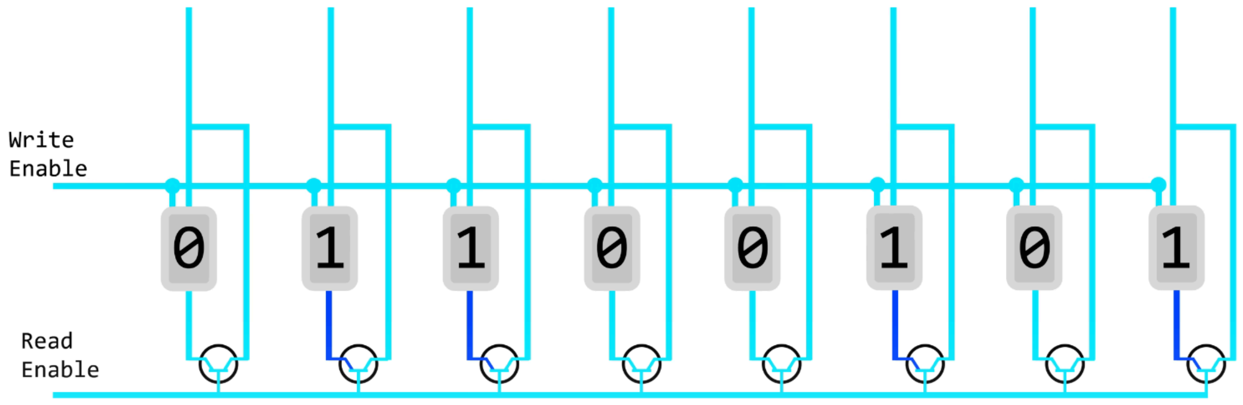
Chapter 3 - Simple CPU

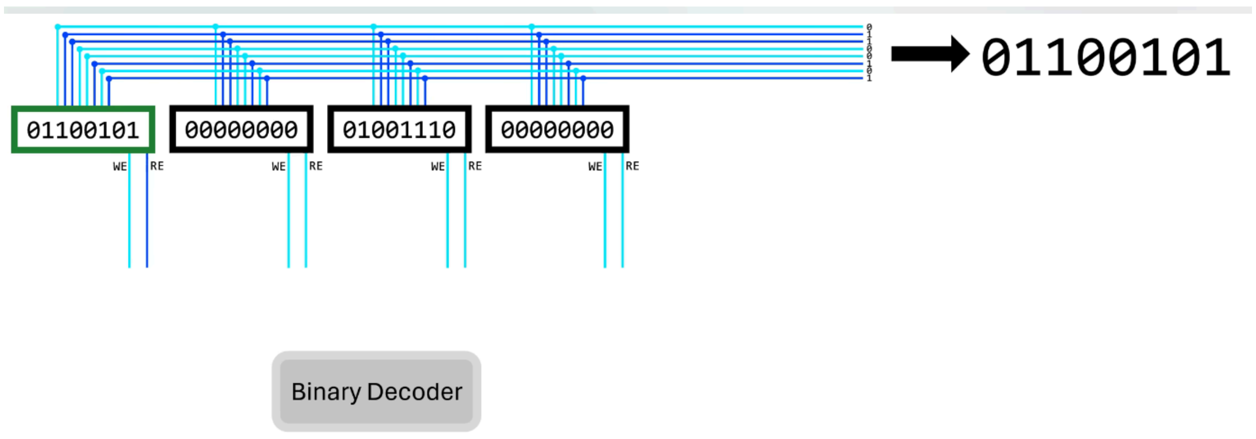
Now that we have two of the core components understood from a transistor level - the RAM and the ALU, we are well on our way to build a minimal CPU. First, let's remind ourselves of the register structure that we came up with in the last chapter.



We can modify this in the same way we did the SRAM gated latches, by combining the data in and data out lines, and adding a read enable line.



This enables us with the same advantages as SRAM - we can write to and read from individual registers by using one data line and controlling which register it reaches by using a decoder. The decoder does this by controlling the ‘write-enable’ and ‘read-enable’ lines on every register.



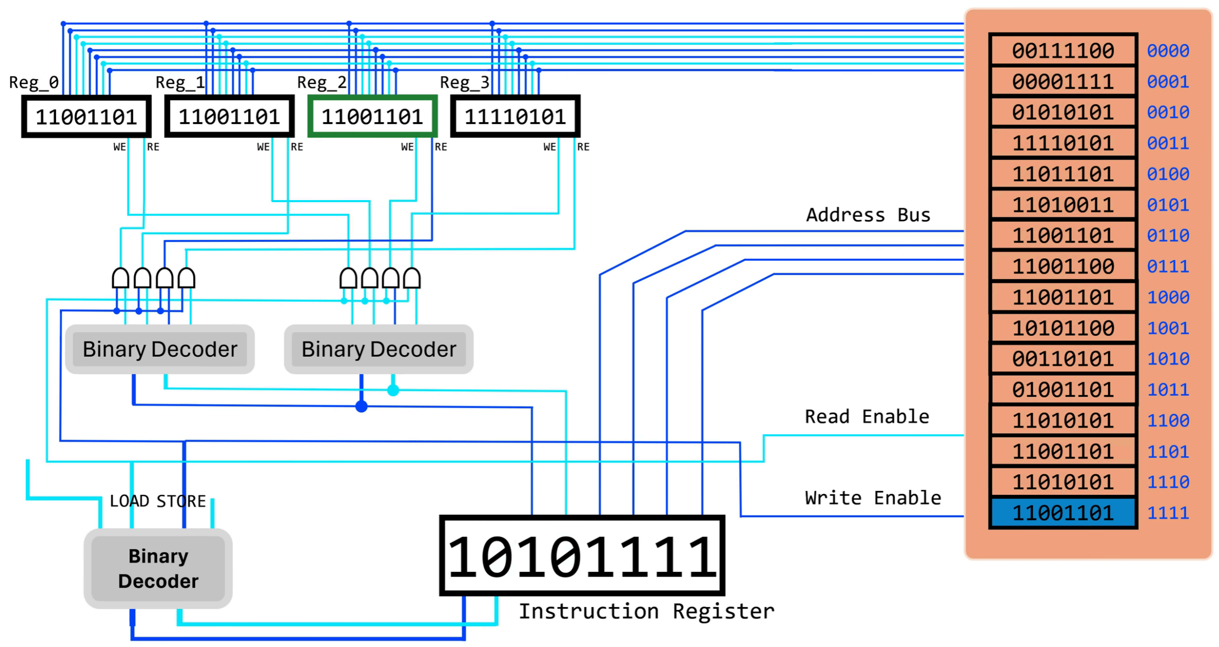
Now, let’s look at implementing some assembly instructions - in particular lets look at load and store. These two instructions are in the following format:

- Load Register_Name Address (Ex: Load R1 1101) - loads the data stored in the memory pointed by the address into the register
- Store Register_Name Address (Ex: Store R1 1101) - stores the data in the register into the memory pointed by the address

Assembly instruction is machine code in a format that is easier for us to understand. Both load and store instructions are in binary format in their simplest form. This means that we can implement these instructions easily by using decoders in the following format:

- First stage decoder would be for the load/store part. The decoder would take in this code and if it receives store, would set write enable high and if it receives load, would set read enable high.
- Second stage decoder would be to access the registers. We only want to read/write from one register at a time and this decoder would be connected to write enable and read enable lines. This is the same decoder as the one drawn above.

Both decoders can be connected in the following manner to achieve implementation of these assembly instructions.


Reg_0
11001101
Reg_1
11001101
Reg_2
11001101
Reg_3
11110101
WE
RE
Binary Decoder
Binary Decoder
LOAD
STORE
Binary Decoder
10101111
Instruction Register
Address Bus
Read Enable
Write Enable
00111100 0000
00001111 0001
01010101 0010
11110101 0011
11011101 0100
11010011 0101
11001101 0110
11001100 0111
11001101 1000
10101100 1001
00110101 1010
01001101 1011
11010101 1100
11001101 1101
11010101 1110
11001101 1111