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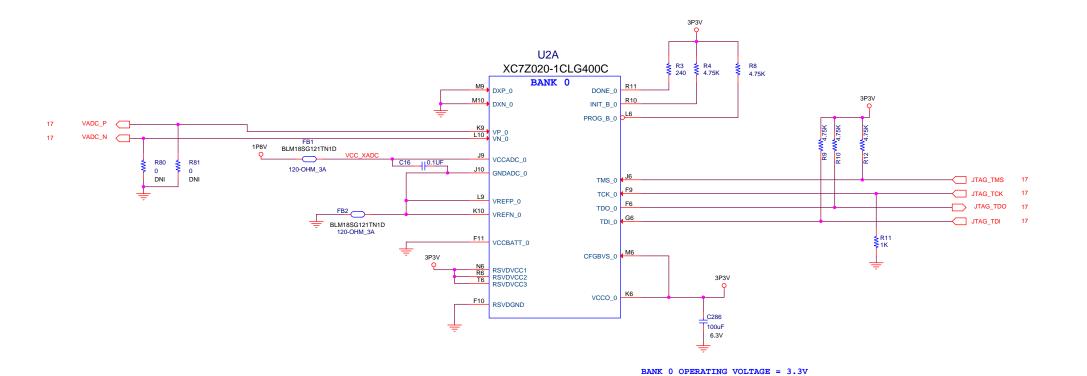
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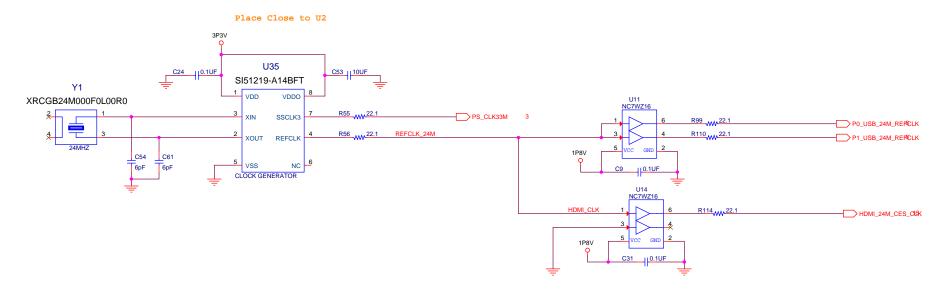
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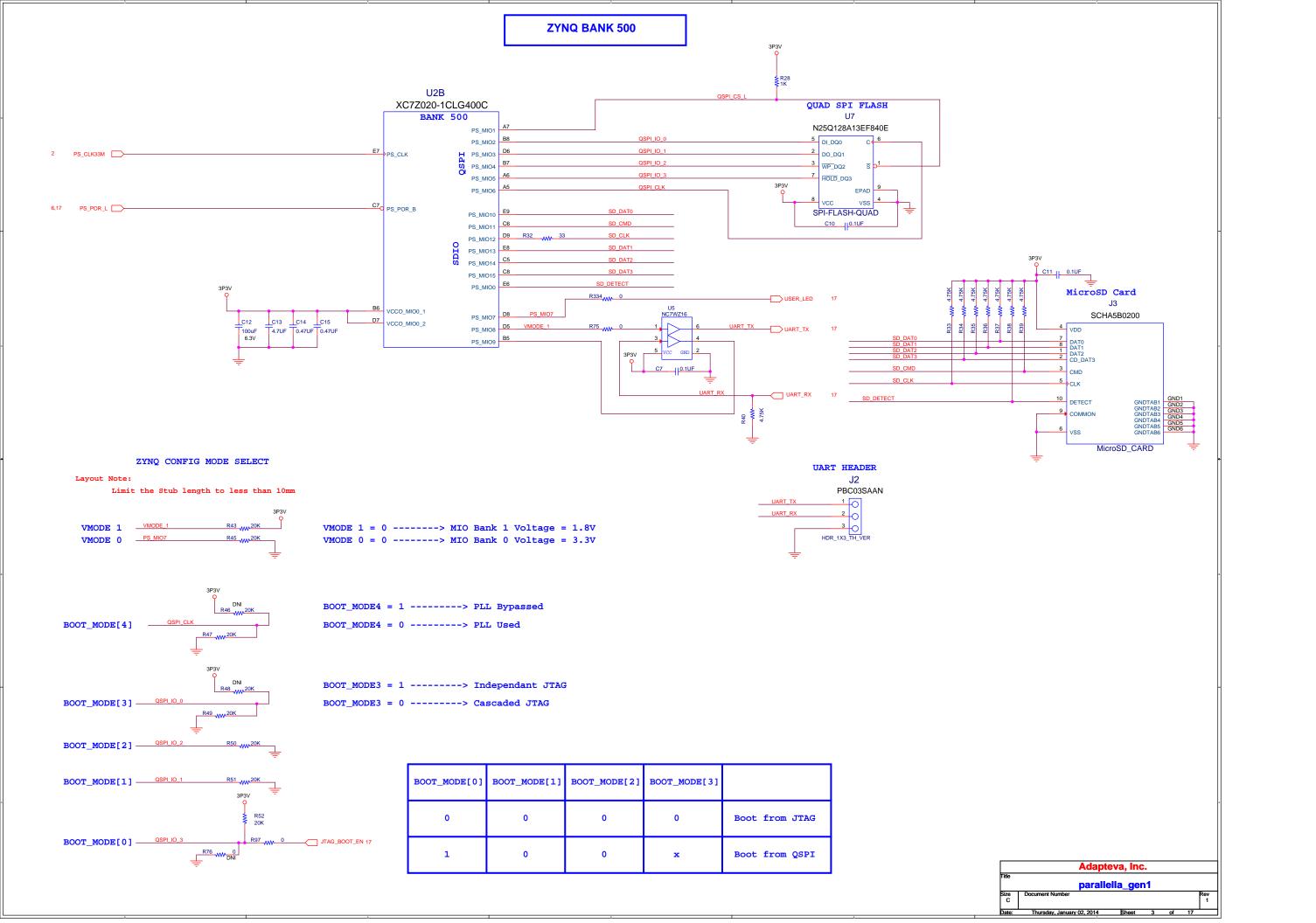
ZYNQ BANK0

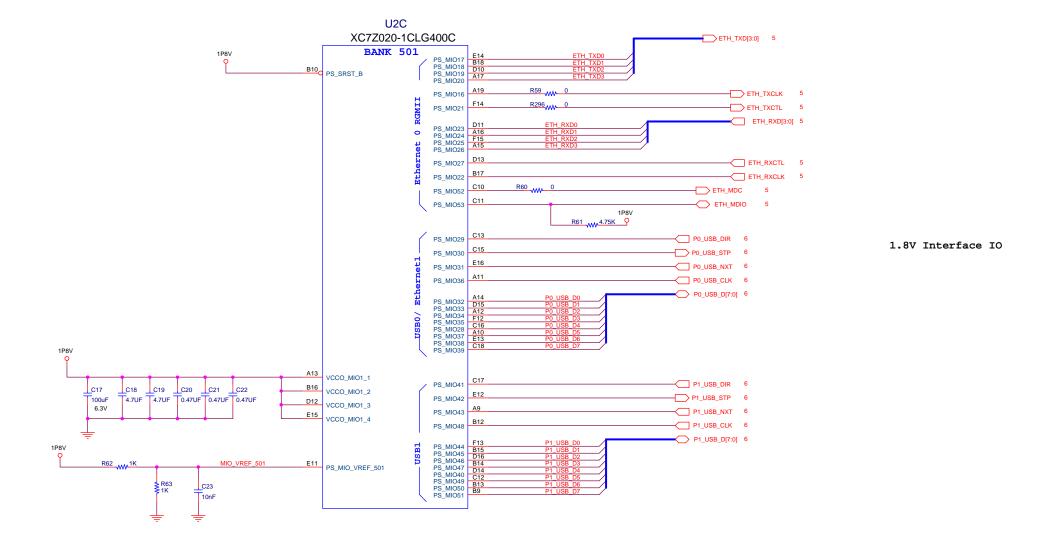


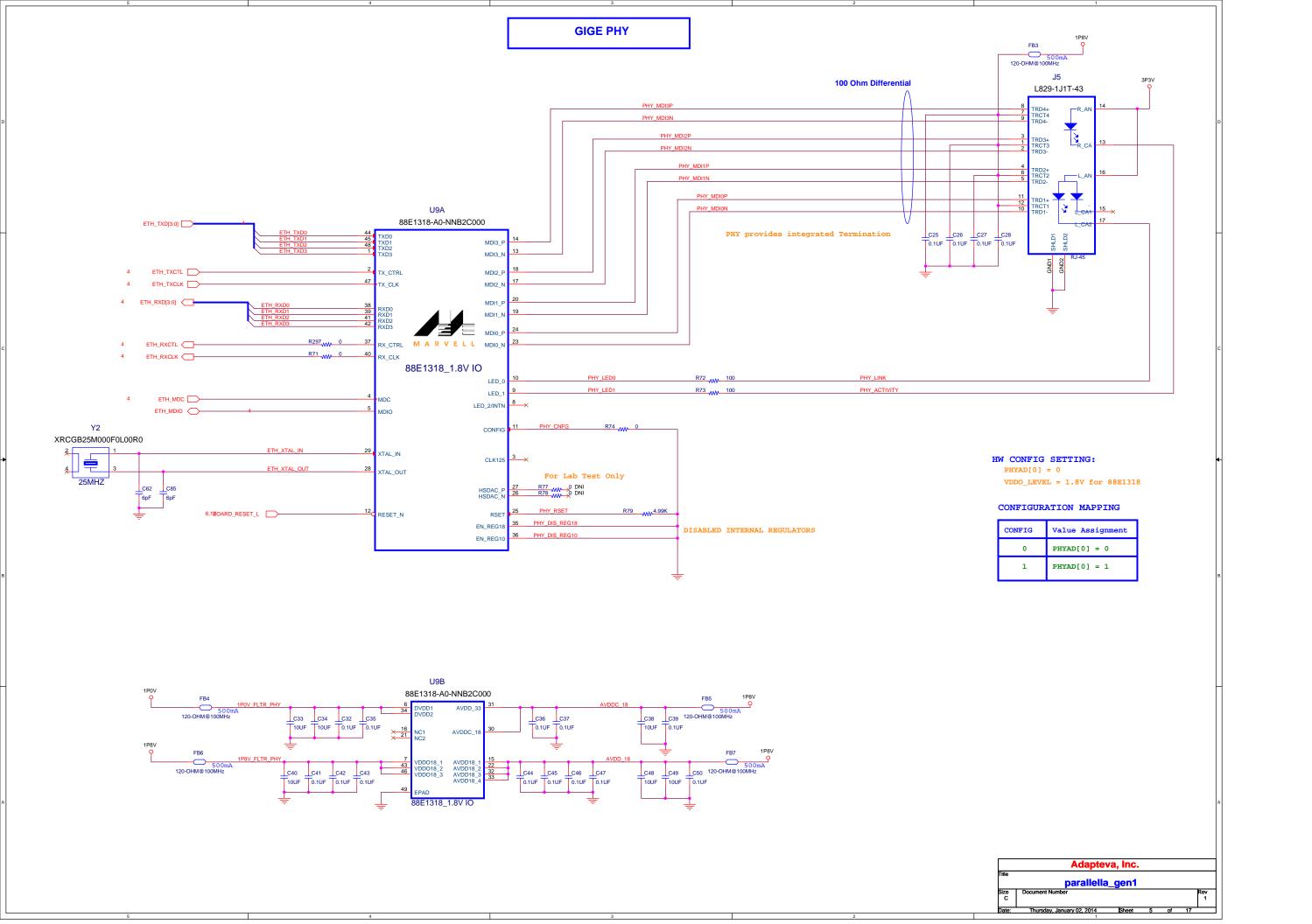
PROGRAMMABLE CLOCK GENERATOR

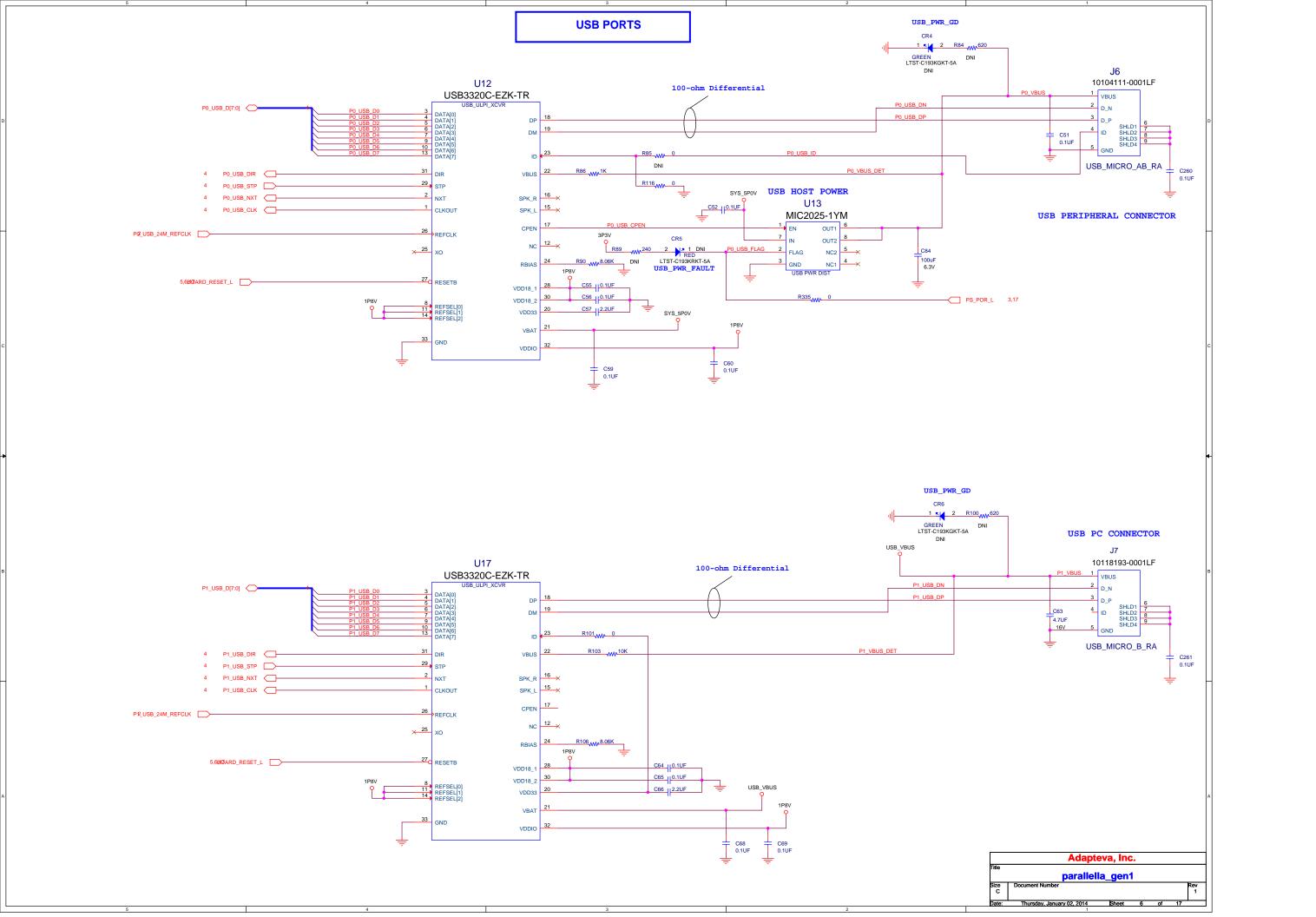


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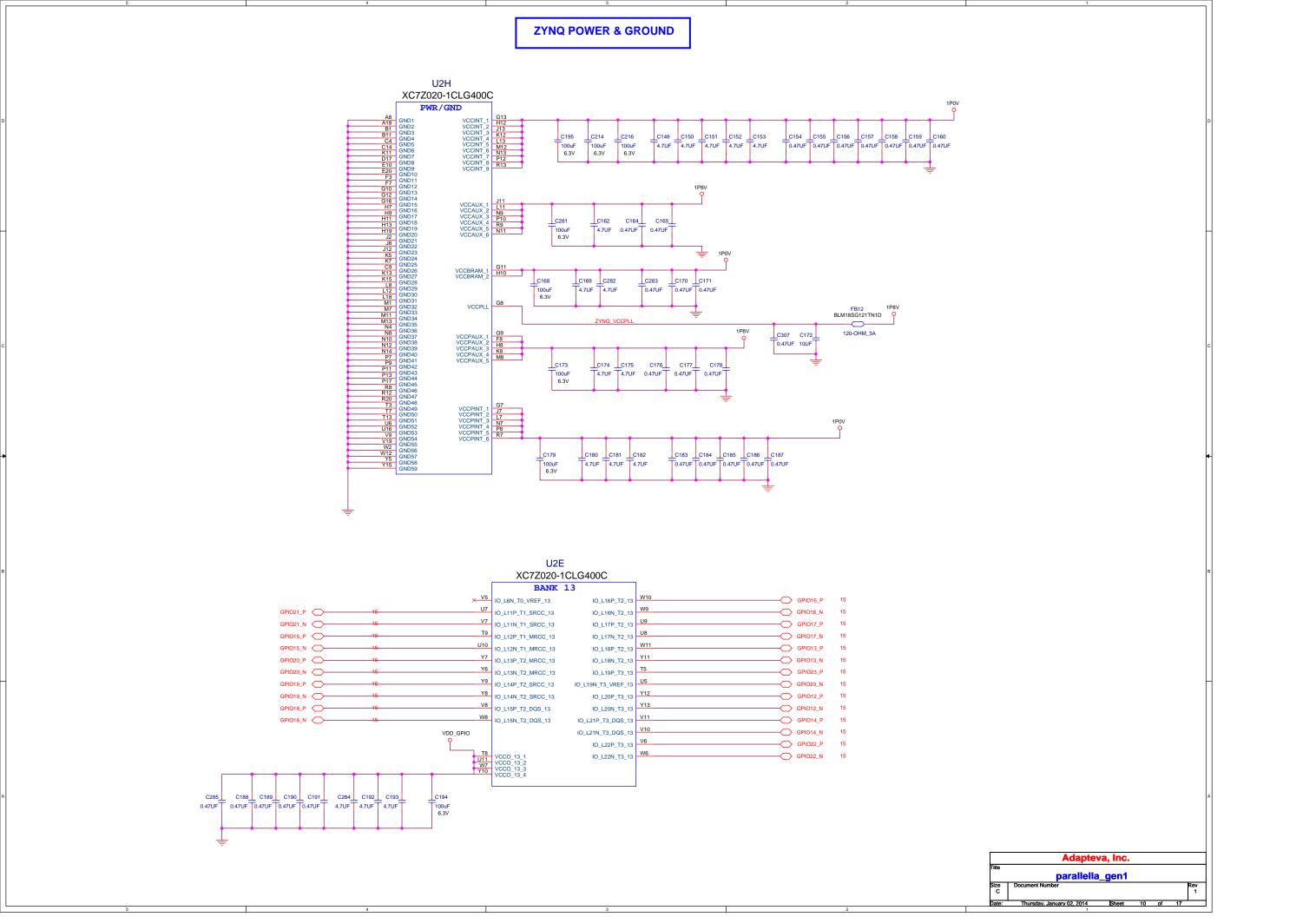


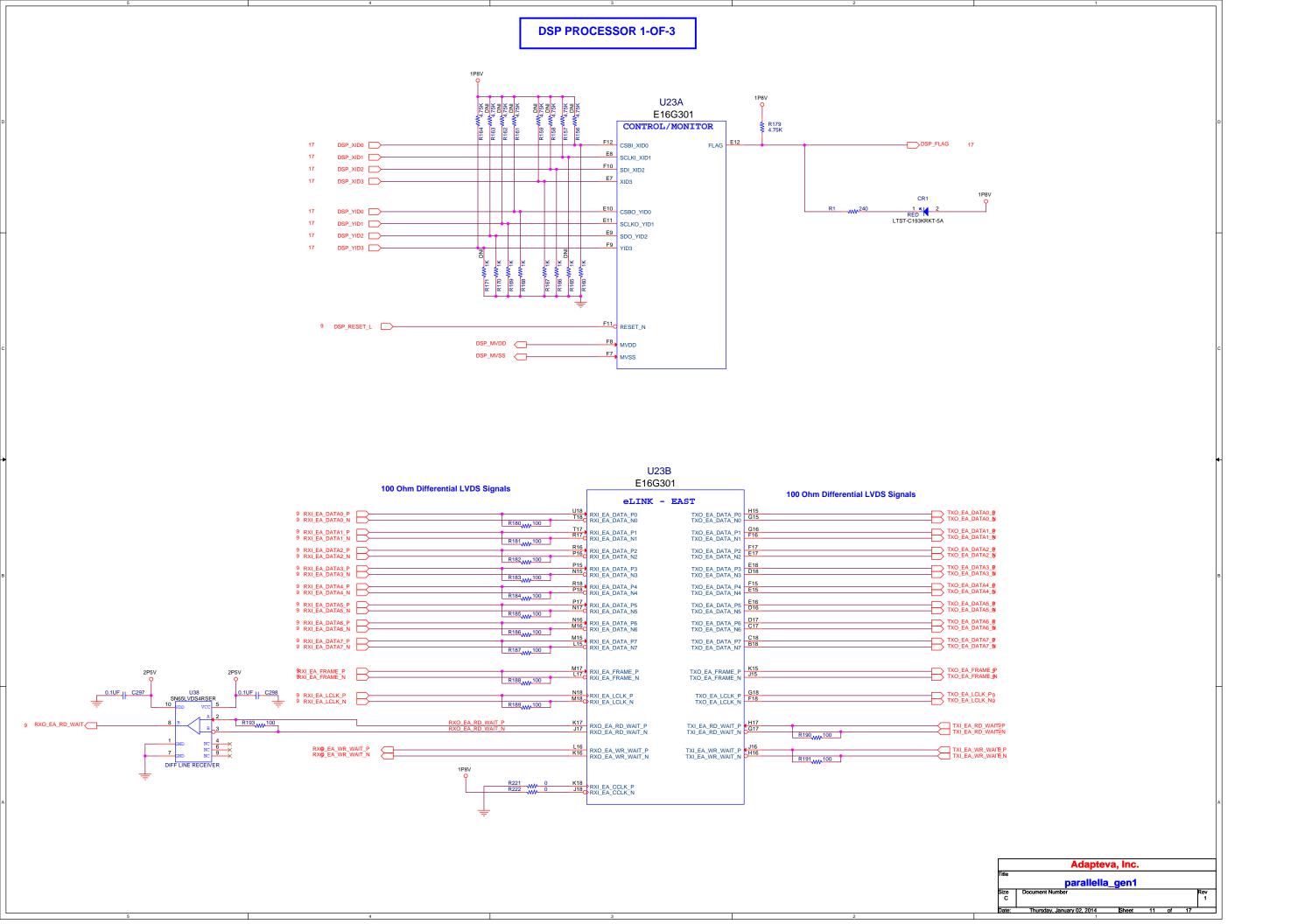
ZYNQ BANK 502 U2D XC7Z020-1CLG400C DDR_A[14:0] 8 DDR_DQ[31:0] BANK 502 DDR_ODT DDR_CS_L PS_DDR_WE_B M5 DDR3 WE L R322 WW 33 DDR_WE_L DDR_CAS_L 8 PS_DDR_RAS_B P4 DDR3_RAS_L R324 WM 33 DDR_RAS_L 8 W5 PS_DDR_DQS_P3 PS_DDR_DQS_N3 R2 PS_DDR_DQS_P2 PS_DDR_DQS_N2 G2 F2 PS_DDR_DQS_P1 PS_DDR_DQS_N1 PS_DDR_DM3 PS_DDR_DM2 PS_DDR_DM1 PS_DDR_DM0 C2 PS_DDR_DQS_P0 PS_DDR_DQS_N0 8 DDR_DQS_P0 DDR_DQS_N0 PS_DDR_DRST_B B4 DDR_RST_L 8 R111_{MM}4.75K 1P35V 1P35V C72 C73 C74 C75 C76 C77 C78 C79 C80 C81

4.7UF 4.7UF 0.47UF 0.47UF 0.47UF 0.47UF 0.47UF 0.47UF 0.47UF C70 C71 100uF 6.3V 6.3V PS_DDR_VRN PS_DDR_VRP G5 H5 PS_DDR_VREF0 P6
PS_DDR_VREF1 C82 C83 R67 1K Adapteva, Inc. parallella_gen1 Thursday, January 02, 2014 Sheet

DDR3 - 256M X 32 DDR_DQ[31:0] U20 MT41K256M32SLD-125:E DDR_A[14:0] DQ0 A4 DQ1 C2 DQ2 B4 DQ3 E2 DQ4 E4 DQ5 F2 DQ6 F4 DQ16 DQ17 DQ18 DQ19 DQ19 DQ20 DQ21 DQ22 DQ23 DDR3_256MX32 H3 ODT DDR_ODT ___ H4_{CS_L} DDR_CS_L G4 RAS_L DDR_RAS_L DQ24 M4 DQ25 N2 DQ26 N4 DQ27 R2 DQ28 T2 DQ30 DQ31 U4 G3_C CAS_L DDR_CAS_L DDR_WE_L 1P35V P10 DQS2 DQS2_L _____C95 _____C96 _____0.1UF VREFDQ J1 P3 DQS3 DQS3_L 1P35V C97 4.7UF VDD1 A12 VDD2 G1 VDD3 G12 VDD4 L1 VDD5 L12 VDD6 U1 VDD7 VDD8 C98 4.7UF C99 4.7UF C100 0.47UF VDD8 81
VDD01 812
VDD02 812
VDD03 612
VDD04 D2
VDD06 D31
VDD06 E30
VDD07 E10
VDD011 M3
VDD011 M3
VDD011 M10
VDD012 N3
VDD014 P11
VDD014 P11
VDD016 E30
VDD017 R12
VDD017 R12
VDD018 T1
VDD018 T1
VDD018 T1
VDD018 T1
VDD019 T1 C101 0.47UF C102 0.47UF C103 0.47UF DDR_RST_L RESET_L C104 0.047UF C105 0.047UF C106 0.047UF C107 0.047UF C108 0.047UF C109 0.047UF C110 0.047UF C111 0.047UF C112 0.047UF VSSQ1 VSSQ1 VSSQ1 VSSQ2 VSSQ3 VSSQ3 VSSQ3 VSSQ1 C113 0.047UF Adapteva, Inc. parallella_gen1

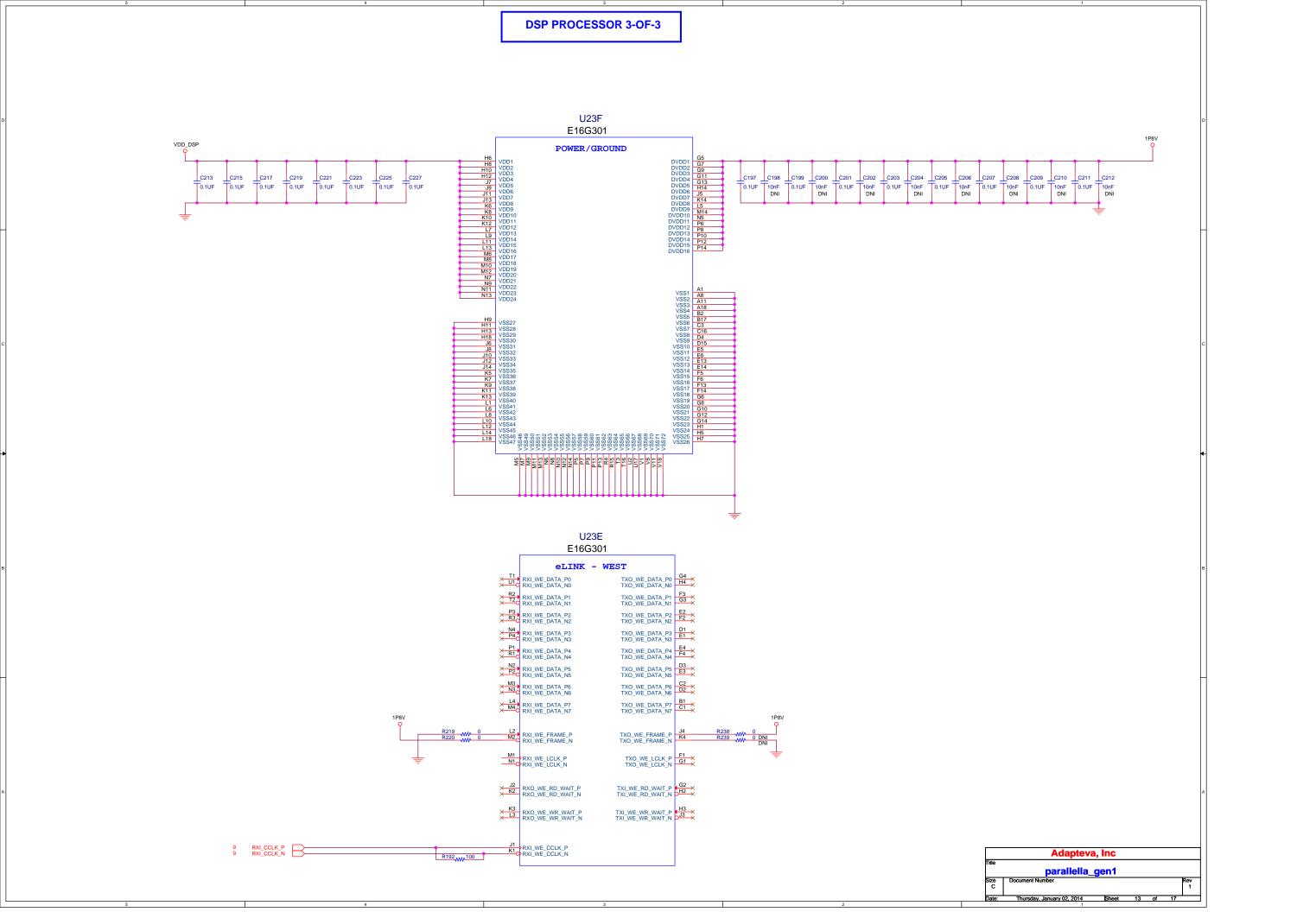
BANKS 34 & 35 Enable 100-ohm internal termination on all LVDS inputs HDMI_D[23:8] U2F U2G XC7Z020-1CLG400C XC7Z020-1CLG400C BANK 34 VDD_GPIO BANK 35 R19 IO_0_34 R20 _{WM} 4.75K IO 25 34 IO_25_34 J15 IO_L13P_T2_MRCC_34 N18 GPIO11_P IO_L1P_T0_34 PS_I2C_SCL 11 RXI_EA_DATA1_P RXI_CCLK_P 13 IO_L13N_T2_MRCC_34 P19 GPIO11_N IO_L1N_T0_34 11 RXI_EA_DATA1_N ____ RXI_CCLK_N 13 T12 IO_L2P_T0_34 GPIO10_P PROG_IO 11 RXI_EA_DATA0_P RXO_EA_WR_WAIT_P U12 IO_L2N_T0_34 GPIO10_N — 11 RXI_EA_DATA0_N RXO_EA_WR_WAIT_N IO_L3P_T0_DQS_PUDC_B_34 IO_L15P_T2_DQS_34 11 RXI_EA_DATA4_P RXI_EA_DATA5_P11 IO_L3N_T0_DQS_34 IO_L15N_T2_DQS_34 11 RXI_EA_DATA4_N IO_L3N_T0_DQS_AD1N<u>I</u>05L15N_T2_DQS_AD12N_35 RXI_EA_DATA5_N₁₁ V12 IO_L4P_T0_34 GPIO9_P — IO L16P T2 34 D19 IO_L4P_T0_35 IO_L16P_T2_35 G17 RXI_EA_DATA6_P11 11 RXI_EA_DATA2_P W13 IO_L4N_T0_34 GPIO9_N — IO_L16N_T2_34 11 RXI_EA_DATA2_N IO_L16N_T2_35 G18 IO_L4N_T0_35 T14 IO_L5P_T0_34 GPIO5_P — IO_L17P_T2_34 11 RXI_EA_DATA3_P IO_L5P_T0_AD9P_35 IO_L17P_T2_AD5P_35 J20 TXO_EA_FRAME_1P T15 IO_L5N_T0_34 IO_L17N_T2_34 IO_L17N_T2_AD5N_35 H20 IO L5N T0 AD9N 35 TXO_EA_FRAME_1\(\frac{1}{2}\) P14 IO_L6P_T0_34 15 11 RXI_EA_LCLK_P GPIO4_P — IO_L18P_T2_34 GPIO1_P IO_L18P_T2_AD13P_35 G19 RXI_EA_DATA7_P11 IO L6P T0 35 R14 IO_L6N_T0_VREF_34 IO_L18N_T2_34 W16 GPIO1_N 11 RXI_EA_LCLK_N ____ RXI_EA_DATA7_N₁₁ IO_L18N_T2_AD13N_35 G20 IO_L6N_T0_VREF_35 Y16 IO_L7P_T1_34 IO_L19P_T3_34 R16 SPDIF ___ TURBO_MODE 16,17 M19 IO_L7P_T1_AD2P_35 IO_L19P_T3_35 H15 RXI_EA_FRAME_19 Y17 IO_L7N_T1_34 HDMI_DE ___ HDMI_CLK 15 M20 IO_L7N_T1_AD2N_35 RXI_EA_FRAME_N W14 IO_L8P_T1_34 HDMI_HSYNC 15 GPIO7_P — TXI_EA_RD_WAIT1_P Y14 IO_L8N_T1_34 GPIO7_N — GPIO0_P — HDMI_VSYNC 15 L19 IO_L9P_T1_DQS_AD3P_I66_L21P_T3_DQS_AD14P_35 N15 IO_L21N_T3_DQS_34 V18 HDMI_D10 11 TXO_EA_DATA4_P U17 | IO_L9N_T1_DQS_34 GPIO0_N — L20 IO_L9N_T1_DQS_AD3N<u>I</u>95L21N_T3_DQS_AD14N_35 N16 11TXO_EA_DATA4_N IO_L22P_T3_34 W18 HDMI_D9 V15 IO_L10P_T1_34 VDD_GPIO IO_L22P_T3_AD7P_35 11 TXO_EA_DATAO_P W15 IO_L10N_T1_34 IO_L22N_T3_34 W19 R18 4.75K IO_L22N_T3_AD7N_35 11TXO_EA_DATAO_N TXO_EA_DATA1_1N U14 IO_L11P_T1_SRCC_34 GPIO6_P — IO_L23P_T3_34 IO_L23P_T3_35 M14 TXO_EA_DATA3_P1 11 TXO EA DATA2 P U15 IO_L11N_T1_SRCC_34 IO_L23N_T3_34 P18 GPIO6_N — L17 IO_L11N_T1_SRCC_35 IO_L23N_T3_35 M15 11TXO_EA_DATA2_N TXO_EA_DATA3_N1 U18 IO_L12P_T1_MRCC_34 GPIO3_P — IO_L24P_T3_34 K17 IO_L12P_T1_MRCC_35 IO_L24P_T3_AD15P_35 K16 11 TXO_EA_LCLK_P ____ U19 IO_L12N_T1_MRCC_34 IO_L24N_T3_34 P16 GPIO2_N K18 | IO_L12N_T1_MRCC_35 | IO_L24N_T3_AD15N_35 | J16 11 TXO_EA_LCLK_N ____ VDD_GPIO C126 C127 C128 C129 C130 C131 C132 C133 C135 C136 C137 C138 C139 C140 C141 C142 0.47UF 0.47UF 0.47UF 4.7UF 4.7UF 4.7UF 4.7UF 0.47UF 0.47UF 0.47UF 0.47UF 4.7UF 4.7UF 4.7UF 4.7UF 100uF 6.3V Adapteva, Inc. parallella_gen1



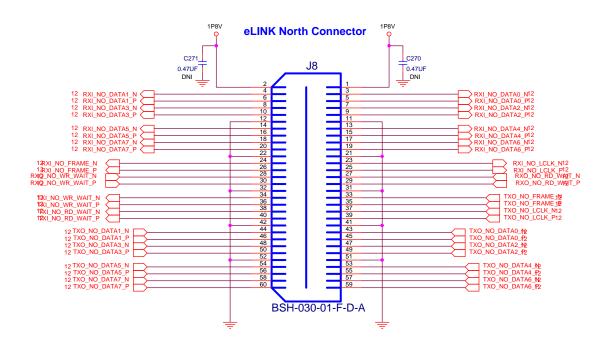


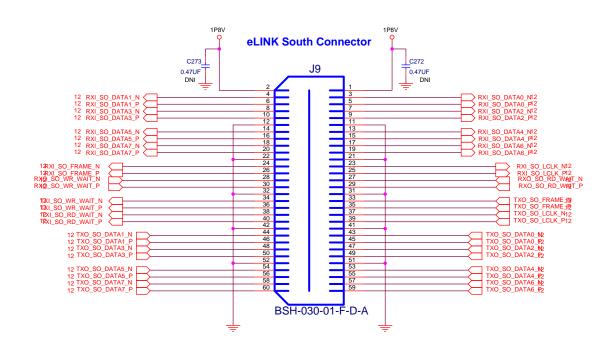
DSP PROCESSOR 2-OF-3 U23C E16G301 100 Ohm Differential LVDS Signals 100 Ohm Differential LVDS Signals eLINK - NORTH 14 RXI_NO_DATA0_P 14 RXI_NO_DATA0_N RXI_NO_DATA_P0 RXI_NO_DATA_N0 TXO_NO_DATA_P0 D12 D11 TXO_NO_DATA_N0 TXO_NO_DATA0_P4
TXO_NO_DATA0_N4 R233_{WW} 100 DNI R194_{MM}100 TXO_NO_DATA_P1 C13
TXO_NO_DATA_N1 TXO_NO_DATA1_f24
TXO_NO_DATA1_f14 R232_{WW} 100 DNI R195_{MM}100 TXO_NO_DATA_P2 B13
TXO_NO_DATA_N2 TXO_NO_DATA2_P4
TXO_NO_DATA2_N4 C5 RXI_NO_DATA_P2 RXI_NO_DATA_N2 R231_{WW} 100 DNI R196_{MM}100 TXO_NO_DATA3_F4
TXO_NO_DATA3_N4 R197_{WW}100 R230_{MM}100 DNI TXO_NO_DATA_P4 D13
TXO_NO_DATA_N4 TXO_NO_DATA4_P4
TXO_NO_DATA4_N4 14 RXI_NO_DATA4_P 14 RXI_NO_DATA4_N R198_{MM}100 R229_{WW} 100 DNI TXO_NO_DATA_P5
TXO_NO_DATA_N5

C15
C14 TXO_NO_DATA5_P4
TXO_NO_DATA5_N4 14 RXI_NO_DATA5_P 14 RXI_NO_DATA5_N R199_{WM}100 R228_{WW}100 DNI TXO_NO_DATA_P6 B16
TXO_NO_DATA_N6 TXO_NO_DATA6_P4
TXO_NO_DATA6_N4 C7 C6 RXI_NO_DATA_P6 RXI_NO_DATA_N6 14 RXI_NO_DATA6_P 14 RXI_NO_DATA6_N R227_{WW} 100 DNI R200_{MM}100 TXO_NO_DATA_P7
TXO_NO_DATA_N7 D8 D7 RXI_NO_DATA_P7 RXI_NO_DATA_N7 14 RXI_NO_DATA7_P 14 RXI_NO_DATA7_N R226_{WW} 100 DNI R201 4444 100 R243 WW 10K TEXI_NO_FRAME_P
TEXI_NO_FRAME_N TXO_NO_FRAME_P D9
TXO_NO_FRAME_N TXO_NO_FRAME_114
TXO_NO_FRAME_114 R202 1P8VO R242 WW 10K TXO_NO_LCLK_P14
TXO_NO_LCLK_N14 R203_{AAA}100 R206_{WM} 100 R241 _____10K R204_{WW}100 R240 WW 10K R205_{WM}100 U23D E16G301 100 Ohm Differential LVDS Signals 100 Ohm Differential LVDS Signals eLINK - SOUTH TXO_SO_DATA0_P4
TXO_SO_DATA0_N4 R207_{MM}100 RXI_SO_DATA_P1 RXI_SO_DATA_N1 TXO_SO_DATA_P1 T13
TXO_SO_DATA_N1 TXO_SO_DATA1_P4
TXO_SO_DATA1_N4 14 RXI_SO_DATA1_P 14 RXI_SO_DATA1_N R208_{MM}100 TXO_SO_DATA2_P4
TXO_SO_DATA2_N4 RXI_SO_DATA_P2 RXI_SO_DATA_N2 TXO_SO_DATA_P2
TXO_SO_DATA_N2
U13
U14 14 RXI_SO_DATA2_P 14 RXI_SO_DATA2_N R209_{MM}100 TXO_SO_DATA_P3 V15
TXO_SO_DATA_N3 TXO_SO_DATA3_P4
TXO_SO_DATA3_N4 RXI_SO_DATA_P3 RXI_SO_DATA_N3 14 RXI_SO_DATA3_P 14 RXI_SO_DATA3_N R210_{MM}100 TXO_SO_DATA_P4
TXO_SO_DATA_N4
R13
R14 RXI_SO_DATA_P4
RXI_SO_DATA_N4 14 RXI_SO_DATA4_P 14 RXI_SO_DATA4_N R211_{WW}100 TXO_SO_DATA_P5 TXO_SO_DATA_N5 TXO_SO_DATA5_fP4
TXO_SO_DATA5_fN4 14 RXI_SO_DATA5_P 14 RXI_SO_DATA5_N RXI_SO_DATA_P5
RXI_SO_DATA_N5 R212_{WW}100 TXO_SO_DATA6_P4
TXO_SO_DATA6_N4 14 RXI_SO_DATA6_P 14 RXI_SO_DATA6_N T6 T7 RXI_SO_DATA_P6 RXI_SO_DATA_N6 TXO_SO_DATA_P6
TXO_SO_DATA_N6
U15
U16 R213_{MM}100 RXI_SO_DATA_P7 RXI_SO_DATA_N7 TXO_SO_DATA_P7 V16
TXO_SO_DATA_N7 14 RXI_SO_DATA7_P 14 RXI_SO_DATA7_N TXO_SO_DATA7_P4
TXO_SO_DATA7_N4 R214_{MM}100 R246 WW 10K TXO_SO_FRAME_P TXO_SO_FRAME_N R236_WM_100 TRIXI_SO_FRAME_P
TRIXI_SO_FRAME_N R215_{WW}100 1P8VO R247 WW 10K R244 WW 10K O1P8V TXO_SO_LCLK_P14
TXO_SO_LCLK_N14 R216_{WW}100 U9 RXO_SO_RD_WAIT_P RXO_SO_RD_WAIT_N TXI_SO_RD_WAIT_P
TXI_SO_RD_WAIT_N TXI_SO_RD_WAIT!4N R234_{WW} 100 DNI R217_{AAAA}100 RXQ4SO_WR_WAIT_P RXQ4SO_WR_WAIT_N TXI_SO_WR_WAITI4P RXO_SO_WR_WAIT_P RXO_SO_WR_WAIT_N R235_{MM}100 R218_{MM}100 Adapteva, Inc. parallella_gen1 v. January 02, 2014



DSP eLINK CONNECTORS





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