Zynq MicroZed	
Avnet Engineering Services	
www.microzed.org	
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MicroZed_Production

12 Dec 2014

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Title: 01 - Avnet Lead Sheet_B.SchDoc		
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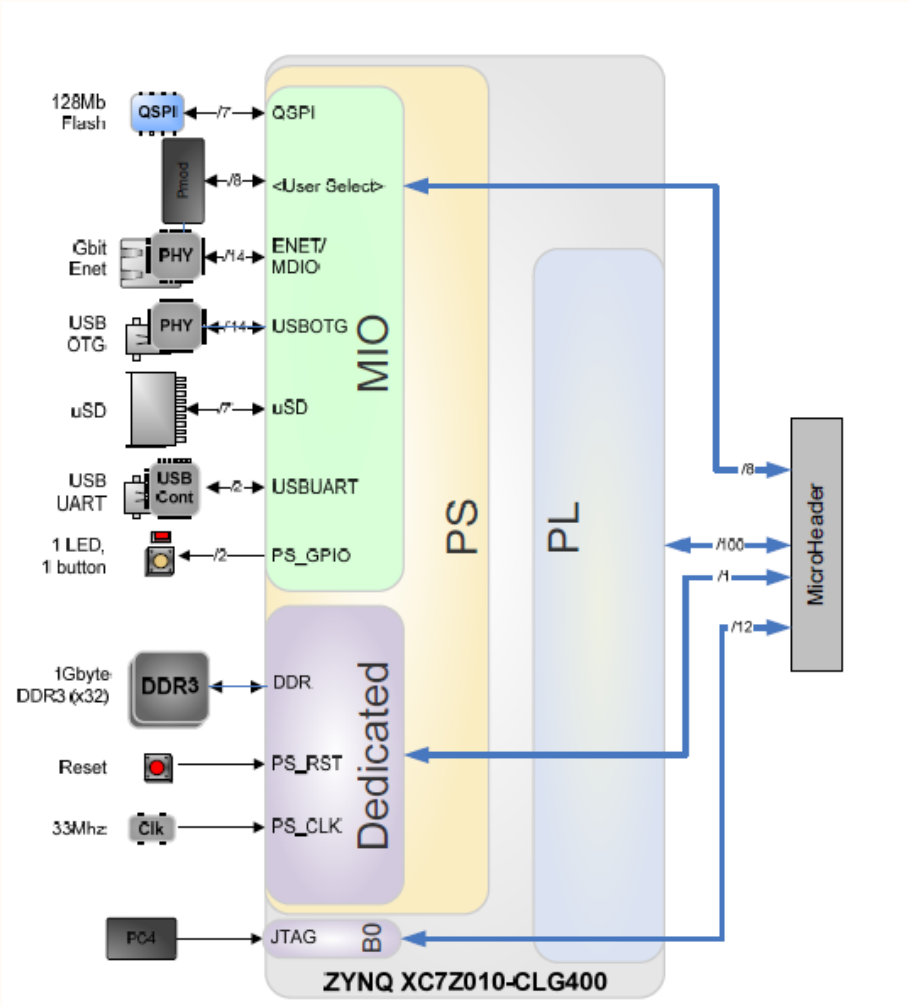

AVNET Avnet Engineering Services		
Title: 02 - Block Diagram.SchDoc		
Size: B	Document Number: MicroZed 7010	Rev: F-06
Date: 12/10/2014	Sheet 2 of 11	

U9G
Zynq 7010/7020 SOC CLG400

BANK 502

PS_DDR_DQ0_502 C3 — DDR3_DQ0
PS_DDR_DQ1_502 B3 — DDR3_DQ1
PS_DDR_DQ2_502 A4 — DDR3_DQ2
PS_DDR_DQ3_502 B4 — DDR3_DQ3
PS_DDR_DQ4_502 C1 — DDR3_DQ4
PS_DDR_DQ5_502 D1 — DDR3_DQ5
PS_DDR_DQ6_502 E1 — DDR3_DQ6
PS_DDR_DQ7_502 F1 — DDR3_DQ7
PS_DDR_DQ8_502 F3 — DDR3_DQ8
PS_DDR_DQ9_502 G3 — DDR3_DQ9
PS_DDR_DQ10_502 G1 — DDR3_DQ10
PS_DDR_DQ11_502 H1 — DDR3_DQ11
PS_DDR_DQ12_502 H2 — DDR3_DQ12
PS_DDR_DQ13_502 J2 — DDR3_DQ13
PS_DDR_DQ14_502 J1 — DDR3_DQ14
PS_DDR_DQ15_502 K1 — DDR3_DQ15
PS_DDR_DQ16_502 P3 — DDR3_DQ16
PS_DDR_DQ17_502 P1 — DDR3_DQ17
PS_DDR_DQ18_502 N1 — DDR3_DQ18
PS_DDR_DQ19_502 M1 — DDR3_DQ19
PS_DDR_DQ20_502 L1 — DDR3_DQ20
PS_DDR_DQ21_502 L3 — DDR3_DQ21
PS_DDR_DQ22_502 K3 — DDR3_DQ22
PS_DDR_DQ23_502 K2 — DDR3_DQ23
PS_DDR_DQ24_502 J4 — DDR3_DQ24
PS_DDR_DQ25_502 J3 — DDR3_DQ25
PS_DDR_DQ26_502 H4 — DDR3_DQ26
PS_DDR_DQ27_502 H3 — DDR3_DQ27
PS_DDR_DQ28_502 G4 — DDR3_DQ28
PS_DDR_DQ29_502 G3 — DDR3_DQ29
PS_DDR_DQ30_502 F4 — DDR3_DQ30
PS_DDR_DQ31_502 E4 — DDR3_DQ31

DDR_D_BL0 — DDR3_DQ[7..0]
DDR_D_BL1 — DDR3_DQ[15..8]
DDR_D_BL2 — DDR3_DQ[23..16]
DDR_D_BL3 — DDR3_DQ[31..24]

DDR_D

PS_DDR_A0_502 N2 — DDR3_A0_3
PS_DDR_A1_502 K2 — DDR3_A1_3
PS_DDR_A2_502 M3 — DDR3_A2_3
PS_DDR_A3_502 K3 — DDR3_A3_3
PS_DDR_A4_502 M4 — DDR3_A4_3
PS_DDR_A5_502 L1 — DDR3_A5_3
PS_DDR_A6_502 L4 — DDR3_A6_3
PS_DDR_A7_502 K4 — DDR3_A7_3
PS_DDR_A8_502 K1 — DDR3_A8_3
PS_DDR_A9_502 J4 — DDR3_A9_3
PS_DDR_A10_502 F5 — DDR3_A10_3
PS_DDR_A11_502 G4 — DDR3_A11_3
PS_DDR_A12_502 E4 — DDR3_A12_3
PS_DDR_A13_502 D4 — DDR3_A13_3
PS_DDR_A14_502 F4 — DDR3_A14_3

DDR_AC

PS_DDR_DQS_P0_502 C2 — DDR3_DQS0_3_P
PS_DDR_DQS_N0_502 B2 — DDR3_DQS0_3_N
PS_DDR_DQS_P1_502 G2 — DDR3_DQS1_3_P
PS_DDR_DQS_N1_502 F2 — DDR3_DQS1_3_N
PS_DDR_DQS_P2_502 R2 — DDR3_DQS2_3_P
PS_DDR_DQS_N2_502 T2 — DDR3_DQS2_3_N
PS_DDR_DQS_P3_502 W5 — DDR3_DQS3_3_P
PS_DDR_DQS_N3_502 W4 — DDR3_DQS3_3_N

PS_DDR_CKP_502 L2 — DDR3_CK0_3_P
PS_DDR_CKN_502 M2 — DDR3_CK0_3_N

PS_DDR_BA0_502 L5 — DDR3_BA0_3
PS_DDR_BA1_502 R4 — DDR3_BA1_3
PS_DDR_BA2_502 J5 — DDR3_BA2_3

PS_DDR_DM0_502 A1 — DDR3_DM0_3
PS_DDR_DM1_502 F1 — DDR3_DM1_3
PS_DDR_DM2_502 T1 — DDR3_DM2_3
PS_DDR_DM3_502 Y1 — DDR3_DM3_3

DDR_DM

PS_DDR_CS_B_502 N1 — DDR3_CS#_3
PS_DDR_WE_B_502 M5 — DDR3_WE#_3
PS_DDR_CAS_B_502 P5 — DDR3_CAS#_3
PS_DDR_RAS_B_502 P4 — DDR3_RAS#_3
PS_DDR_CKE_502 N3 — DDR3_CKE_3
PS_DDR_ODT_502 N5 — DDR3_ODT_3

PS_DDR_DRST_B_502 B4 — DDR3_RESET#_3

PS_DDR_VRP_502 H5 — R74 80.6 — GND
PS_DDR_VRN_502 G5 — R75 80.6 — 1.5V

Layout Note:
DDR3 trace lengths must include Zynq package flight times. See UG933 and Layout Guidelines.

Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms

1.5V
C41 47uF, C170 0.1uF, C176 0.1uF, C181 0.1uF, C188 0.1uF
C193 0.01uF, C196 0.01uF, C200 0.01uF, C203 0.01uF
DDR_PWR
C43 47uF, C199 0.1uF, C194 0.1uF, C186 0.1uF, C184 0.1uF
C180 0.01uF, C178 0.01uF, C172 0.01uF, C174 0.01uF
GND
VTTREF
C187 0.01uF

U11
MT41K256M16HA-125:E

DDR3_A0_3 N3 — A0
DDR3_A1_3 P7 — A1
DDR3_A2_3 P3 — A2
DDR3_A3_3 N2 — A3
DDR3_A4_3 P8 — A4
DDR3_A5_3 P2 — A5
DDR3_A6_3 R8 — A6
DDR3_A7_3 R2 — A7
DDR3_A8_3 T8 — A8
DDR3_A9_3 R3 — A9
DDR3_A10_3 L7 — A10/AP
DDR3_A11_3 R7 — A11
DDR3_A12_3 N7 — A12/BC#
DDR3_A13_3 T3 — A13
DDR3_A14_3 T7 — A14

DDR3_BA0_3 M2 — BA0
DDR3_BA1_3 N8 — BA1
DDR3_BA2_3 M3 — BA2

DDR3_CS#_3 L2 — CS#
DDR3_WE#_3 L3 — WE#
DDR3_CAS#_3 K3 — CAS#
DDR3_RAS#_3 J3 — RAS#

DDR3_CKE_3 K9 — CKE
DDR3_CK0_3_P J7 — CK
DDR3_CK0_3_N K7 — CK#

DDR3_RESET#_3 T2 — RESET#

ODT — DDR3_ODT_3
ZQ — L8 — R79 240 — GND

DQ0 DDR3_DQ0, DQ1 DDR3_DQ1, DQ2 DDR3_DQ2, DQ3 DDR3_DQ3, DQ4 DDR3_DQ4, DQ5 DDR3_DQ5, DQ6 DDR3_DQ6, DQ7 DDR3_DQ7, DQ8 DDR3_DQ8, DQ9 DDR3_DQ9, DQ10 DDR3_DQ10, DQ11 DDR3_DQ11, DQ12 DDR3_DQ12, DQ13 DDR3_DQ13, DQ14 DDR3_DQ14, DQ15 DDR3_DQ15

UDM DDR3_DM1_3, LDM DDR3_DM0_3
UDQS DDR3_DQS1_3_P, DDR3_DQS1_3_N
LDQS DDR3_DQS0_3_P, DDR3_DQS0_3_N

U12
MT41K256M16HA-125:E

DDR3_A0_3 N3 — A0
DDR3_A1_3 P7 — A1
DDR3_A2_3 P3 — A2
DDR3_A3_3 N2 — A3
DDR3_A4_3 P8 — A4
DDR3_A5_3 P2 — A5
DDR3_A6_3 R8 — A6
DDR3_A7_3 R2 — A7
DDR3_A8_3 T8 — A8
DDR3_A9_3 R3 — A9
DDR3_A10_3 L7 — A10/AP
DDR3_A11_3 R7 — A11
DDR3_A12_3 N7 — A12/BC#
DDR3_A13_3 T3 — A13
DDR3_A14_3 T7 — A14

DDR3_BA0_3 M2 — BA0
DDR3_BA1_3 N8 — BA1
DDR3_BA2_3 M3 — BA2

DDR3_CS#_3 L2 — CS#
DDR3_WE#_3 L3 — WE#
DDR3_CAS#_3 K3 — CAS#
DDR3_RAS#_3 J3 — RAS#

DDR3_CKE_3 K9 — CKE
DDR3_CK0_3_P J7 — CK
DDR3_CK0_3_N K7 — CK#

DDR3_RESET#_3 T2 — RESET#

ODT — DDR3_ODT_3
ZQ — L8 — R85 240 — GND

DQ0 DDR3_DQ16, DQ1 DDR3_DQ17, DQ2 DDR3_DQ18, DQ3 DDR3_DQ19, DQ4 DDR3_DQ20, DQ5 DDR3_DQ21, DQ6 DDR3_DQ22, DQ7 DDR3_DQ23, DQ8 DDR3_DQ24, DQ9 DDR3_DQ25, DQ10 DDR3_DQ26, DQ11 DDR3_DQ27, DQ12 DDR3_DQ28, DQ13 DDR3_DQ29, DQ14 DDR3_DQ30, DQ15 DDR3_DQ31

UDM DDR3_DM3_3, LDM DDR3_DM2_3
UDQS DDR3_DQS3_3_P, DDR3_DQS3_3_N
LDQS DDR3_DQS2_3_P, DDR3_DQS2_3_N

Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.

DDR_T

DDR3_A14_3 — DDR3_T_A14_3 R29 40.2
DDR3_A13_3 — DDR3_T_A13_3 R27 40.2
DDR3_A12_3 — DDR3_T_A12_3 R80 40.2
DDR3_A11_3 — DDR3_T_A11_3 R84 40.2
DDR3_A10_3 — DDR3_T_A10_3 R76 40.2
DDR3_A9_3 — DDR3_T_A9_3 R24 40.2
DDR3_A8_3 — DDR3_T_A8_3 R31 40.2
DDR3_A7_3 — DDR3_T_A7_3 R30 40.2
DDR3_A6_3 — DDR3_T_A6_3 R86 40.2
DDR3_A5_3 — DDR3_T_A5_3 R28 40.2
DDR3_A4_3 — DDR3_T_A4_3 R83 40.2
DDR3_A3_3 — DDR3_T_A3_3 R26 40.2
DDR3_A2_3 — DDR3_T_A2_3 R23 40.2
DDR3_A1_3 — DDR3_T_A1_3 R88 40.2
DDR3_A0_3 — DDR3_T_A0_3 R21 40.2
DDR3_BA0_3 — DDR3_T_BA0_3 R25 40.2
DDR3_BA1_3 — DDR3_T_BA1_3 R81 40.2
DDR3_BA2_3 — DDR3_T_BA2_3 R22 40.2
DDR3_CS#_3 — DDR3_T_CS#_3 R18 40.2
DDR3_WE#_3 — DDR3_T_WE#_3 R20 40.2
DDR3_CAS#_3 — DDR3_T_CAS#_3 R19 40.2
DDR3_RAS#_3 — DDR3_T_RAS#_3 R17 40.2
DDR3_ODT_3 — DDR3_T_ODT_3 R16 40.2

DDR3_RESET#_3 — DDR3_T_RESET#_3
DDR3_CK0_3_P — DDR3_T_CK0_3_P — R77 80.6
DDR3_CK0_3_N — DDR3_T_CK0_3_N
DDR3_CKE_3 — DDR3_T_CKE_3 R15 40.2

DDR3_0V75

JT6: A — 4.7K — Com — B — GND

Default: Pins 2 - 3, 4.7K ohm resistor.

NOTE:
RESET# requires a 4.7K pull down resistor. Please refer to the latest Xilinx UG933 for further information.

DDR3 Termination Supply

3.3V
C205 0.1uF — GND
3.3V 1.5V
U13
VDD 10, VDDQSNS 1, VLDOIN 2, PGND 4, VTTREF 6, S3 7, S5 9, PAD, VTT 3, VTTSNS 5, GND 8
TPS51206
R33 10K, R32 10K
C55 10uF
C48 10uF
C49 0.22uF
DDR3_0V75
VTTREF
DDR_PWR
GND

DDR3_0V75
C47 100uF, C46 100uF, C39 4.7uF, C45 4.7uF, C185 0.1uF, C204 0.1uF, C37 0.01uF, C38 0.01uF
GND

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Title:	03 - DDR3.SchDoc
Size: C	Document Number: MicroZed 7010
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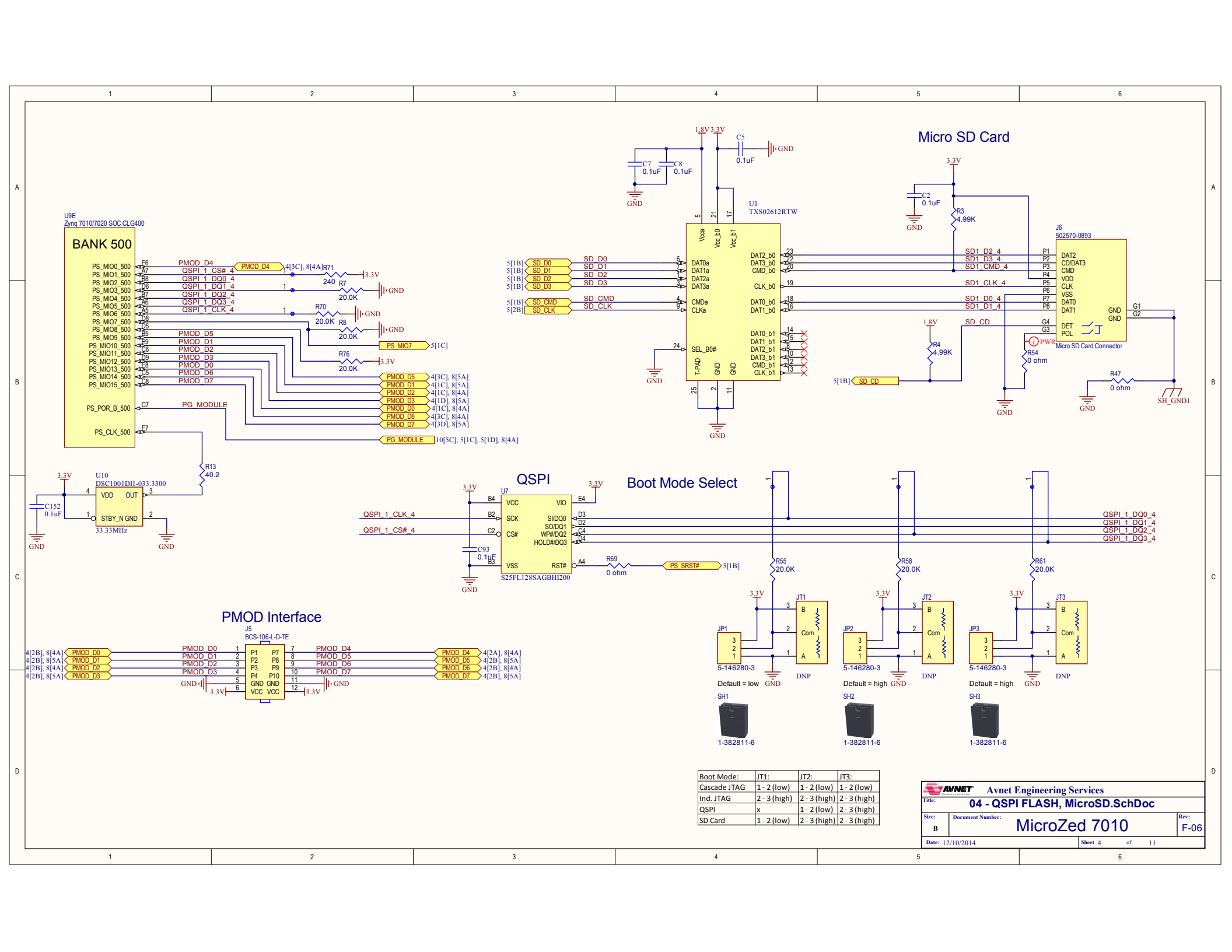

Boot Mode:	JT1:	JT2:	JT3:
Cascade JTAG	1 - 2 (low)	1 - 2 (low)	1 - 2 (low)
Ind. JTAG	2 - 3 (high)	2 - 3 (high)	2 - 3 (high)
QSPI	x	1 - 2 (low)	2 - 3 (high)
SD Card	1 - 2 (low)	2 - 3 (high)	2 - 3 (high)

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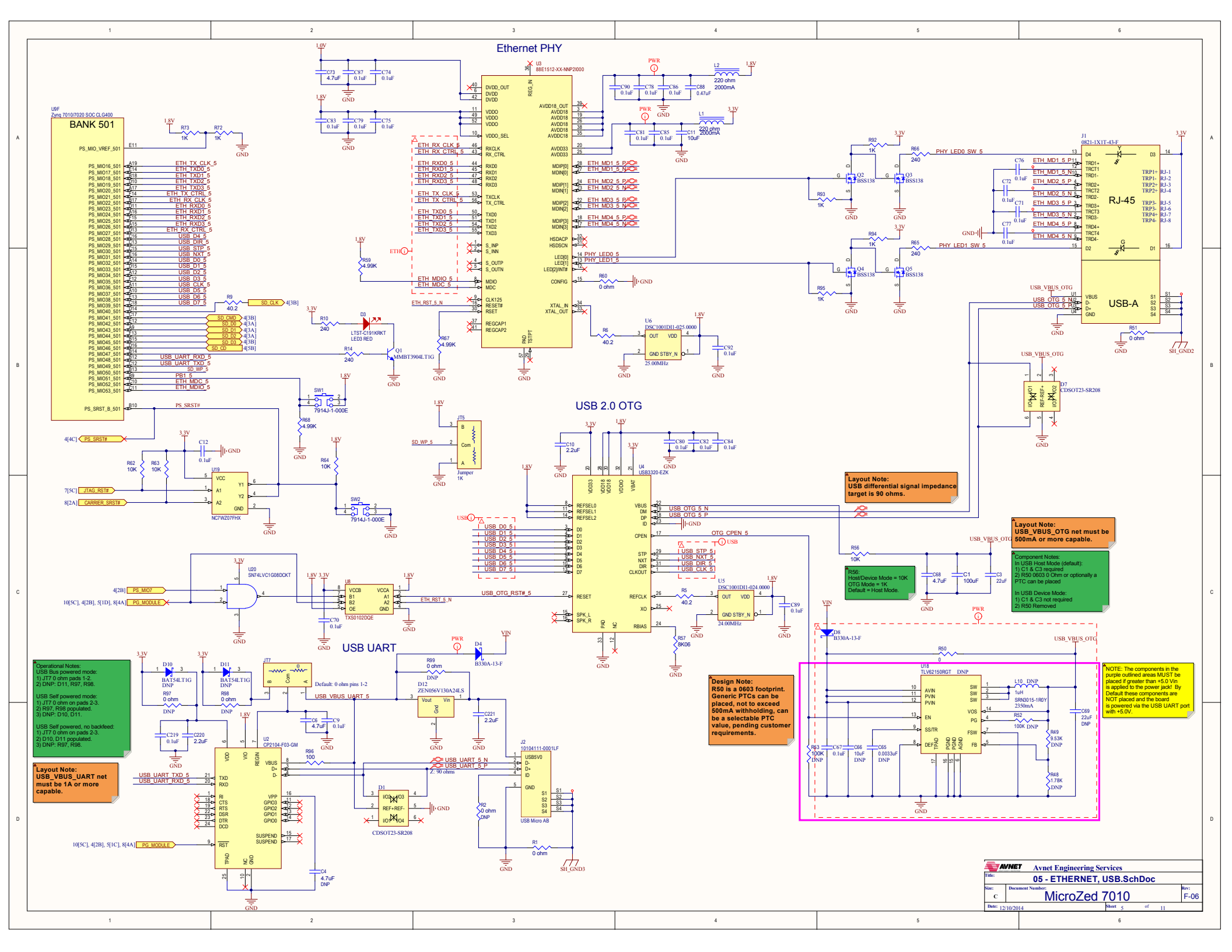
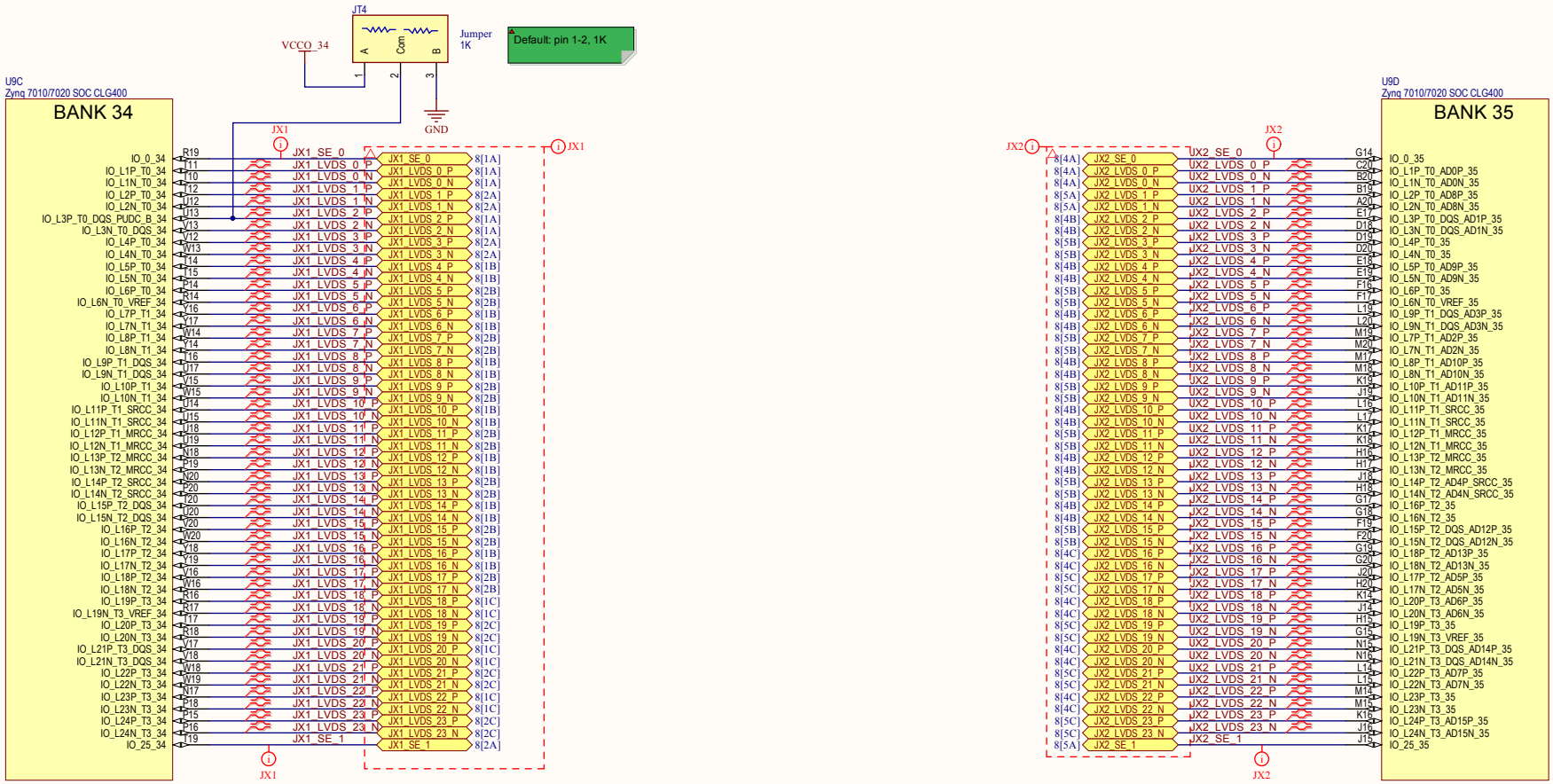
Size: B	Document Number: MicroZed 7010	Rev: F-06
Date: 12/10/2014	Sheet 4 of 11	


Ethernet PHY
BANK 501
U9F
Zynq 7010/7020 SOC CLG400
U3
88E1512-XX-NNP2I000
RJ-45
USB-A
J1
0821-1X1T-43-F
USB 2.0 OTG
U4
USB3320-EZK
USB UART
U2
CP2104-F03-GM
U8
TXS0102DQE
U19
NC7WZ07FHX
U20
SN74LVC1G08DCKT
U6
DSC1001DI1-025.0000
25.00MHz
U5
DSC1001DI1-024.0000
24.00MHz
U18
TLV62150RGT DNP
Q1
MMBT3904LT1G
Q2
BSS138
Q3
BSS138
Q4
BSS138
Q5
BSS138
D3
LTST-C191KRKT
LED3 RED
D7
CDSOT23-SR208
D1
CDSOT23-SR208
D8
B330A-13-F
D4
B330A-13-F
D10
BAT54LT1G
D11
BAT54LT1G
D12
ZEN056V130A24LS
SW1
7914J-1-000E
SW2
7914J-1-000E
JT5
Jumper
JT7
Default: 0 ohm pins 1-2
J2
10104111-0001LF
USB Micro AB
SH_GND2
SH_GND3
Layout Note:
USB differential signal impedance target is 90 ohms.
Layout Note:
USB_VBUS_OTG net must be 500mA or more capable.
Component Notes:
In USB Host Mode (default):
1) C1 & C3 required
2) R50 0603 0 Ohm or optionally a PTC can be placed
In USB Device Mode:
1) C1 & C3 not required
2) R50 Removed
R56:
Host/Device Mode = 10K
OTG Mode = 1K
Default = Host Mode.
Design Note:
R50 is a 0603 footprint. Generic PTCs can be placed, not to exceed 500mA withholding, can be a selectable PTC value, pending customer requirements.
NOTE: The components in the purple outlined areas MUST be placed if greater than +5.0 Vin is applied to the power jack! By Default these components are NOT placed and the board is powered via the USB UART port with +5.0V.
Operational Notes:
USB Bus powered mode:
1) JT7 0 ohm pads 1-2
2) DNP: D11, R97, R98.
USB Self powered mode:
1) JT7 0 ohm on pads 2-3.
2) R97, R98 populated.
3) DNP: D10, D11.
USB Self powered, no backfeed:
1) JT7 0 ohm on pads 2-3.
2) D10, D11 populated.
3) DNP: R97, R98.
Layout Note:
USB_VBUS_UART net must be 1A or more capable.
Avnet Engineering Services
05 - ETHERNET, USB.SchDoc
MicroZed 7010
F-06
12/10/2014
5
11



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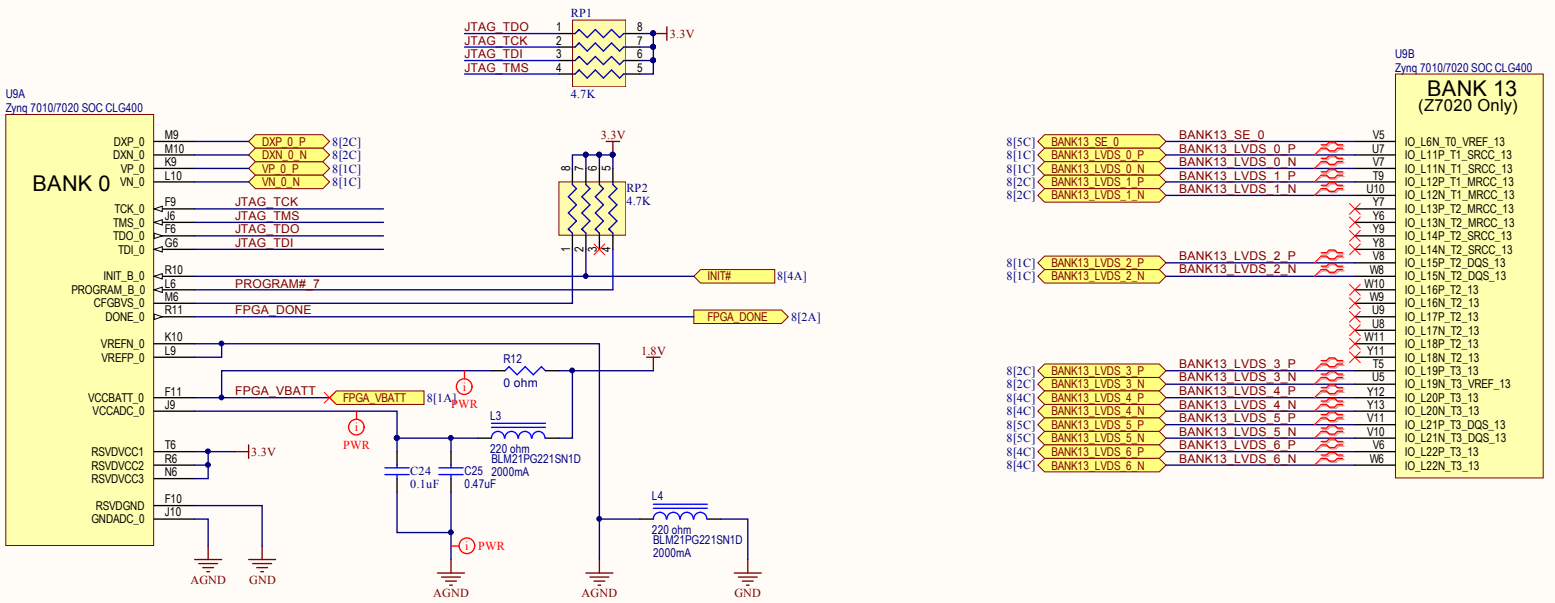
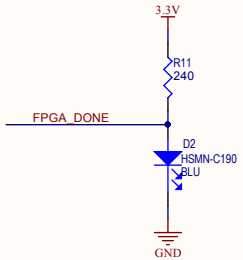
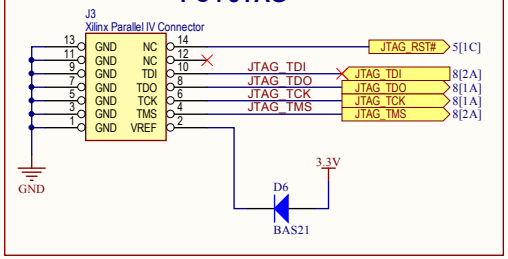


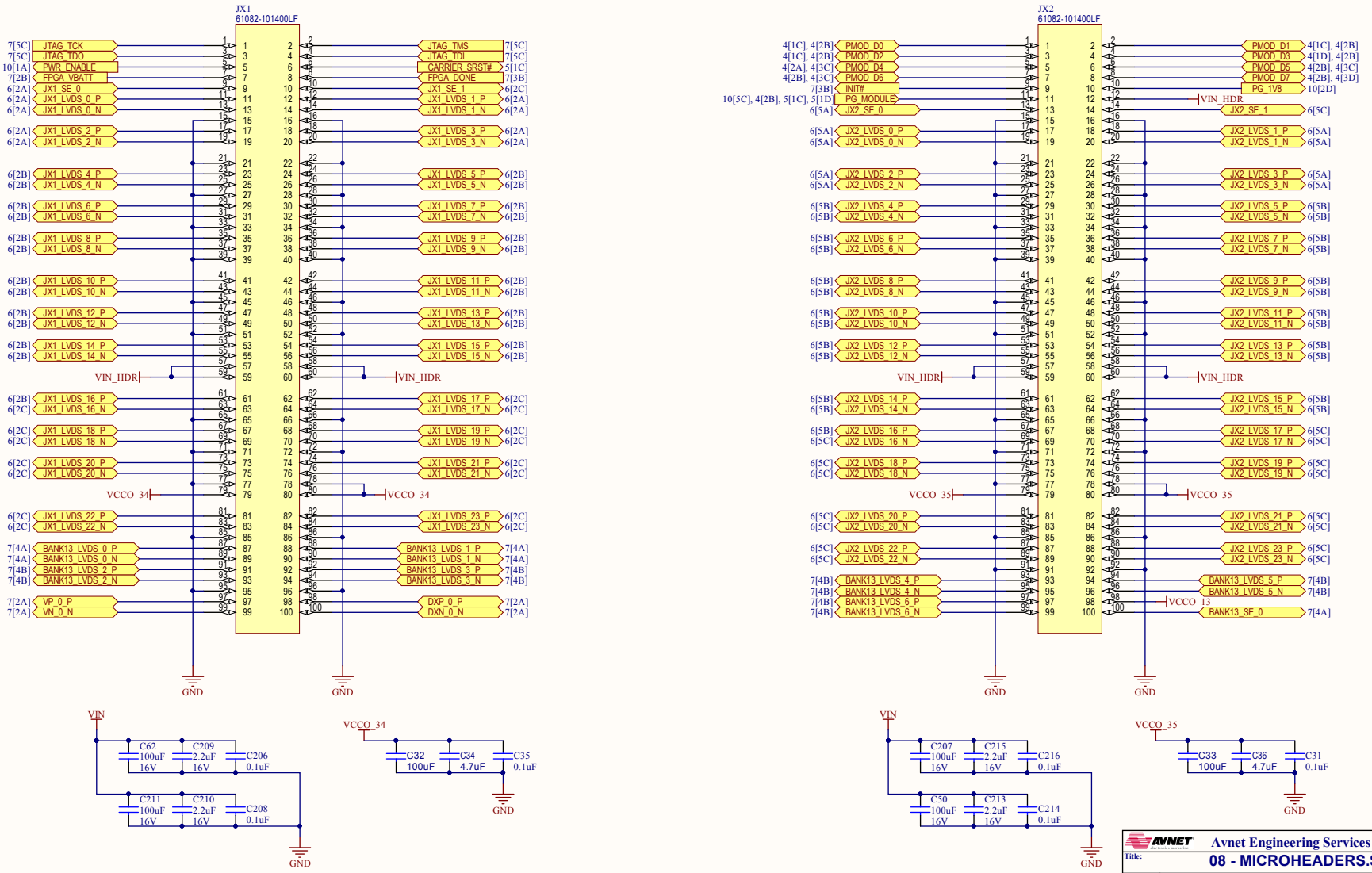
DONE LED



PC4 JTAG



AVNET Avnet Engineering Services		
Title: 07 - BANK 0, BANK13, JTAG.SchDoc		
Size: B	Document Number: MicroZed 7010	Rev: F-06
Date: 12/10/2014	Sheet 7 of 11	


JX1
61082-101400LF
JTAG_TCK
JTAG_TDO
PWR_ENABLE
FPGA_VBATT
JX1_SE_0
JX1_LVDS_0_P
JX1_LVDS_0_N
JX1_LVDS_2_P
JX1_LVDS_2_N
JX1_LVDS_4_P
JX1_LVDS_4_N
JX1_LVDS_6_P
JX1_LVDS_6_N
JX1_LVDS_8_P
JX1_LVDS_8_N
JX1_LVDS_10_P
JX1_LVDS_10_N
JX1_LVDS_12_P
JX1_LVDS_12_N
JX1_LVDS_14_P
JX1_LVDS_14_N
VIN_HDR
JX1_LVDS_16_P
JX1_LVDS_16_N
JX1_LVDS_18_P
JX1_LVDS_18_N
JX1_LVDS_20_P
JX1_LVDS_20_N
VCCO_34
JX1_LVDS_22_P
JX1_LVDS_22_N
BANK13_LVDS_0_P
BANK13_LVDS_0_N
BANK13_LVDS_2_P
BANK13_LVDS_2_N
VP_0_P
VN_0_N
JTAG_TMS
JTAG_TDI
CARRIER_SRST#
FPGA_DONE
JX1_SE_1
JX1_LVDS_1_P
JX1_LVDS_1_N
JX1_LVDS_3_P
JX1_LVDS_3_N
JX1_LVDS_5_P
JX1_LVDS_5_N
JX1_LVDS_7_P
JX1_LVDS_7_N
JX1_LVDS_9_P
JX1_LVDS_9_N
JX1_LVDS_11_P
JX1_LVDS_11_N
JX1_LVDS_13_P
JX1_LVDS_13_N
JX1_LVDS_15_P
JX1_LVDS_15_N
JX1_LVDS_17_P
JX1_LVDS_17_N
JX1_LVDS_19_P
JX1_LVDS_19_N
JX1_LVDS_21_P
JX1_LVDS_21_N
JX1_LVDS_23_P
JX1_LVDS_23_N
BANK13_LVDS_1_P
BANK13_LVDS_1_N
BANK13_LVDS_3_P
BANK13_LVDS_3_N
DXP_0_P
DXN_0_N
GND
VIN
C62 100uF 16V
C209 2.2uF 16V
C206 0.1uF
C211 100uF 16V
C210 2.2uF 16V
C208 0.1uF
VCCO_34
C32 100uF
C34 4.7uF
C35 0.1uF
JX2
61082-101400LF
PMOD_D0
PMOD_D2
PMOD_D4
PMOD_D6
INIT#
PG_MODULE
JX2_SE_0
JX2_LVDS_0_P
JX2_LVDS_0_N
JX2_LVDS_2_P
JX2_LVDS_2_N
JX2_LVDS_4_P
JX2_LVDS_4_N
JX2_LVDS_6_P
JX2_LVDS_6_N
JX2_LVDS_8_P
JX2_LVDS_8_N
JX2_LVDS_10_P
JX2_LVDS_10_N
JX2_LVDS_12_P
JX2_LVDS_12_N
VIN_HDR
JX2_LVDS_14_P
JX2_LVDS_14_N
JX2_LVDS_16_P
JX2_LVDS_16_N
JX2_LVDS_18_P
JX2_LVDS_18_N
VCCO_35
JX2_LVDS_20_P
JX2_LVDS_20_N
JX2_LVDS_22_P
JX2_LVDS_22_N
BANK13_LVDS_4_P
BANK13_LVDS_4_N
BANK13_LVDS_6_P
BANK13_LVDS_6_N
PMOD_D1
PMOD_D3
PMOD_D5
PMOD_D7
PG_1V8
JX2_SE_1
JX2_LVDS_1_P
JX2_LVDS_1_N
JX2_LVDS_3_P
JX2_LVDS_3_N
JX2_LVDS_5_P
JX2_LVDS_5_N
JX2_LVDS_7_P
JX2_LVDS_7_N
JX2_LVDS_9_P
JX2_LVDS_9_N
JX2_LVDS_11_P
JX2_LVDS_11_N
JX2_LVDS_13_P
JX2_LVDS_13_N
JX2_LVDS_15_P
JX2_LVDS_15_N
JX2_LVDS_17_P
JX2_LVDS_17_N
JX2_LVDS_19_P
JX2_LVDS_19_N
JX2_LVDS_21_P
JX2_LVDS_21_N
JX2_LVDS_23_P
JX2_LVDS_23_N
BANK13_LVDS_5_P
BANK13_LVDS_5_N
VCCO_13
BANK13_SE_0
VIN
C207 100uF 16V
C215 2.2uF 16V
C216 0.1uF
C50 100uF 16V
C213 2.2uF 16V
C214 0.1uF
VCCO_35
C33 100uF
C36 4.7uF
C31 0.1uF
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08 - MICROHEADERS.SchDoc
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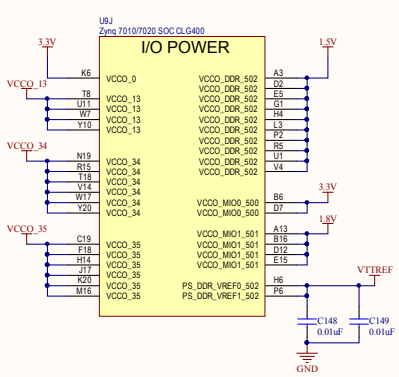

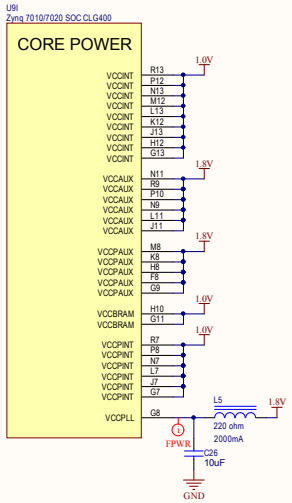

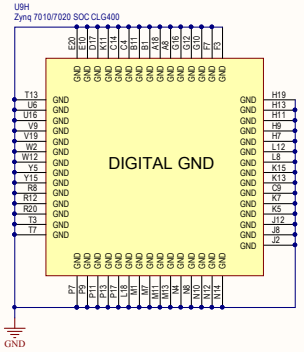

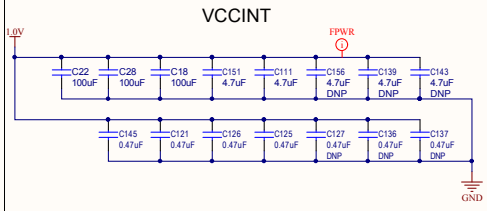

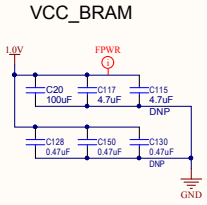

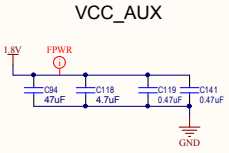

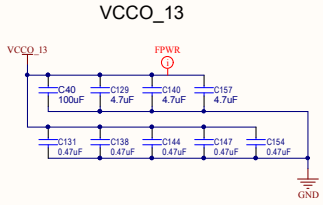

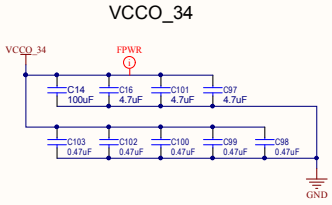

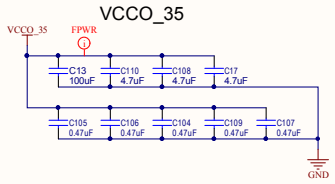

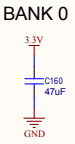

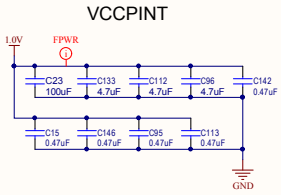

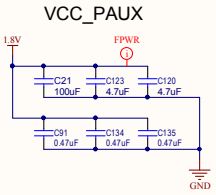

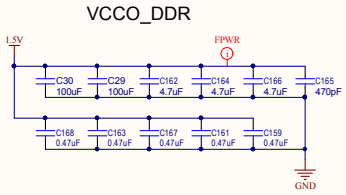

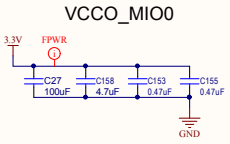

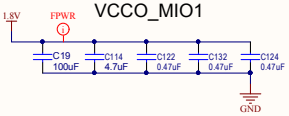

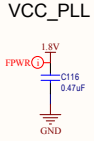

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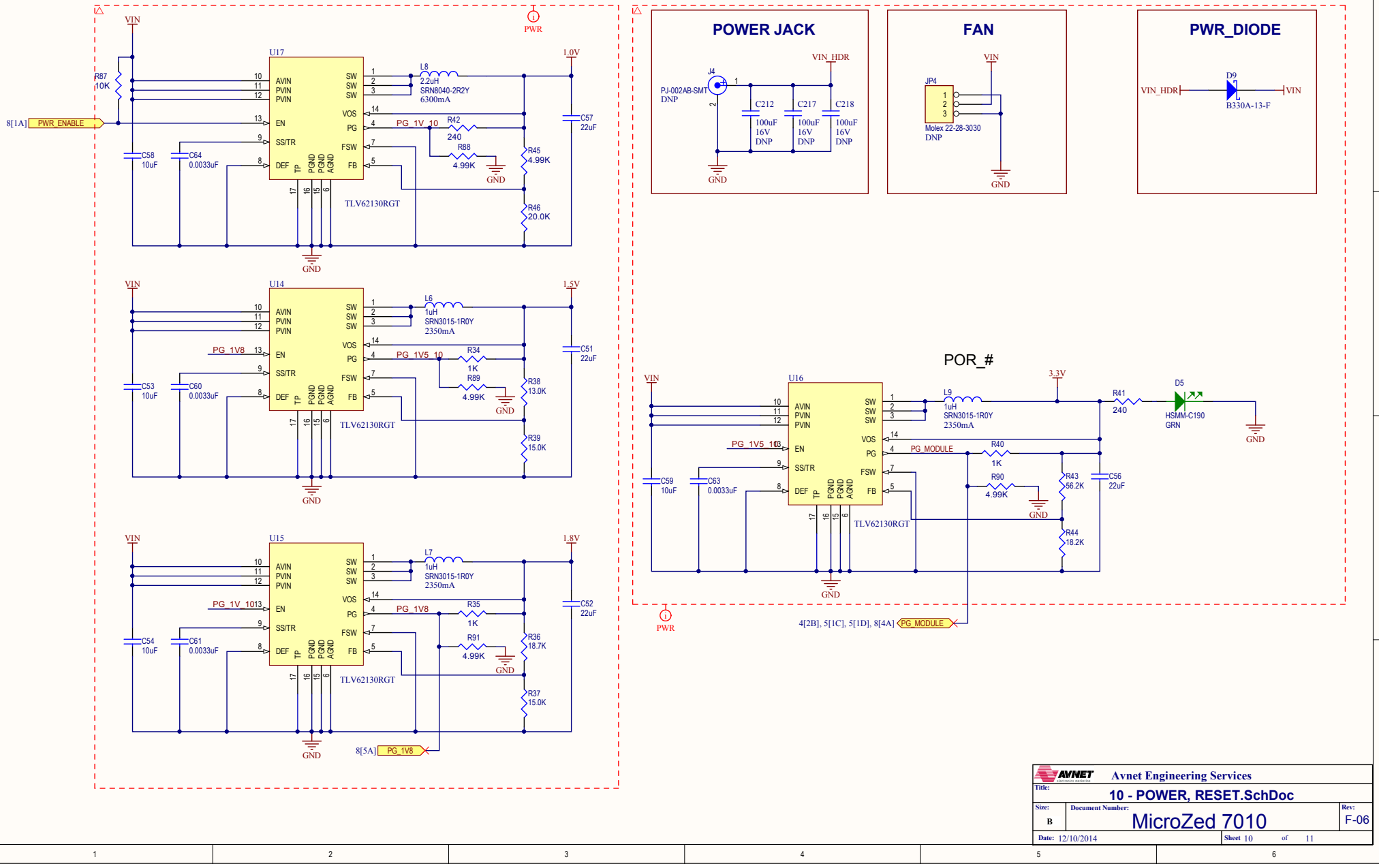

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Revision Notes:

Revision C Changes:
1) Add Silkscreen Logos - CE, RoHS and Copper Part Number on board
2) Reduce R34, 35, (40), 42 from 100K to 1K
3) Add pulldown resistors to R34, 35, (40), 42 - Value 2.2K - 5.00K
4) Fuse (PTC) recommendation note for R50, 12V input
5) Connect: U8.6 to U20.2
6) Connect: U3.16 to U8.3
7) Connect: JX2.10 to U15.4
8) Change 4.75K resistors to 4.99K
9) Added rubber feet to BOM
10) Add staple point vias for J2 USB connector.

Revision D Changes (no production):
1) Attached JX2.10 to U15.4

Revision E Changes (no production):
1) Replaced U1 from MAX13035EETE+ to TI TXS02612ZQSR part.
2) Added Sheet 11.
3) Moved mechanical information to back page.

Revision F Changes:
1) Changed USB UART default power to bus power. Attach VBUS power net to U2.7 REGIN pin. Disconnect Vdd pin from +3.3V.
2) Added Ethernet LED drive buffer circuit to reduce 3.3V PHY backfeed.
3) Added: D10, D11, JT7, R97, R98 to allow user to configure USB Bus or Self power mode.
4) Removed two fansink mounting holes. Removed ground attribute to mounting holes (in layout files).
5) Added D12 PolyZen (PTC+Zen) USB UART protection component as configurable option.
6) Added R99 0 ohm resistor for D12 bypass (default).
7) Added C221 2.2uF capacitor for USB transient and flyback voltage protection.
8) Revised notes (above).
9) 28 Jan 14: Updated USB OTG configuration notes.
10) 10 Dec 14: Updated JT6 note on sheet 3.

Mechanicals:

PCB
MMP-7Z045-PCB-F

PCB Mounting Holes

MTG5 0
MOUNTING HOLE 125mil

MTG2 0
MOUNTING HOLE 125mil

MTG1 0
MOUNTING HOLE 125mil

MTG6 0
MOUNTING HOLE 125mil

Fansink Mounting Holes

MTG4
MOUNTING HOLE

MTG3
MOUNTING HOLE

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