

Key high-speed connector layout techniques

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This article discusses the essential considerations of mounting connectors on PCBs. These aspects include the pin assignments for signals and grounds, stubs due to the pins of through-hole or press-fit connector, and impedance mismatch caused by surface mount pads of the connector. A connector is one of the transmission-line elements along a multiple-board signal path between transmitter and receiver. Therefore, it is crucial to select and mount the connector in a manner that best suits the system design.

Pin assignment for signals with respect to ground

High speed serial signal pairs can be routed to connector pins as shown in Figure 1, where inverting (S-) and non-inverting (S+) are assigned to two adjacent pins. Furthermore, a signal pair is segregated from another by ground (G). Such pin assignments prevent mode conversion from differential to common. As a result, the risk of inter-pair crosstalk and common-mode noise coupling is minimized.

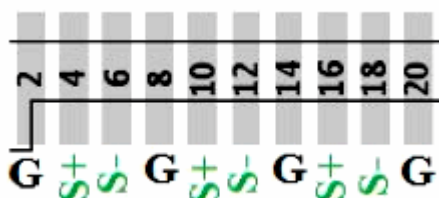


Figure 1. Pin assignment on connector for high speed serial signal pairs

Effect of connector pin stubs

When a through-hole or press-fit connector is used, it's important to make sure that the pin length does not exceed the PCB thickness. A stub exists when the connector pin is longer than the PCB thickness. With reference to a 3D model using Keysight EMPro shown in Figure 2, a press-fit connector with 145 mil pin length is mounted on top of a PCB with 45 mil thickness. Assuming a signal pair is routed on the bottom layer of the PCB, a 100 mil pin stub results. This pin stub has a negative impact on signal transmission, as the bandwidth or resonant frequency of the signal path is inversely proportional to the pin stub length and impedance discontinuity or mismatch. The relationship between the channel bandwidth and pin stub length is governed by Eq. (1). The longer stub intensifies the impedance mismatch, which in turn decreases the channel bandwidth.

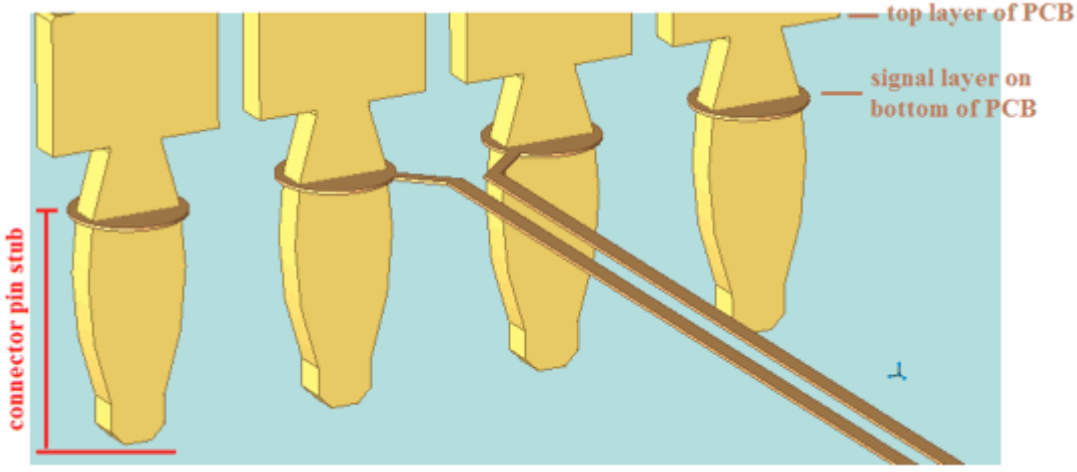


Figure 2. 3D model of connector pin stub using Keysight EMPro

$$f_o = \frac{c}{4 \times stub_length \times \sqrt{D_{keff}}} \quad (1)$$

f_o = resonant frequency (Hz)

c = speed of light (12 inch/ns)

$stub_length$ in inches

D_{keff} = effective dielectric constant

The effect of a pin stub on signal transmission is studied by observing differential insertion loss (SDD21) and time domain reflectometry (TDR) of a 3D transmission line model constructed using EMPro. A differential pair of 100Ω enters the press-fit male connector with various stub lengths (0 mil, 50 mil, and 100 mil) on PCB #1 and exits the press-fit female connector without stubs on PCB #2. The trace length on each PCB is 0.5 inch and medium loss material is used as substrate. The plots of SDD21 and TDR are shown in Figure 3. The model with a 100 mil stub has 20Ω impedance mismatch and 11 GHz resonance. Meanwhile, the model with a 50 mil stub has 14Ω impedance mismatch and 17 GHz resonance. Once there is no pin stub, the impedance mismatch is reduced to 10Ω and resonance extends beyond 18GHz.

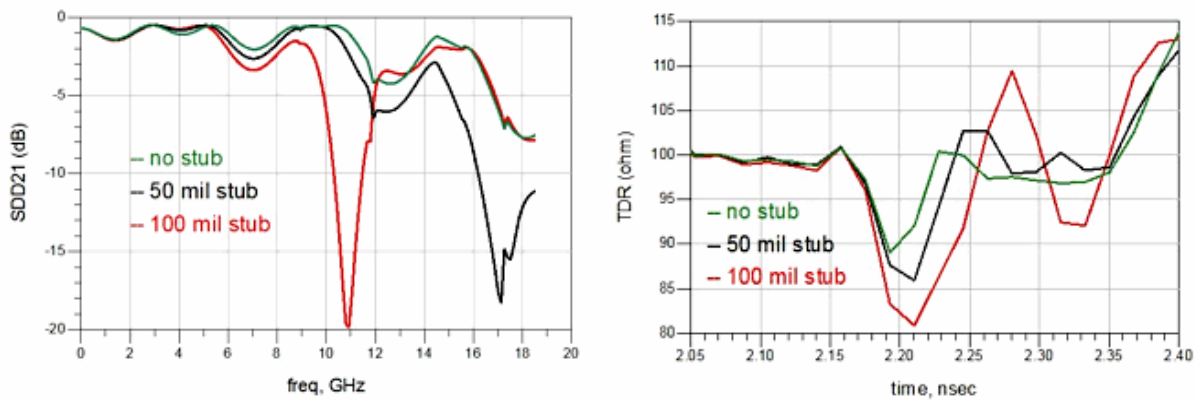


Figure 3. SDD21 and TDR plots reflecting the effect of pin stub

There are several ways to reduce or remove pin stubs on a PCB. When dealing with a soldered through-hole connector, stubs can be reduced by manually trimming the pins, as illustrated in Figure 4. On the other hand, when dealing with press-fit types, always try to use a connector with pin lengths shorter than the PCB thickness, and route the high speed signal on the layer as close as possible to the tip of the pin or bottom of the PCB with blind or backdrilled vias, as illustrated in Figure 5.

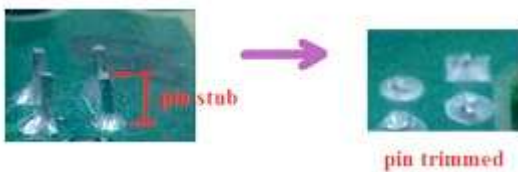


Figure 4. Stub reduction by trimming pins

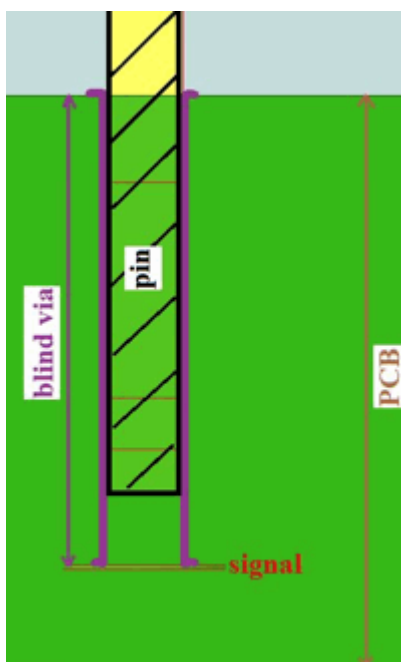


Figure 5. Cross sectional view of press-fit connector on thicker PCB with blind via

Effect of SMT pads

Connector SMT pads contribute to impedance mismatch on the transmission line. Once a signal pair with narrower traces reaches the SMT pads with wider copper, the strip capacitance of this segment is increased, as governed by Eq. (3), which in turn leads to the dip of characteristic impedance of the transmission segment, as governed by Eq. (2). This scenario is known as a capacitive discontinuity and it causes signal reflection and degradation. To mitigate this negative impact, a cutout – the same size as the SMT pad and right beneath it – is inserted on the ground plane on layer 2, so that the SMT pad is referenced to ground on layer 3. This technique increases the “ d ” or distance between the SMT pad and its reference, which in turn balances out the effect due to the wider copper of the pad, and minimizes the impedance mismatch. However, “ d ” shall not be increased too much, where strip inductance overrides capacitance, and leads to the increase of impedance or inductive discontinuity, as governed by Eq. (4).

$$Z_o = 31.6 \times \sqrt{\frac{L}{C}} \quad (2)$$

$$C = \frac{\epsilon w l}{d} \quad (3)$$

$$L \approx 2 \left[\ln \left(\frac{5.98d}{0.8w + t} \right) \right] \quad (4)$$

C = strip capacitance (in pF)

L = strip inductance (in nH)

Z_o = characteristic impedance (in ohms)

ϵ = dielectric permittivity

w = width of SMT pad

l = length of SMT pad

d = distance between SMT pad and reference plane underneath

t = thickness of SMT pad

To observe the effect of an SMT pad and reference plane cutout on signal transmission, a 3D model illustrated in Figure 6 is constructed in EMPro. A signal pair of 100Ω (6 mil trace width and 1.2 mil thickness in single ended mode) enters the SMT pad of female connector on PCB #1 and exits the SMT pad of male connector on PCB #2. Each SMT pad is 12 mil wide. The trace length on each PCB is 0.5 inch and medium loss material is used as substrate. Meanwhile, the substrate thickness between the top and second layer is 4 mil. A cutout is inserted on layer two right beneath each SMT

pad. Various “ d ” are set and results are compared.

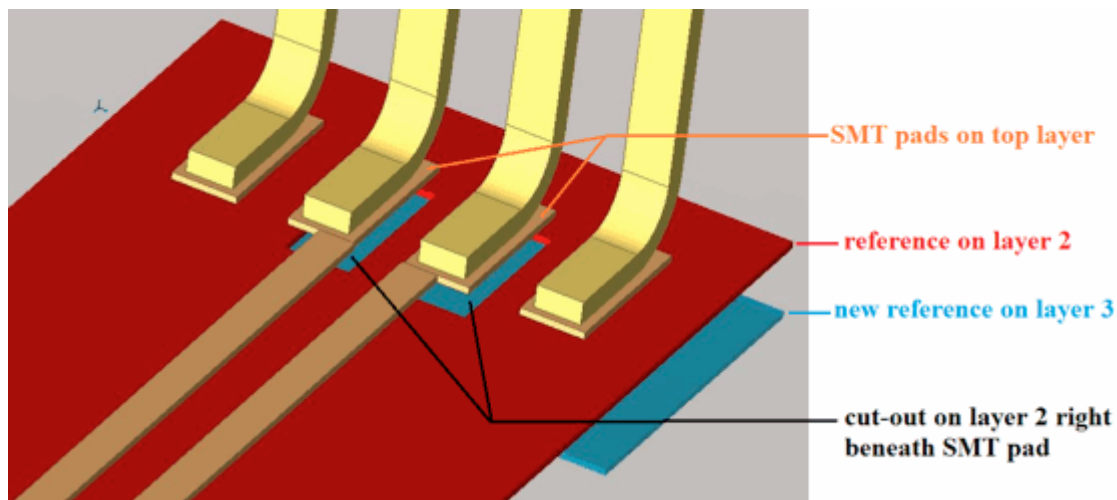


Figure 6. 3D model of SMT connector on PCB with ground plane cutout in Keysight EMPro

With reference to SDD21 and TDR plots in Figure 7, a cutout with moderate “ d ” (10 mil “ d ” for 12 mil SMT pad width) is necessary to mitigate the capacitive discontinuity and insertion loss. A further increase in “ d ” intensifies the inductive discontinuity and insertion loss.

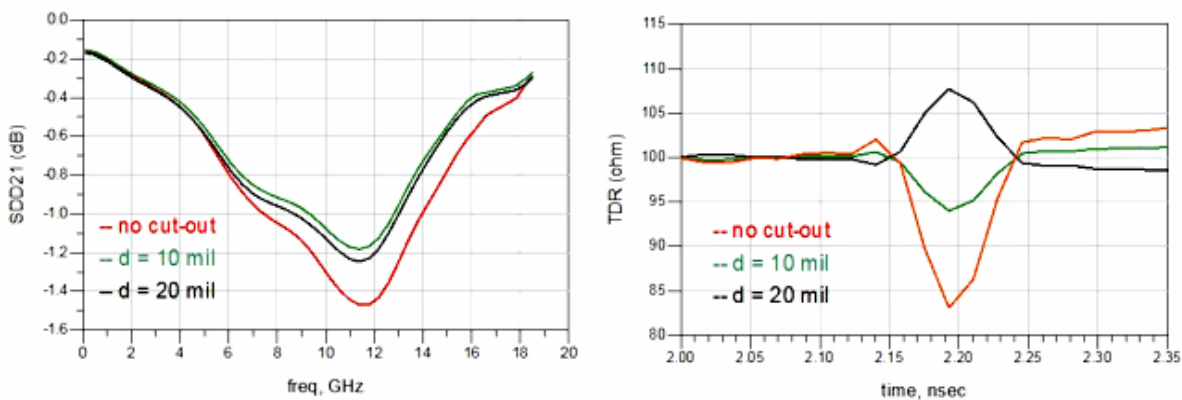


Figure 7. SDD21 and TDR plots reflecting the effect of SMT pad and reference plane cutout

References

- [1] Eric Bogatin, “Signal Integrity-Simplified”, Prentice Hall, 2003
- [2] Brian Vicich, EDN, "[Bandwidth demand drives connector design](#)"
- [3] [Samtec connectors](#)
- [4] [Erni connectors](#)

[5] TI, "[High Speed PCB Layout Techniques](#)"

Also see:

- [How to estimate ground bounce in a connector: Rule of Thumb #8](#)
- [How long a stub is too long?: Rule of Thumb #18](#)
- [PCB design course & checklist](#)

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