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A	Picozed 7010/7020 SOM	Avnet Engineering Services	www.picozed.org	AVNET®	A
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Picozed 7010/7020 SOM

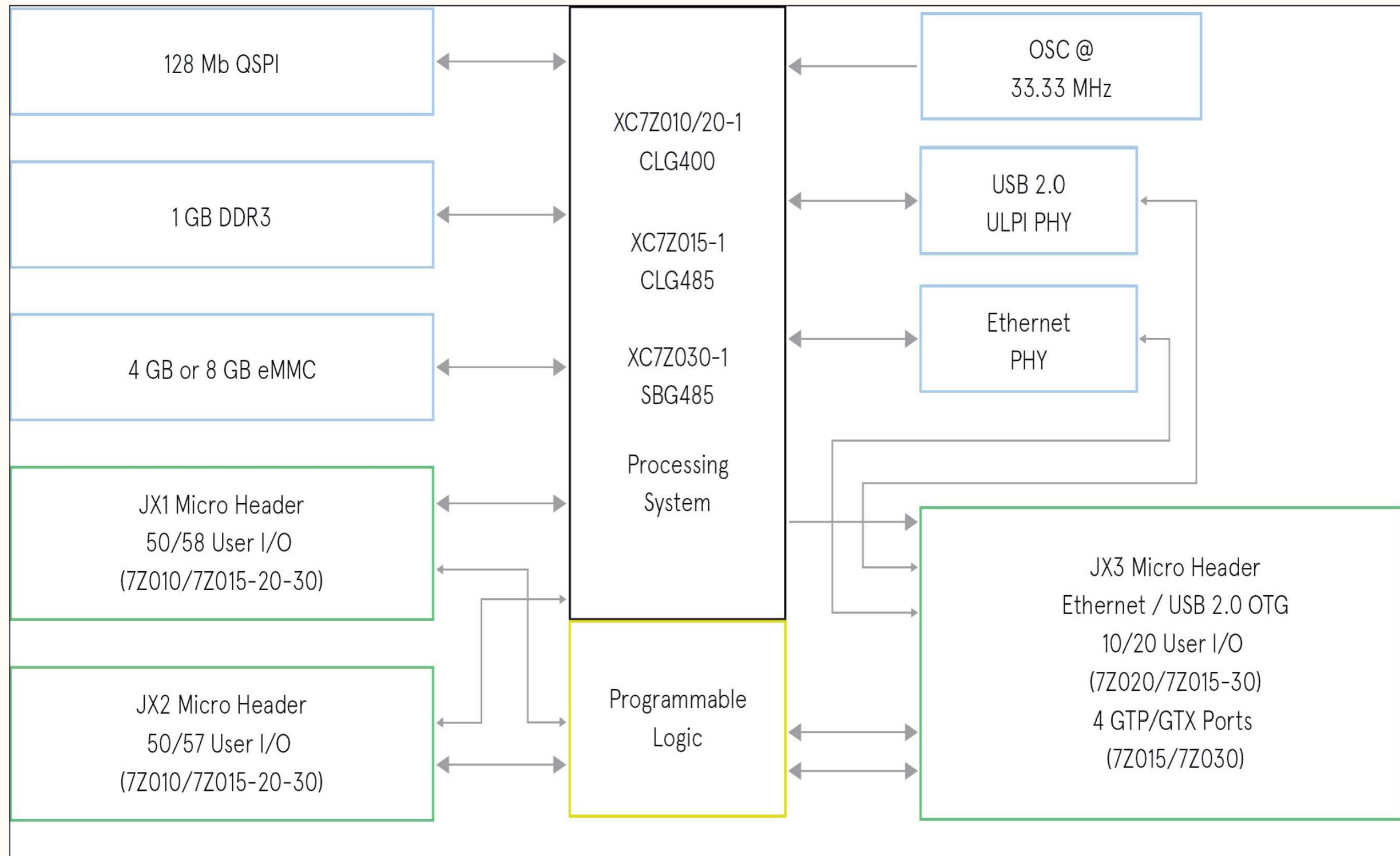
Revision E

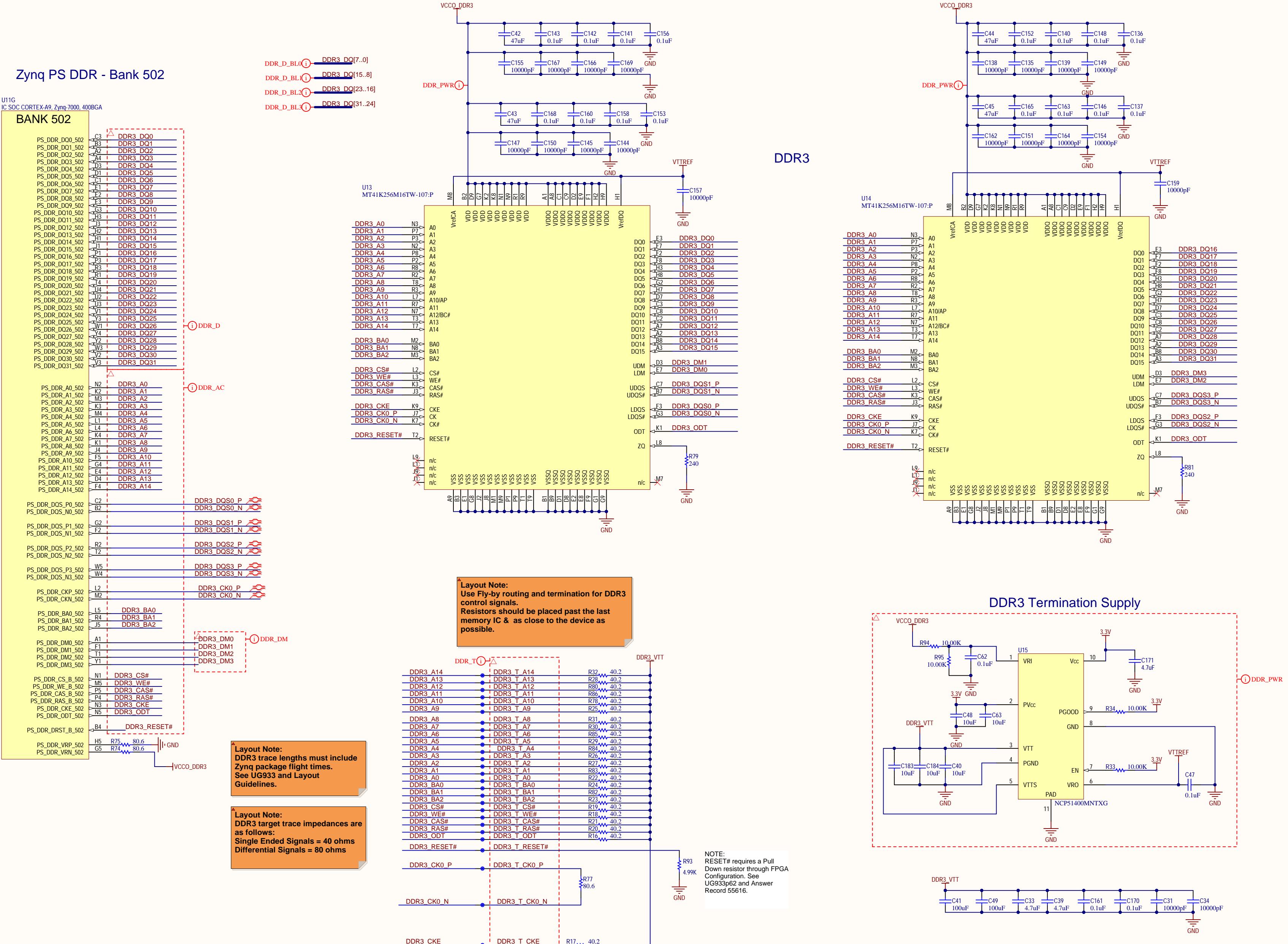
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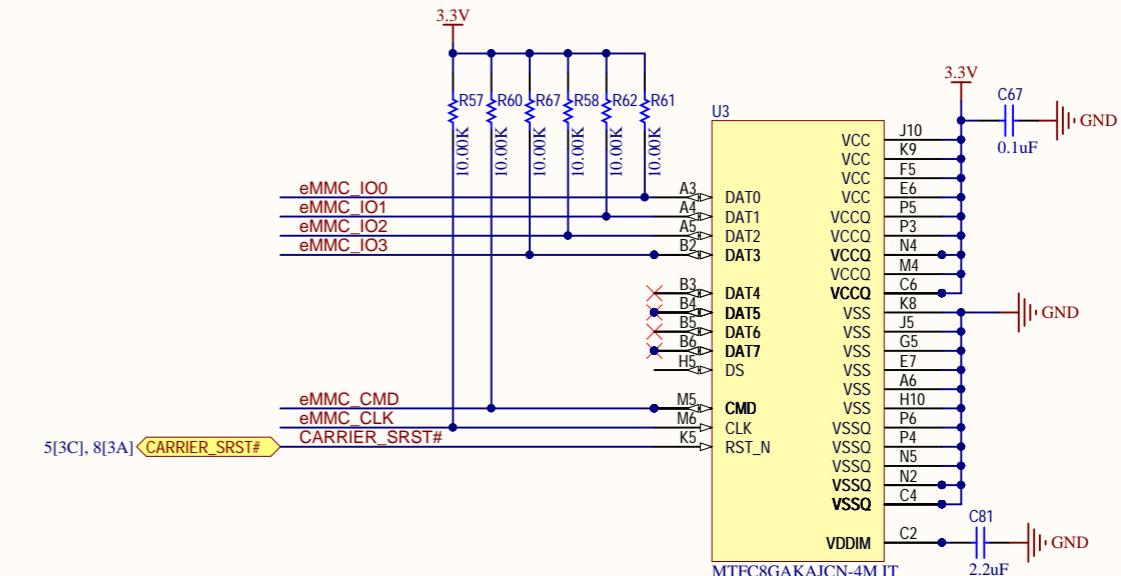
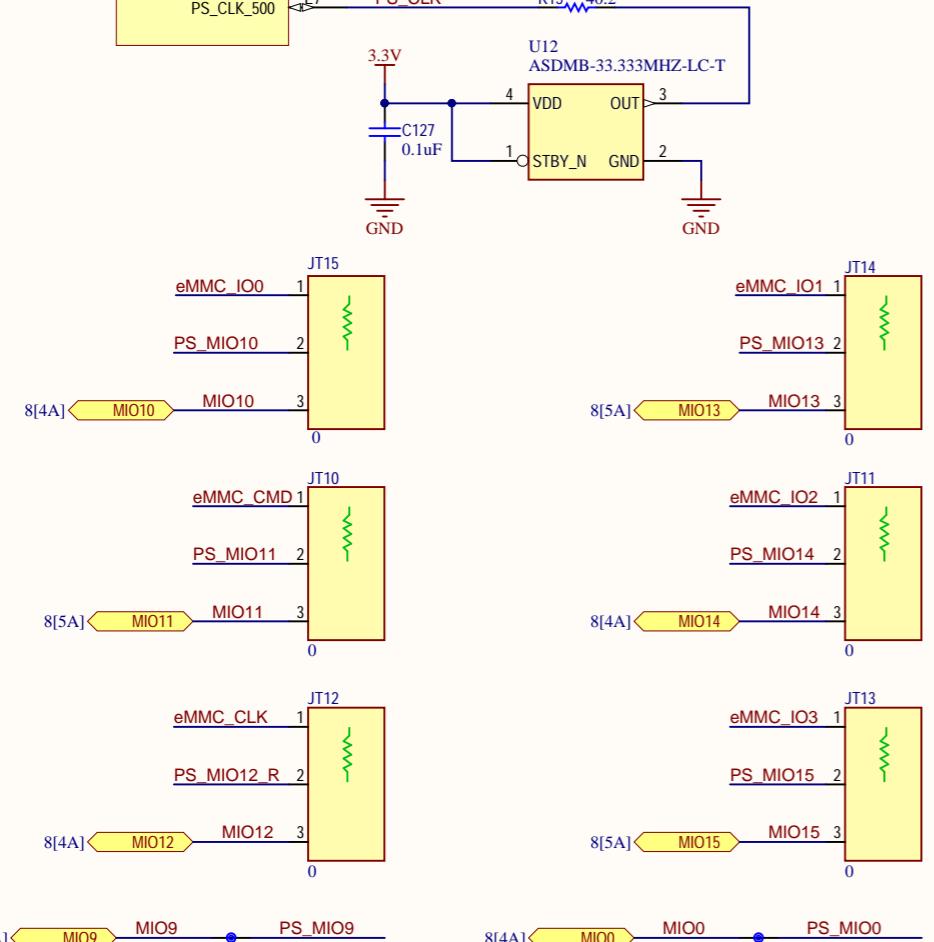
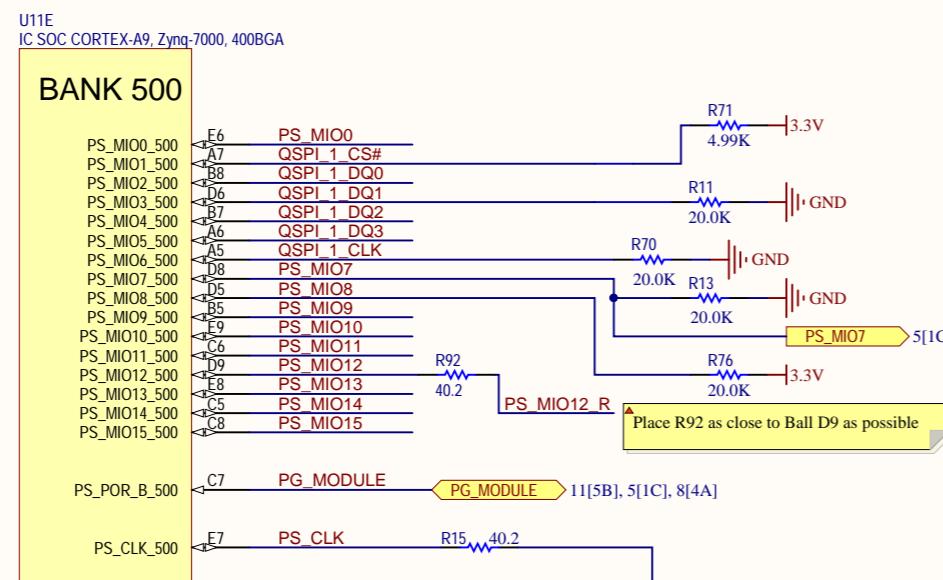
Project Name:	Picozed 7010/7020 SOM	PCB Rev:	E	BOM:	01	Variant:	01
Doc Num:	SCH-PZ1SOM	Date:	12/18/2017	Time:	11:11:34 AM		
Sheet Title:	01 - Avnet Lead Sheet_B.SchDoc	Size:	B	Sheet:	1 of 12		



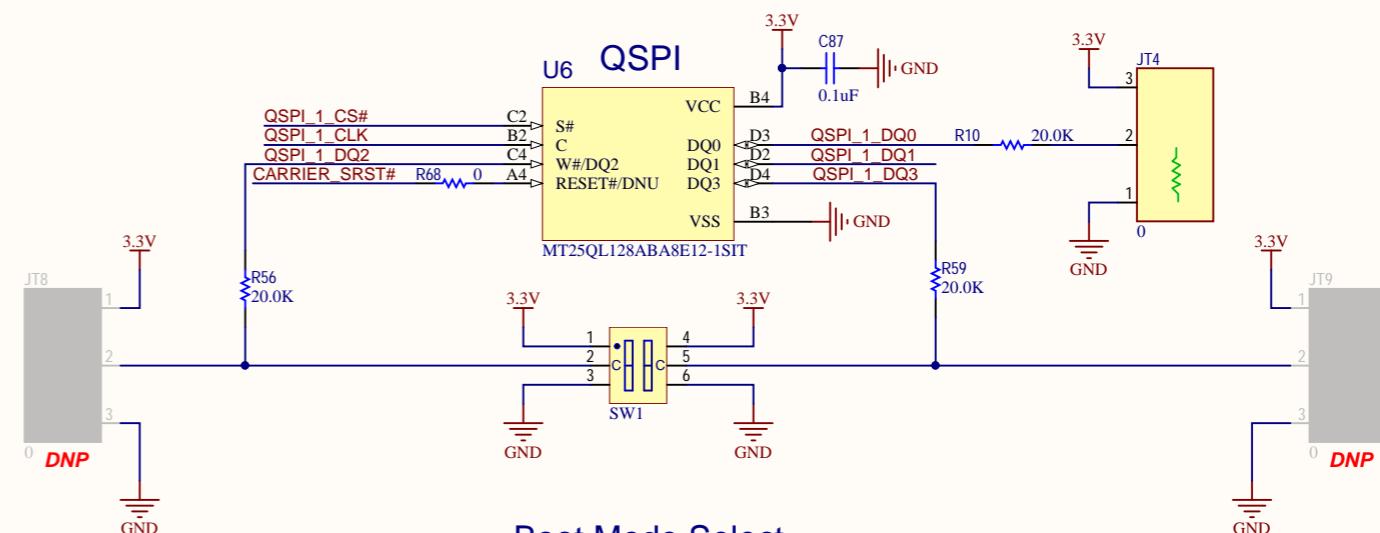


Embedded eMMC: 4GB, 8GB (default), 16GB, 32GB, 64GB

Zynq PS MIO - Bank 500



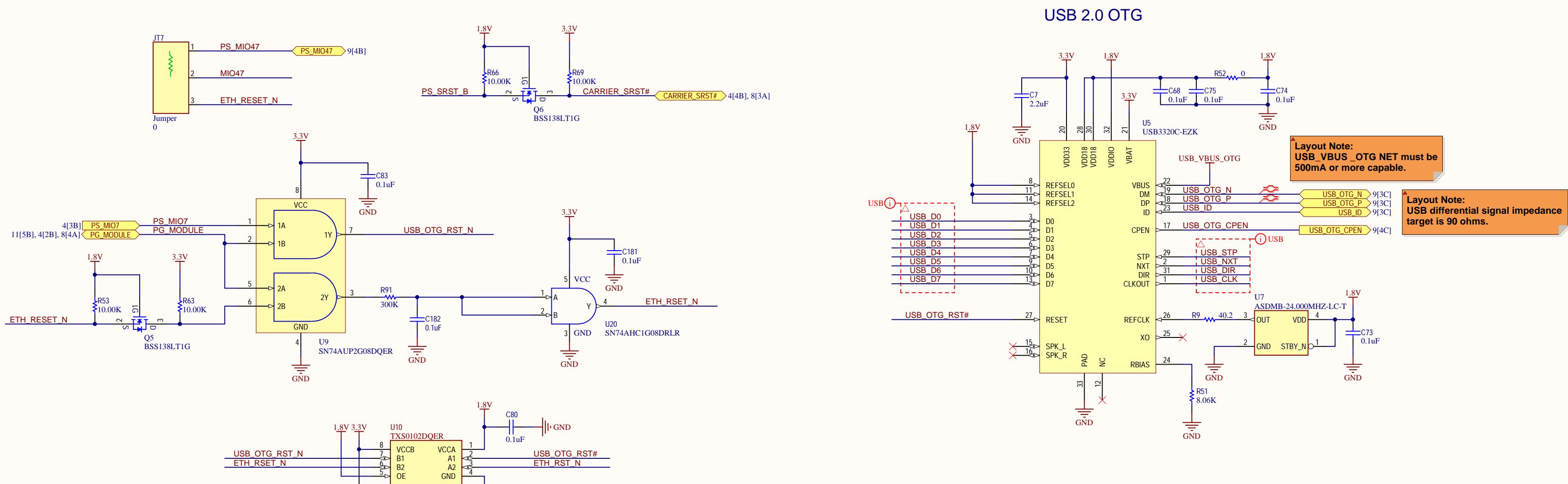
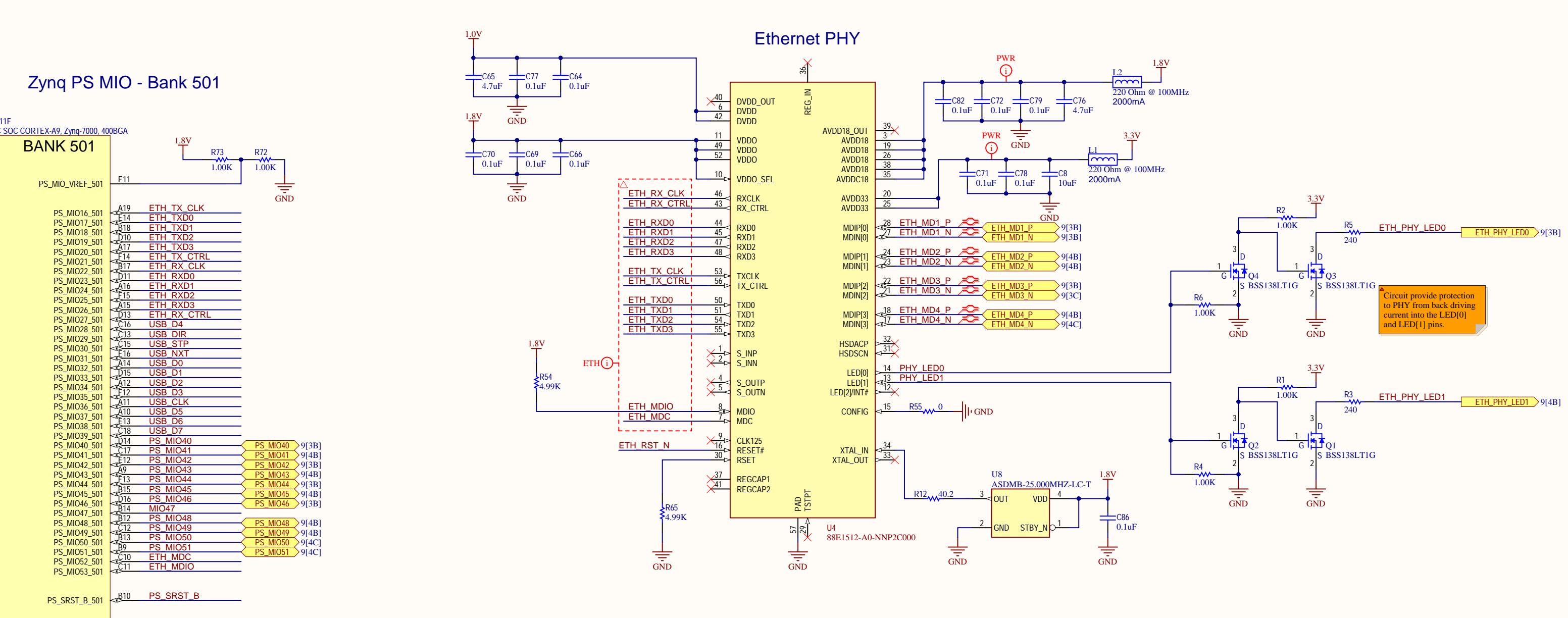
▲ This eMMC footprint is based on the 169-ball WFBGA 14.0mm x 18.0mm x 0.8mm Micron package. The footprint is compatible with the 153-ball WFBGA 11.5mm x 13.0mm x 0.8mm, which is what is populated. See the Hardware User Guide for a conversion table

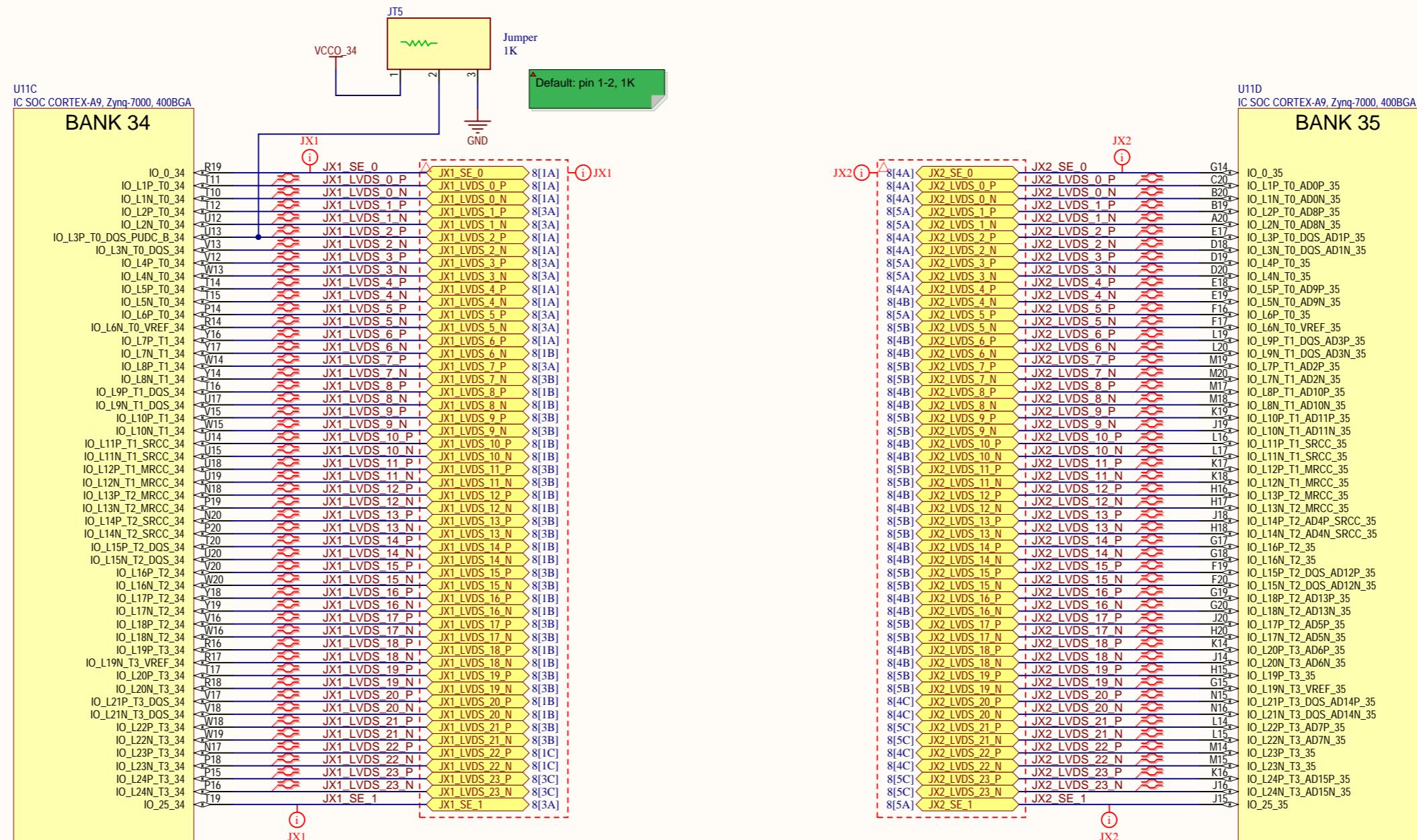


Boot Mode Select

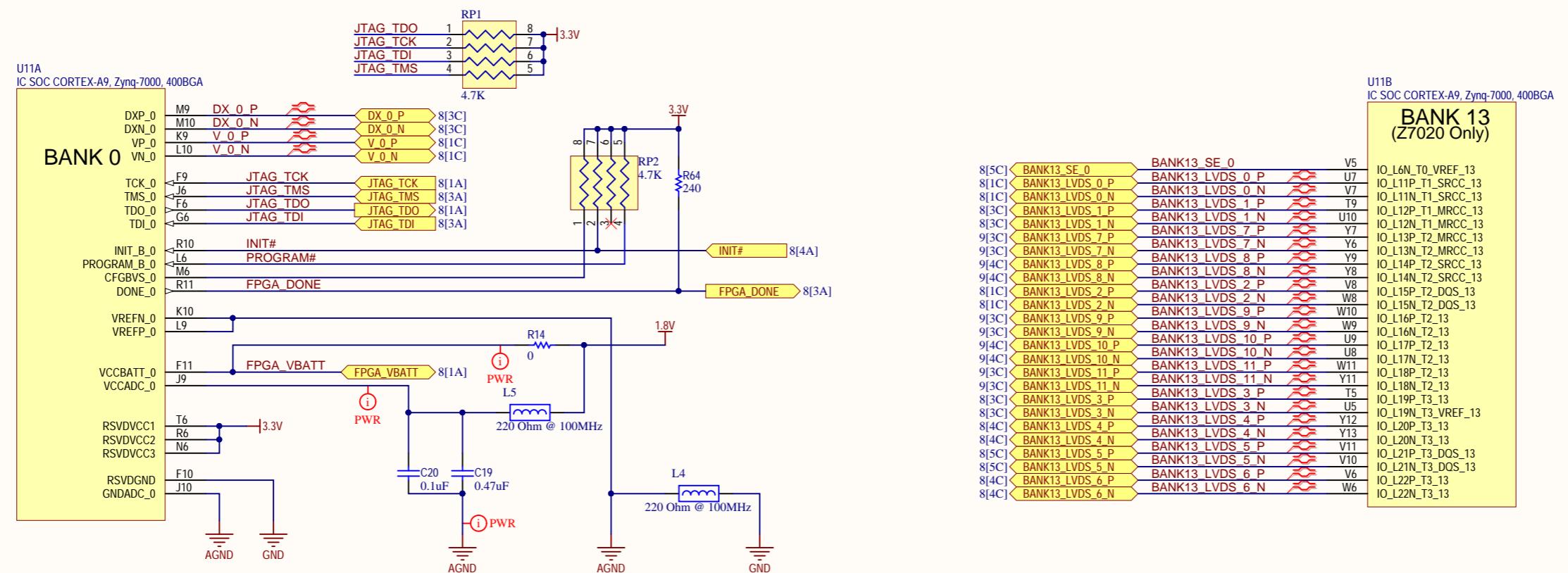
BOOT MODE	JT4	SW1 (1-3)	SW1 (4-6)
QSPI	X	LOW (2-3)	HIGH (4-5)
SD CARD	X	HIGH (1-2)	HIGH (4-5)
JTAG	X	LOW (2-3)	LOW (5-6)
IND JTAG	HIGH (2-3)	LOW (2-3)	LOW (5-6)
CASCADE JTAG	LOW (1-2)	LOW (3-3)	LOW (5-6)

CASCADE ITAG - DEFAULT MODE



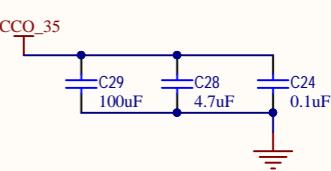
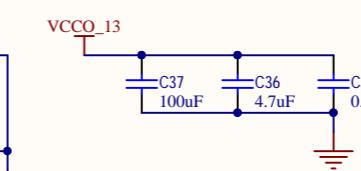
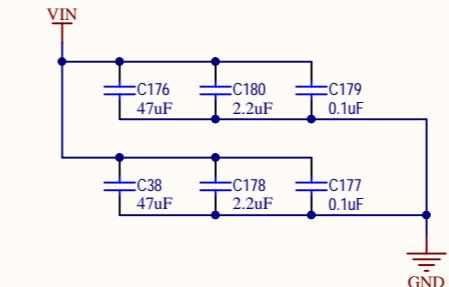
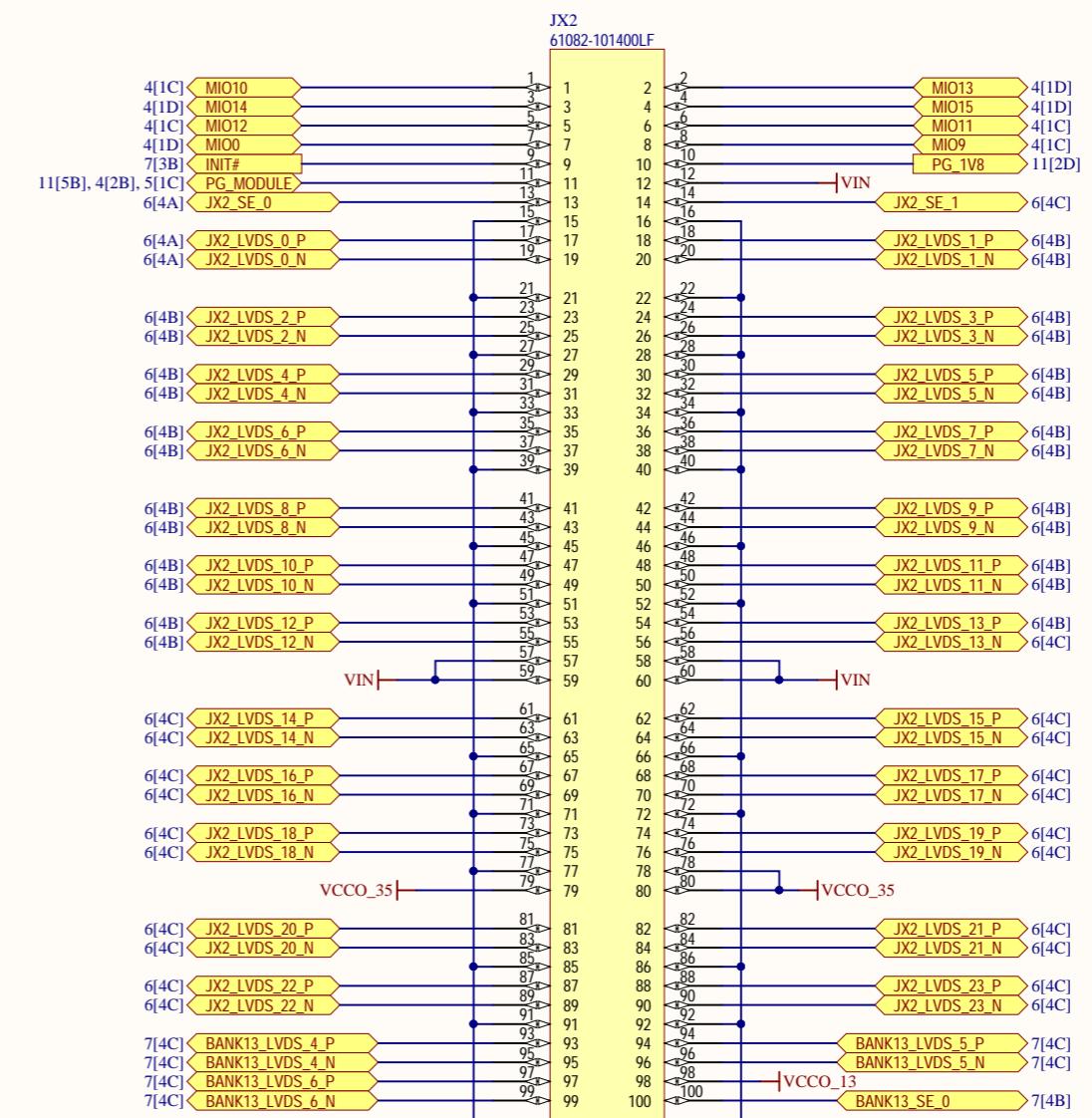
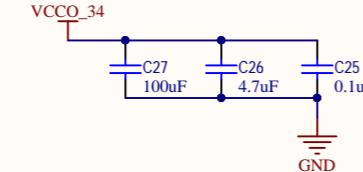
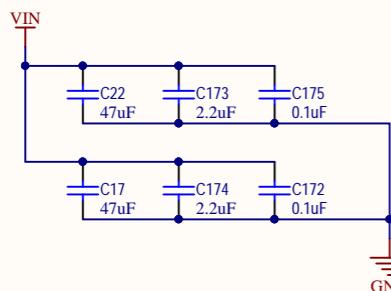
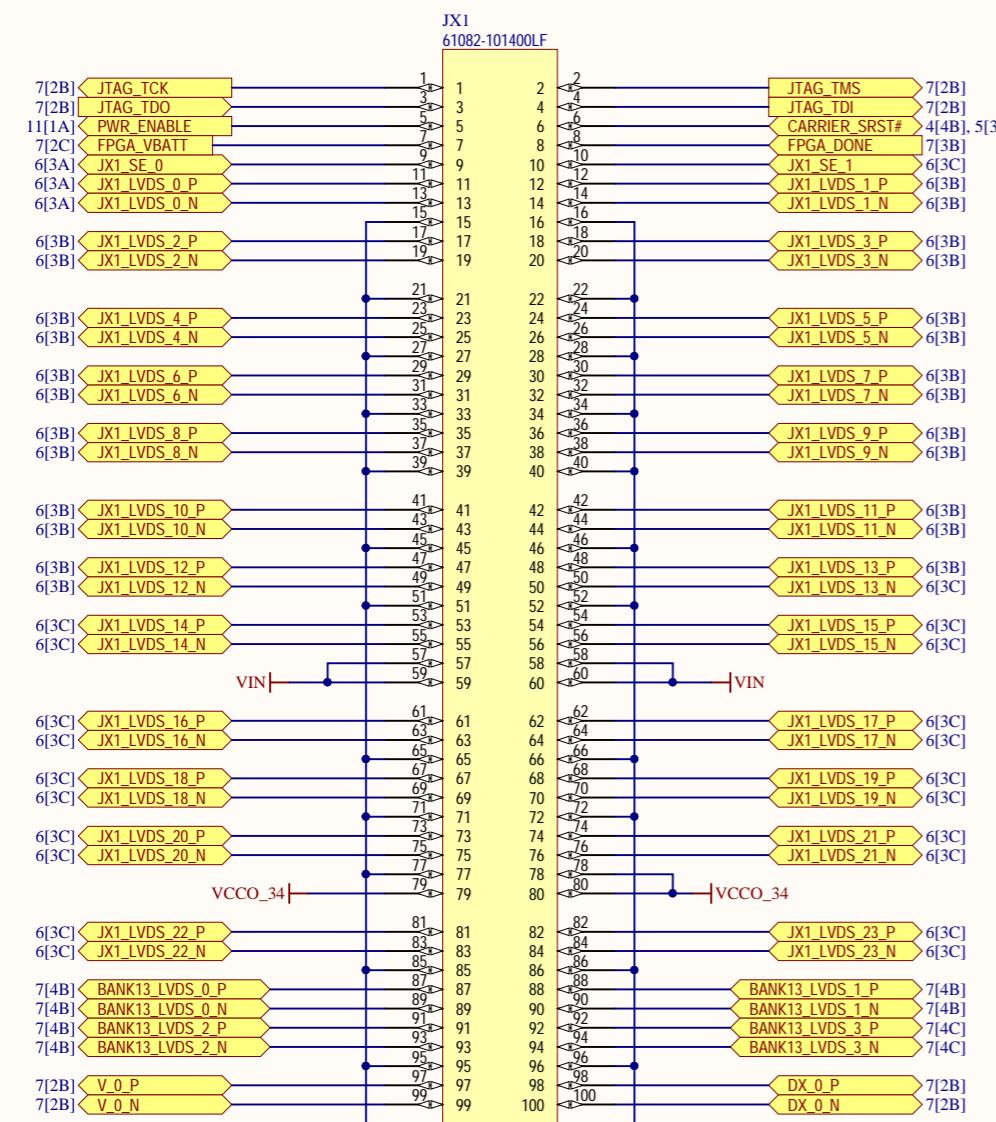


A



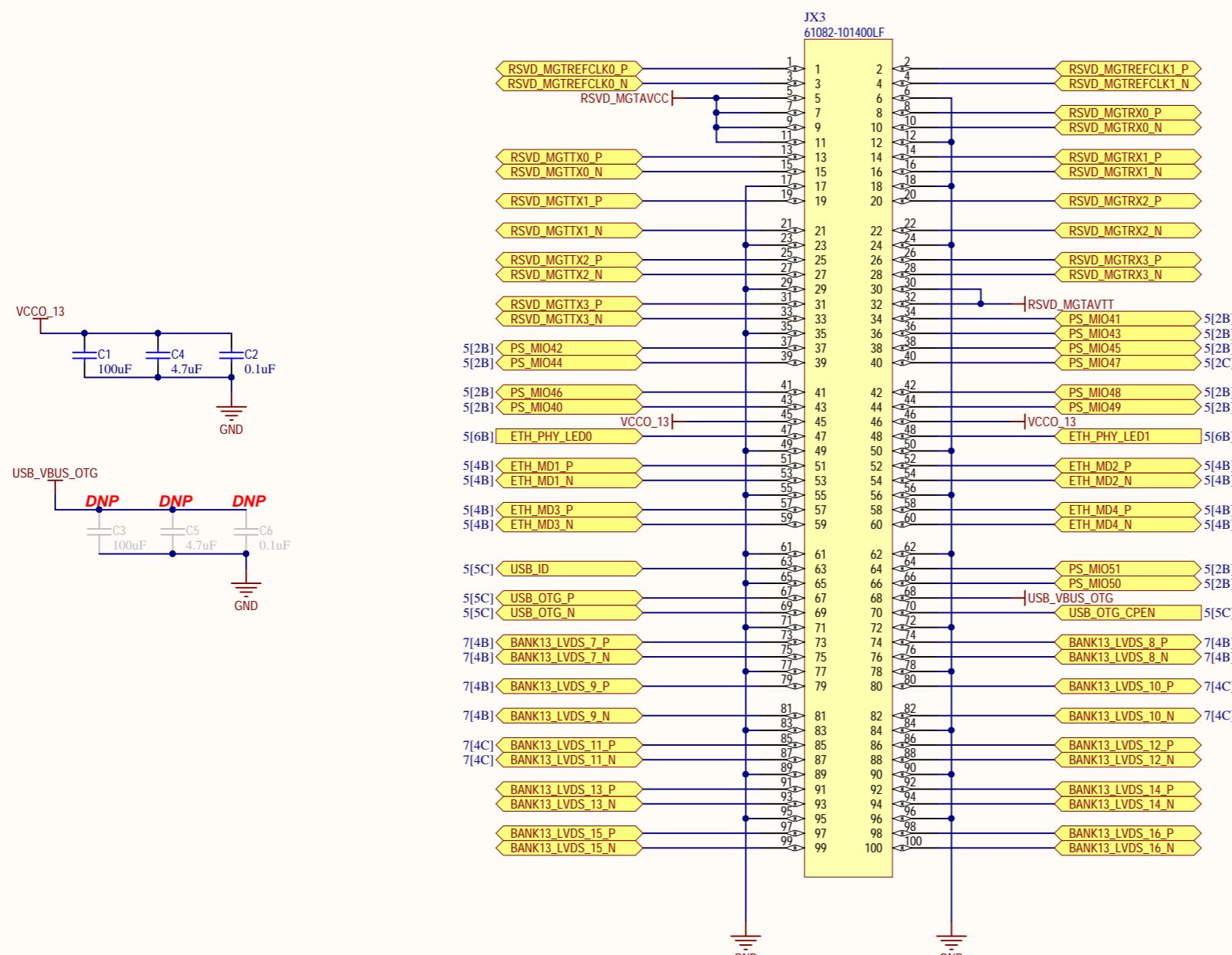
A

11[5B], 4[2B], 5[1C]



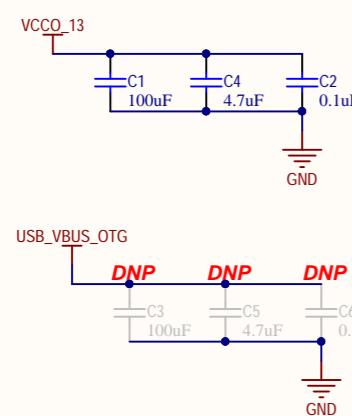
Avnet Engineering Services		PCB Rev:	BOM:	Variant:	
Project Name:	Picozed 7010/7020 SOM	E	01	01	
Doc Num:	SCH-PZ1SOM	Date:	12/18/2017	Time:	11:11:36 AM
Sheet Title:	08 - MICROHEADERS - JX1 and JX2.SchDoc		Size:	B	Sheet: 8 of 12

A



All RSVD_MGT* signals are RESERVED for devices with MGTs.

B



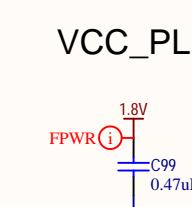
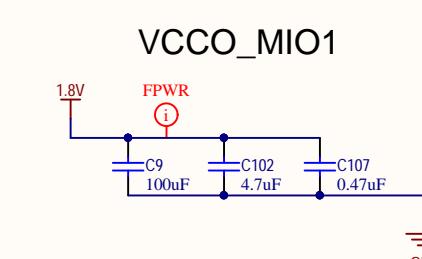
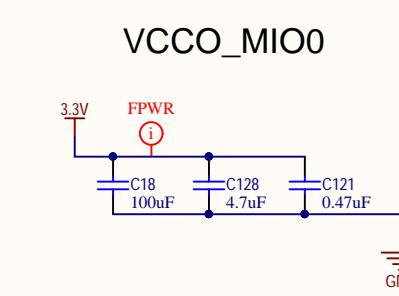
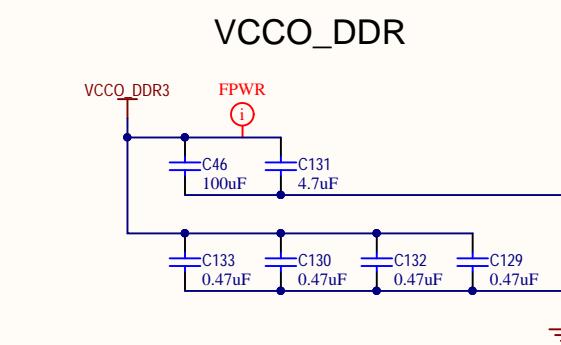
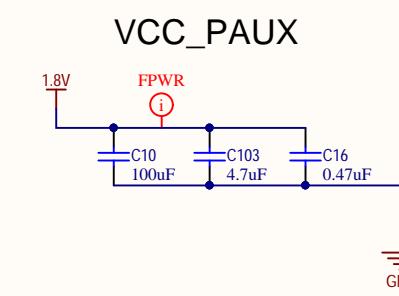
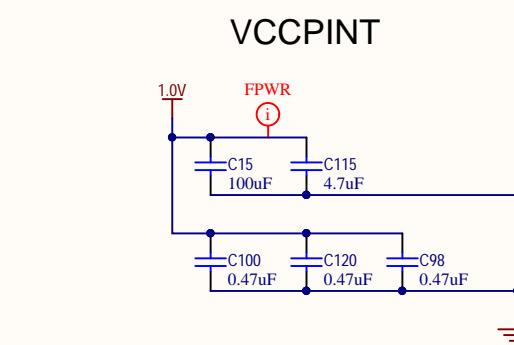
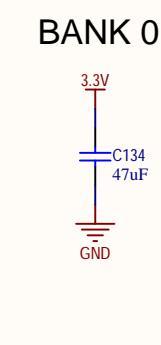
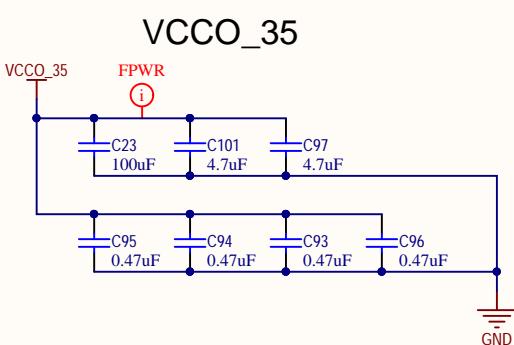
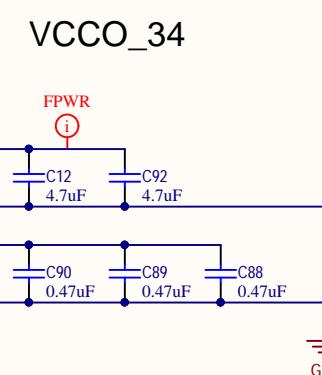
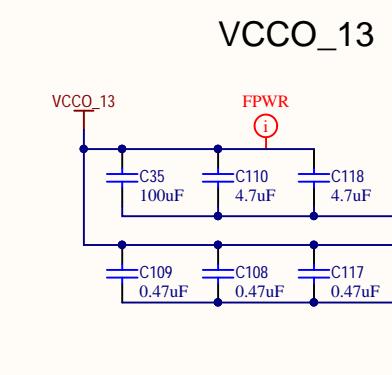
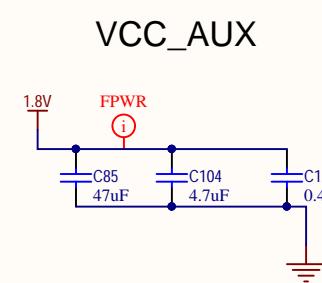
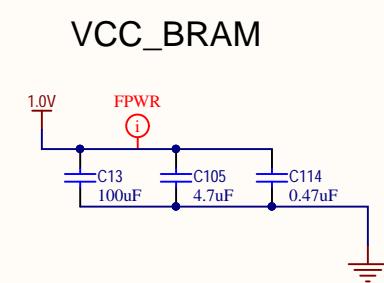
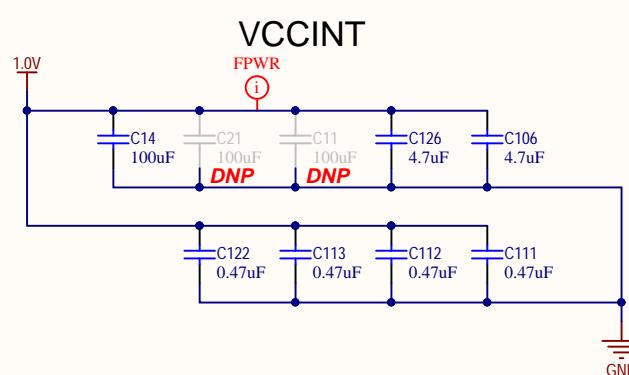
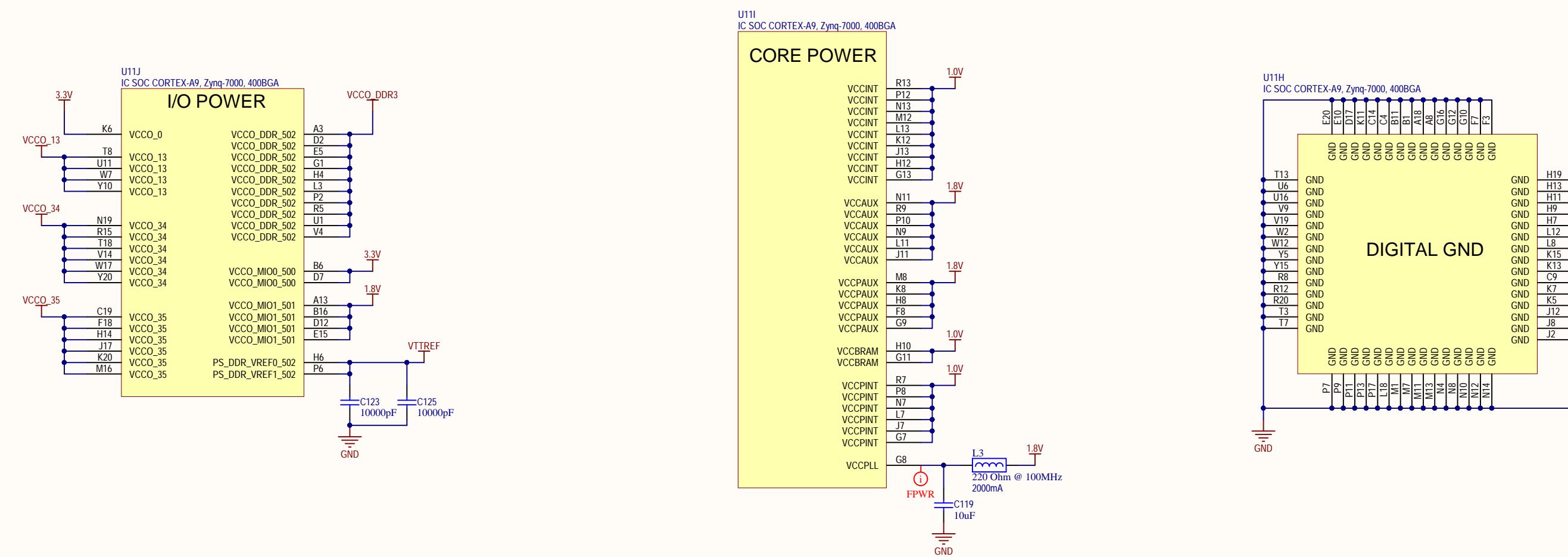
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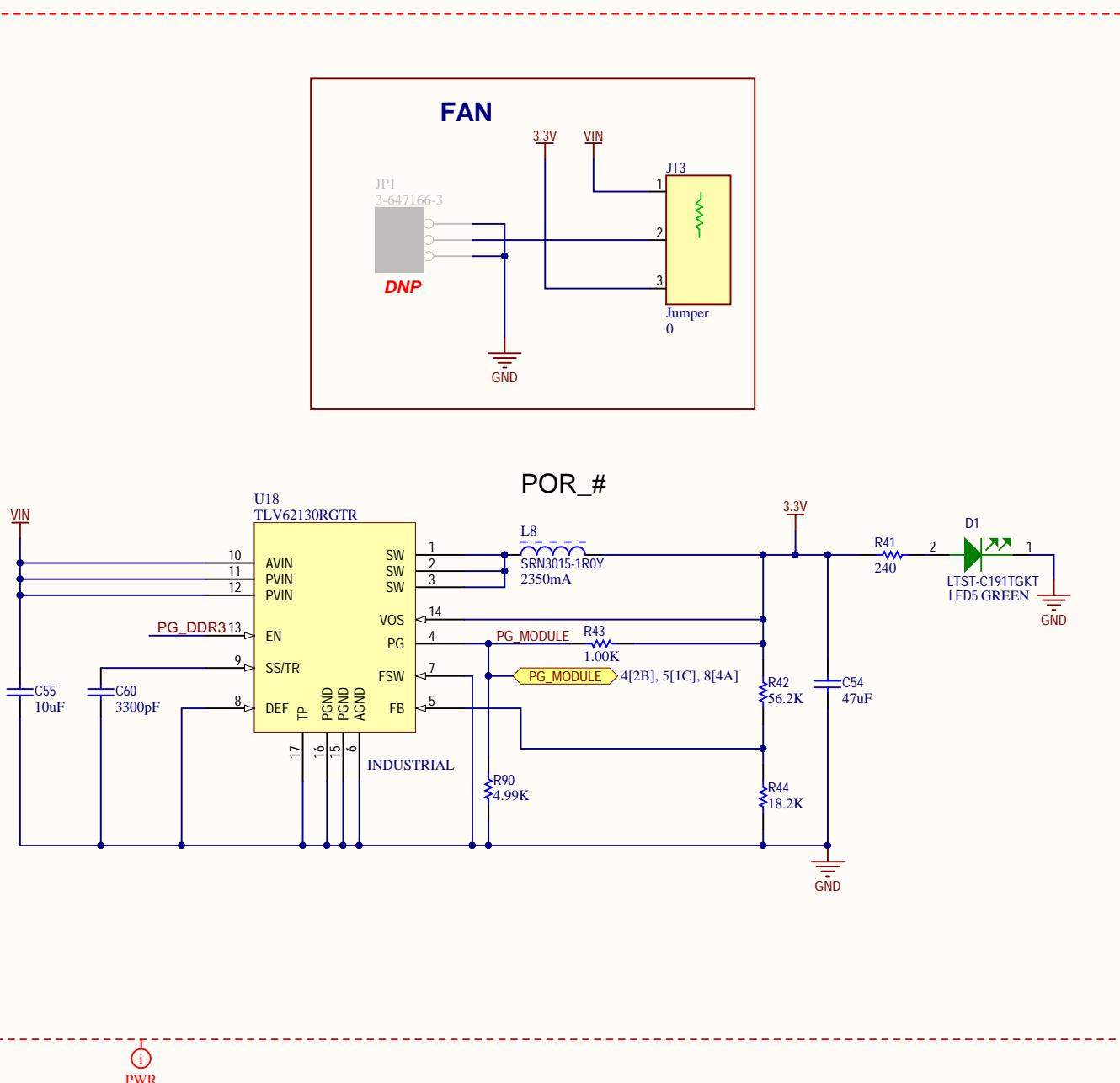
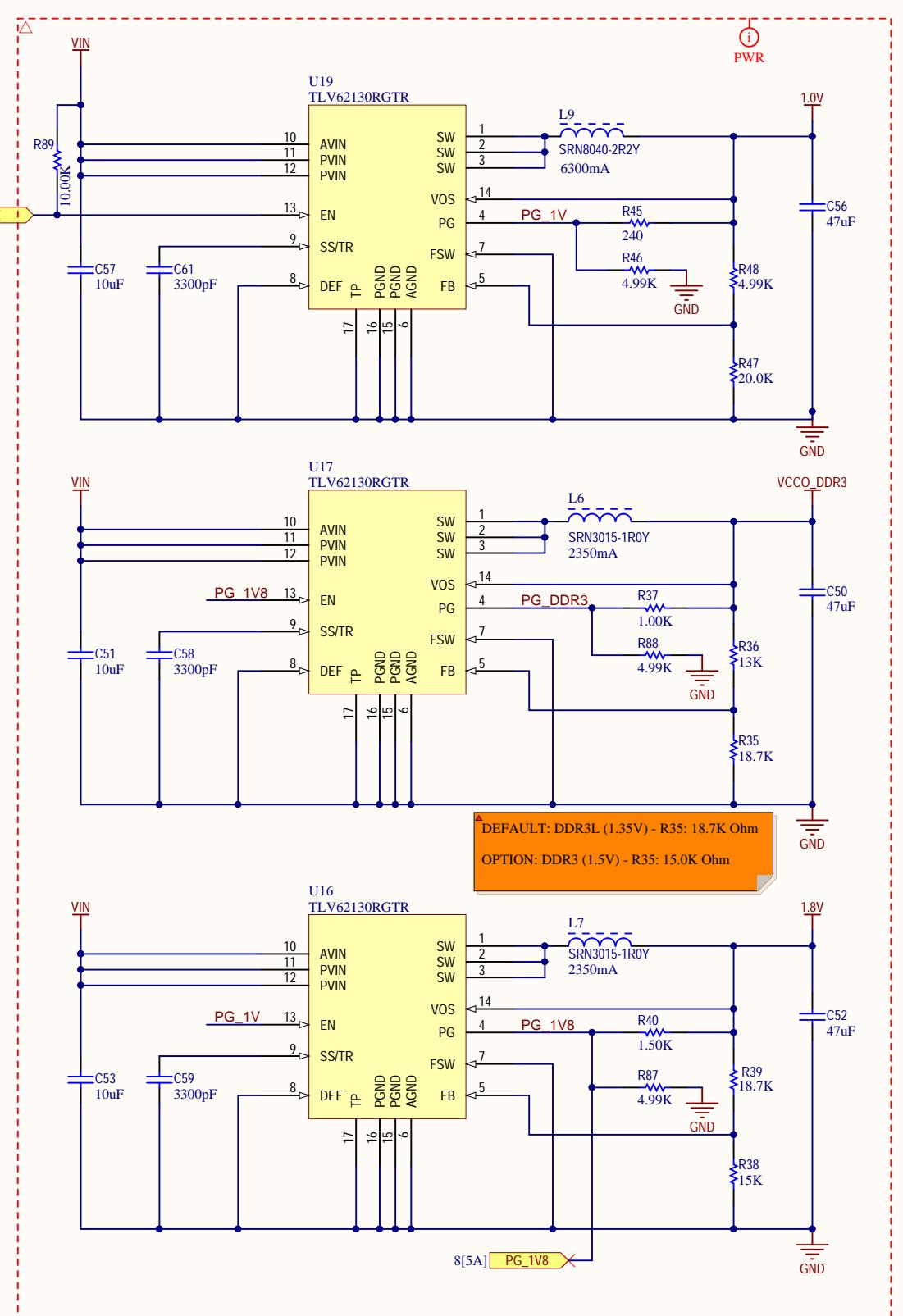
ZYNQ MIO POTENTIAL MAPPING OPTIONS:

SDIO INTERFACE
PS_MIO40 - SD_CLK through a 40.2-ohm RES
PS_MIO41 - SD_CMD
PS_MIO42 - SD_D0
PS_MIO43 - SD_D1
PS_MIO44 - SD_D2
PS_MIO45 - SD_D3
PS_MIO46 - SD_CD
UART INTERFACE
PS_MIO48 - UART_RXD (Tie to the TXD pin of a UART)
PS_MIO49 - UART TXD (Tie to the RXD pin of a UART)
USB INTERFACE
PS_MIO40 - DATA
PS_MIO41 - DIR
PS_MIO42 - STP
PS_MIO43 - NXT
PS_MIO44 - DATA
PS_MIO45 - DATA
PS_MIO46 - DATA
PS_MIO47 - DATA
PS_MIO48 - CK
PS_MIO49 - DATA
PS_MIO50 - DATA

D

BANK13_LVDS_12_P/N thru BANK13_LVDS_16_P/N is reserved for larger density BANK13





Revision Notes:

PicoZed Revision B1:
 1) Multiplexed JX2 MIO signals with EMMC
 2) Removed Push Button Footprint
 3) Incorporated ETHERNET RESET circuit
 4) Added bulk cap to AVDD18
 5) Added GND Testpoints

PicoZed Revision B2:
 1) Updated BOOT MODE table

PicoZed Revision C:
 1) Updated Block Diagram
 2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
 3) Added RC time constant to ETHERNET RESET
 4) DDR3L / DDR3 Option Added
 5) Modified resistor divider value on PG_1V8
 6) Changed DDR3 Termination Regulator VLDOIN from 1.8V to 3.3V

PicoZed Revision C (Errata):
 1) R71: Changed to 4.99K
 2) R182: Changed to 0.1uF

PicoZed Revision D:
 U1, U2, JT1, JT2, and JT6 have been removed
 U3, U6, and U15 part numbers changed
 Moved U12, R15, C12,C19, and C20 away from FPGA to allow for heatsink clearance
 JT8 and JT9 added to allow Boot Mode to be hard wired with 0 Ohm Jumpers
 JT6 Replaced with 4.99K Pulldown resistor

PicoZed Revision E:
 Connected U6 Pin B3 to GND
 Added Voltage Divider (R94, R95) and filter cap (C62) to U15 "VRI" pin
 Added C183 and C184 to U15 Pin 3/5 (DDR3_VTT)
 Added C63 to U15 Pin 2 (PVcc)
 Changed C47 to 0.1uF Cap
 Changed C171 to 4.7uF Cap

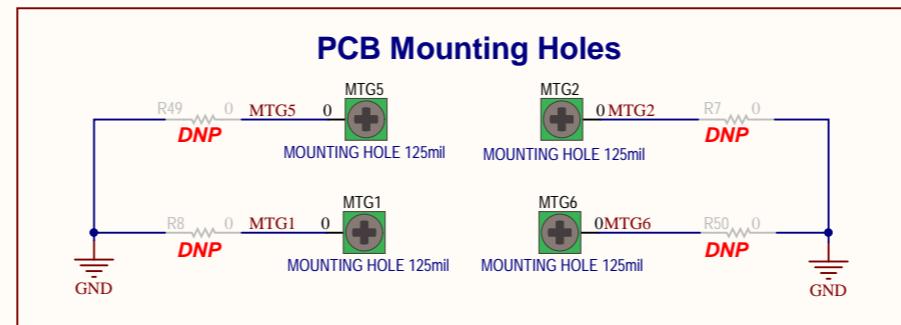
Mechanicals:



PCB

XXX-XXX-PCB-X

PCB PN (In Copper)



Assembly:

Label1
RD-XXXX-XXXXX-G
Label, Product

Label2
XXXXXXX
Label, Serial Number



Label, ESD



Avnet Engineering Services			
Project Name:	Picozed 7010/7020 SOM	PCB Rev:	E 01 01
Doc Num:	SCH-PZ1SOM	Date:	12/18/2017 Time: 11:11:36 AM
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