RTL8366/8369 & RTL8212

6/9-PORT 10/100/1000MBPS SWITCH CONTROLLER and 10/100/1000 DUAL ETHERNET TRANSCEIVER

LAYOUT GUIDE

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REVISION HISTORY

Revision	Release Date	Summary
1.0	2005/08/11	First release.
1.1	2005/08/29	Change all model numbers RTL8365 to RTL8366. Add RREF and MDI_REF pin design rule (See section 2.1 General Guidelines, page 5).

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1. General Description

This document provides detailed design and layout guidelines to achieve the best performance when implementing a 4-layer board design with the RTL8366/8369 10/100/1000Mbps switch controller, and the RTL8212 dual port 10/100/1000Mbps Ethernet transceiver.

The RTL8366 and RTL8369 are 128-pin, ultra-low-power, high-performance 5/8-port Gigabit Ethernet switches, with one extra GMII/MII/RGMII port for specific applications. They integrate all the functions of a high speed switch system; including SRAM for packet buffering, non-blocking switch fabric, internal register management, and an embedded 8051 into a single 0.15µm CMOS device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

The 6/9th port of the RTL8366/8369 implements a GMII/MII/RGMII interface for connecting with an external PHY or MAC in specific applications. This interface could be connected to an external CPU or RISC in 1 WAN + 4 LAN or 1 WAN + 8 LAN Router applications.

The RTL8212 integrates dual independent Gigabit Ethernet transceivers into a single 0.13µm CMOS device and includes the PCS, PMA, and PMD sub-layers. They perform encoding/decoding, clock/data recovery, digital adaptive equalization, echo cancellers, cross-talk elimination, line driver, as well as all other required support circuit functions.

2. General Design and Layout

In order to achieve maximum performance with the RTL8366/8369 and RTL8212, good design attention is required throughout the design and layout process. The following recommendations will help implement a high performance system.

2.1. General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<100mV).
- Verify the critical components, such as clock source and transformer, to meet the application requirements.
- Keep power and ground noise levels below 100mV.
- Use bulk capacitors (4.7uF-10uF) between each power and ground plane.
- Use 0.1uF decoupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep decoupling capacitors as close as possible to the RTL8366/8369 and RTL8212.
- Fill in unused areas of component side and solder side with solid copper and attach them with vias to ground plane.
- The RREF pin of the RTL8366/8369 and the MDI_REF pin of the RTL8212 must connect to GND via a 2.49K +/- 1% Ohm resister. This resister must be placed as close as possible to the RTL8366/8369 and RTL8212.

3. RSGMII PCB Layout Guidelines

As the RSGMII transmits over 2.5GHz differential signal pairs, the PCB layout needs some attention in order to meet layout guidelines. The following lists some important guidelines for layout of the RSGMII in a 4-layer PCB.

- Differential impedance is 100Ω±10% and single-ended impedance is 60Ω±6%.
- All micro-strip traces of a differential pair should be 5-mil-wide with 7-mil-wide air-gap spacing between the traces of the pair.
- Spacing to all non-Serdes signals should be at least 30-mil in order to avoid harmful coupling issues.
- Trace routes over long distances should be routed at an off-angle to the X-Y axis of a PCB layer to distribute the effects of fiberglass bundle weaves and resin-rich areas of the dielectric. See Figure 1 for an illustration of diagonal routing.

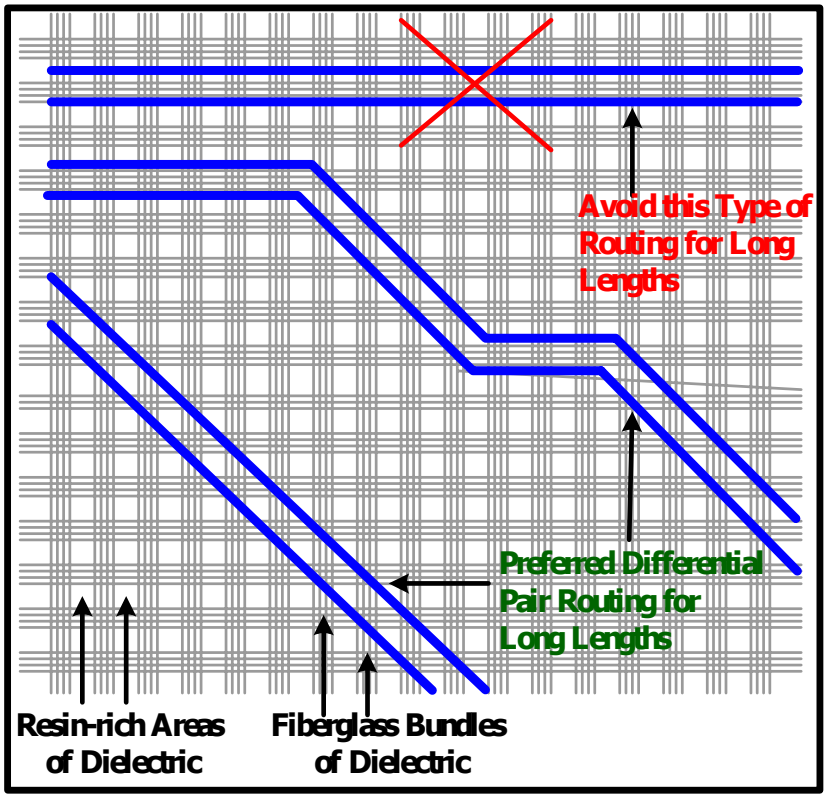

Figure 1. Long Trace Layout for RSGMII

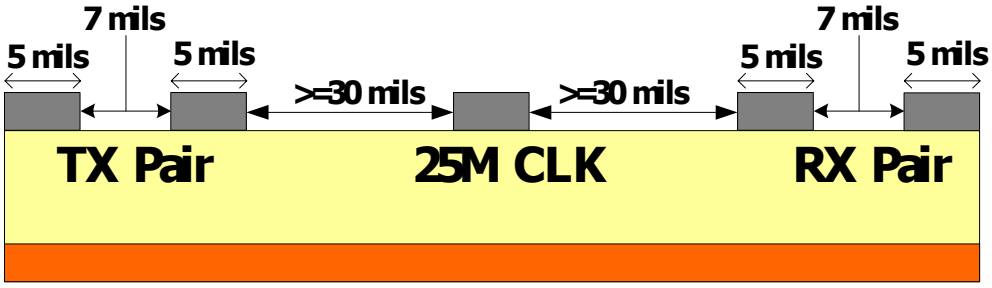

Figure 2. Trace Width and Spacing Recommendation for Microstrip

- Differential pairs should maintain symmetry between the two signals of a differential pair whenever possible.

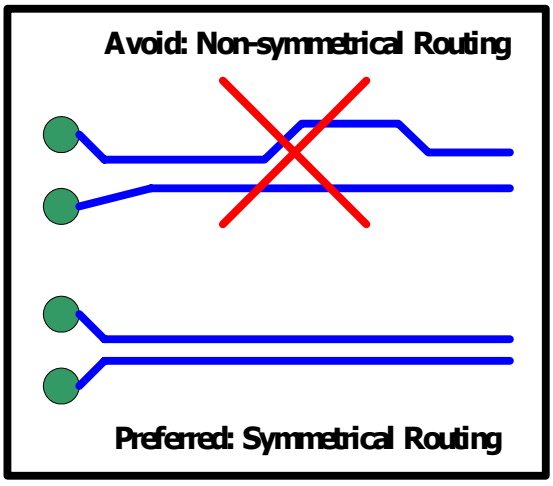

Figure 3. Symmetrical Routing

- Keep differential pair routing lengths as short as possible.
- Match the length of both sets of the differential pairs, allowing no more than a 5-mil delta between the lengths of the two signals.
- Length matching should occur on a segment-by-segment basis vs. across the total distance of the overall route.
- Differential pairs should have a continuous reference plane, and avoid vias.
- Size 0402 AC coupling capacitors are strongly encouraged as the smaller the package size, the less ESL.
- Place AC coupling capacitors near output pins of differential pairs.
- Locate capacitors for coupled traces at the same location along the differential traces and near output pins of differential pairs.

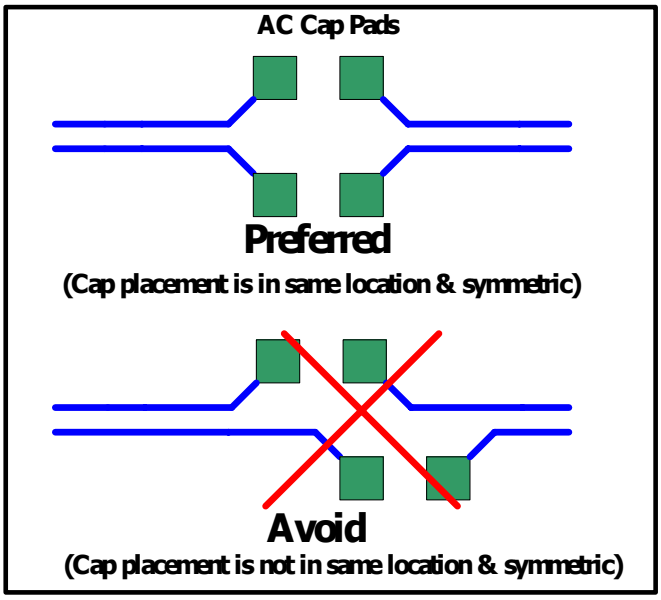

Figure 4. Symmetrical Routing Into AC Caps

- RSGMII layout reference is shown in Figure 5.

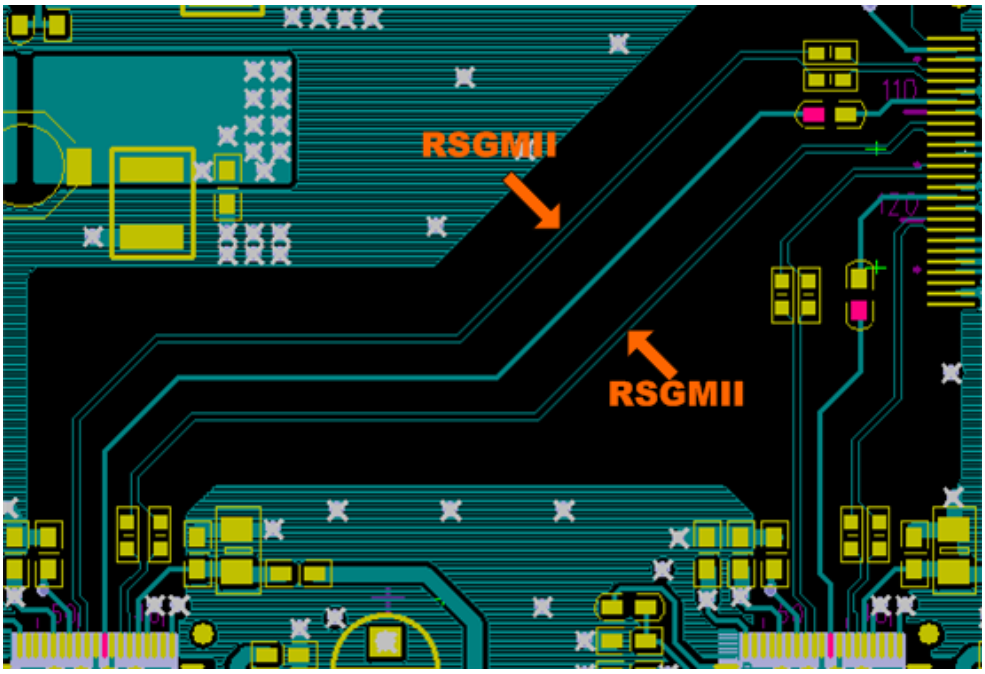

Figure 5. RSGMII Layout Reference

3.1. Ethernet MDI Differential Signals

- Keep differential-pair impedance at 100Ω±10%, single-ended impedance at 60Ω±6%.
- All microstrip traces of a differential pair should be 5-mil wide with a 7-mil wide air gap spacing between the trace of the pair.
- Keep differential pairs as close as possible and route both traces as identically as possible, meaning width, length, and location.
- Avoid vias and layer change if possible.
- MDI Differential layout reference is show in Figure 6.

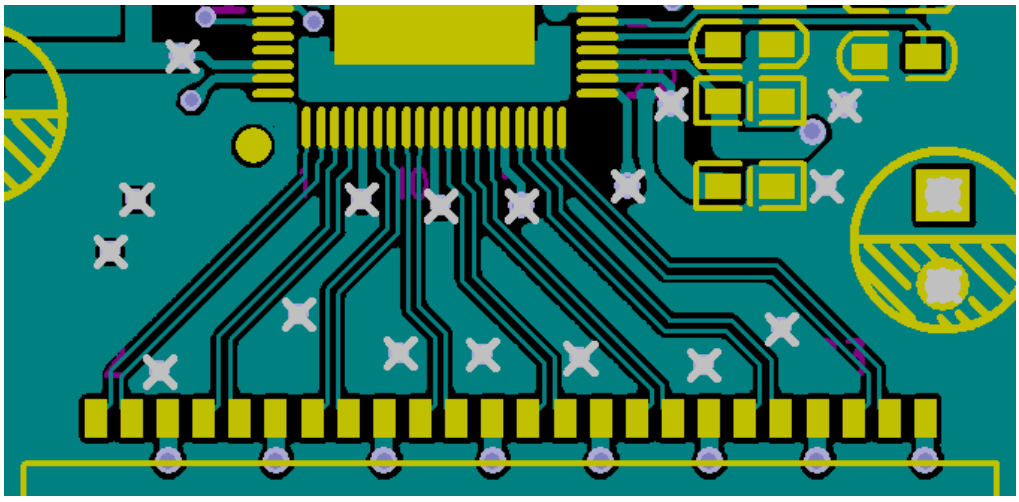

Figure 6. MDI Differential Layout Reference

3.2. RTL8212 Layout Note

- Separate Serdes ground (AVSS pin46, pin48) and system ground by a bead (size= 0603). See Figure 7.

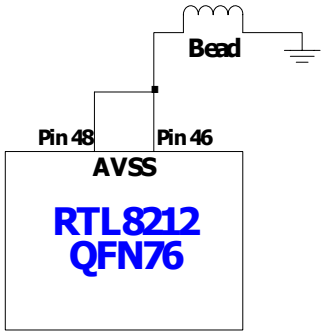

Figure 7. Separate Serdes GND and System GND via a Bead

- Use multi-vias (drill size= 20~24 mil) in the RTL8212 footprint and fill in large areas of component side and solder side with solid copper. Then attach them with vias to the ground plane in order to reduce the temperature of the PCB.
- The following figures are examples of an RTL8212 footprint.

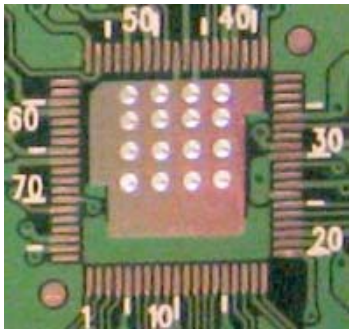

Figure 8. RTL8212 Component Side Footprint

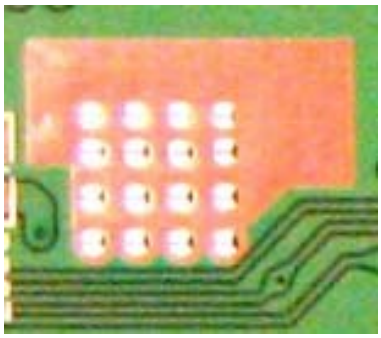

Figure 9. RTL8212 Solder Side Footprint

3.3. Clock Circuit

- Place the crystal as close to the RTL8366/8369 as possible.
- Surround the clock with ground trace to minimize high-frequency emissions.
- Use only one 1.5K pull up external resistance to 3.3V for MDIO.
- Keep the MDC trace away from the other signals, to avoid unnecessary interference.
- Keep clearance area under the crystal or OSC component.
- Don't let the clock trace pass over a gap in the ground plane.

3.4. Power Planes

- When designing a 4-layer PCB layout, divide the power plane into 3.3V_MAC, 3.3V_PHY, 1.8V and 1.2V.
- Use 0.1μF decoupling capacitors and bulk capacitors between each power plane and ground plane.

3.5. Ground Planes

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.
- Ensure the chassis ground area is voided at some point such that no ground loop exists on the chassis ground area.

4. Transformer Options

- The RTL8212 uses a transformer with a 1:1 turn ratio. There are many venders offering transformer designs that meet the RTL8212's requirement. Examples are Pulse H5014, Bothhand GS5014, and Lankom LG4803S.
- A 10/100/1000Base-T UTP application circuit with transformer is show in Figure 10.

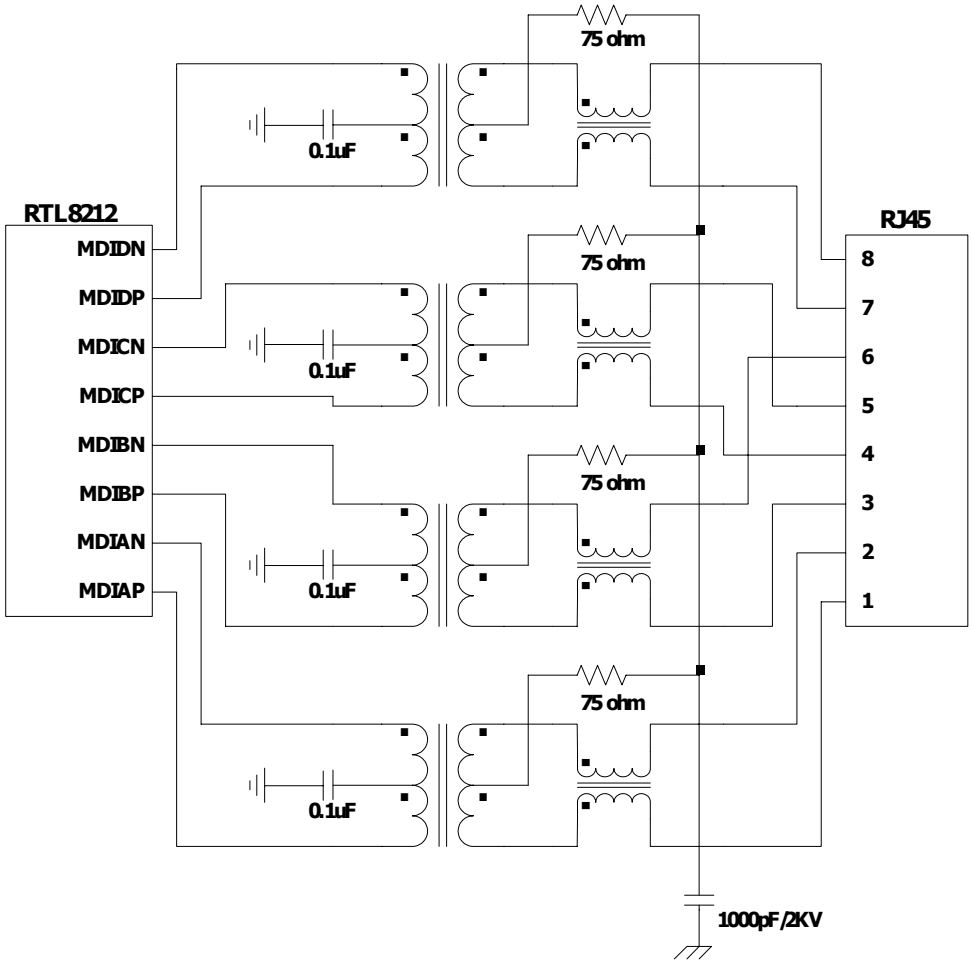

Figure 10. UTP Application Circuit with Transformer

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