Technical Note

Migrating from Winbond's W25Q to Micron's MT25Q

Introduction

This technical note describes the process for converting a system design from the Winbond W25Q to the Micron® MT25Q Flash memory device. Features compared include memory organization, package options, signal descriptions, the software command set, electrical specifications and device identification.

This document is written based on device information available at the time of publication. In case of inconsistency, information contained in the relevant MT25Q data sheet supersedes the information in this technical note. This technical note does not provide detailed device information. The standard density-specific device data sheet provides a complete description of device functionality, operating modes and specifications.

General Feature Differences

Table 1: Feature Differences

Features	W25Q	MT25Q
Densities monolithic	128Mb–256Mb	128Mb–512Mb
Densities stacked	512Mb (2 stack)	1Gb (2 stack), 2Gb (4 stack)
Voltage range	1.65–1.95V[1] 2.7–3.6V	1.7–2.0 V 2.7–3.6 V
Program	1 to 256 bytes	1 to 256 bytes
Sector architecture	Uniform sector (64KB)	Uniform sector (64KB)
Subsector	Uniform subsector (4KB, 32KB)	Uniform subsector (4KB, 32KB)
Endurance	100,000 cycle	100,000 cycle
Retention	20 years	20 years
Industrial temperature range	–40 to +85°C	–40 to +85°C
Automotive temperature range	N/A	–40 to +105°C

Note: 1. For the W25Q, 1.8V is only available on the 128Mb device.

Package Configurations

Table 2: Package Configurations

Package	Shorted name	W25Q	MT25Q	Notes
8-pin SOP2, 208 mil	SO8W	Yes	Yes	1
16-pin SOP2, 300 mil	SO16W	Yes	Yes	
24-ball T-PBGA, 05/6mm x 8mm (5 x 5 array)	T-PBGA 24	Yes	Yes	
24-ball T-PBGA, 05/6mm x 8mm (4 x 6 array)	T-PBGA 24	Yes	Yes	
W-PDFN-8 6mm x 5mm (MLP8 6mm x 5mm)	WDFN/6x5	No	Yes	
W-PDFN-8 8mm x 6mm (MLP8 8mm x 6mm)	WDFN/8x6	Yes	Yes	
Wafer level chip-scale package (WLCSP)	XFWLBGA 0.5P	Yes	Yes	2

Notes: 1. Only for the 128Mb density.
2. Only for 1.8V.

Signal Descriptions

Table 3: Signal Differences

W25Q Signal	MT25Q Signal	Type	Description	Notes
/CS	S#	Input	Chip select	
CLK	C	Input	Serial clock	
/WP	W#	Input	Write protect	1
/HOLD	HOLD#	Input	HOLD	2
/RESET	RESET#	Input	Reset	3
IO[3:0]	DQ[3:0]	I/O	Serial data input or output	
V_{CC}	V_{CC}	Supply	Core and I/O power supply	
GND	V_{SS}	Supply	Core and I/O ground connection	

Notes:
1. Signal shared with DQ2.
2. Signal shared with DQ3.
3. For MT25Q devices in BGA24 and SO16 packages, a dedicated RESET# pin is available for every memory size (selected MPN). The RESET# signal has an internal pull-up resistor and may be left unconnected if not used.

Commands, Transfer Rate and Protocol

Table 4: Command Set Differences

Command	Command Code	
	W25Q	MT25Q
READ ID	9Fh	9Eh/9Fh
MULTIPLE I/O READ ID	N/A	AFh
DTR DUAL OUTPUT FAST READ	N/A	3Dh
DTR QUAD OUTPUT FAST READ	N/A	6Dh
4-BYTE DTR DUAL INPUT/OUTPUT FAST READ	N/A	BEh
4-BYTE DTR QUAD INPUT/ OUTPUT FAST READ	N/A	EEh
READ NONVOLATILE CONFIGURATION REGISTER	N/A	B5h
READ VOLATILE CONFIGURATION REGISTER	N/A	85h
READ ENHANCED VOLATILE CONFIGURATION REGISTER	N/A	65h
READ GENERAL PURPOSE READ REGISTER	N/A	96h
WRITE NONVOLATILE CONFIGURATION REGISTER	N/A	B1h
WRITE VOLATILE CONFIGURATION REGISTER	N/A	81h
WRITE ENHANCED VOLATILE CONFIGURATION REGISTER	N/A	61h
CLEAR FLAG STATUS REGISTER	N/A	50h
DUAL INPUT FAST PROGRAM	N/A	A2h
EXTENDED DUAL INPUT FAST PROGRAM	N/A	D2h
EXTENDED QUAD INPUT FAST PROGRAM	N/A	38h
4-BYTE QUAD INPUT EXTENDED FAST PROGRAM	N/A	3Eh
READ OTP ARRAY	N/A	4Bh
PROGRAM OTP ARRAY	N/A	42h
ENTER QUAD INPUT/OUTPUT MODE	N/A	35h
RESET QUAD INPUT/OUTPUT MODE	N/A	F5h
READ SECTOR PROTECTION	N/A	2Dh
PROGRAM SECTOR PROTECTION	N/A	2Ch
READ VOLATILE LOCK BITS	N/A	E8h
WRITE VOLATILE LOCK BITS	N/A	E5h
READ NONVOLATILE LOCK BITS	N/A	E2h
WRITE NONVOLATILE LOCK BITS	N/A	E3h
ERASE NONVOLATILE LOCK BITS	N/A	E4h
READ GLOBAL FREEZE BIT	N/A	A7h
WRITE GLOBAL FREEZE BIT	N/A	A6h
READ PASSWORD	N/A	27h
WRITE PASSWORD	N/A	28h
UNLOCK PASSWORD	N/A	29h
4-BYTE READ VOLATILE LOCK BITS	N/A	E0h
4-BYTE WRITE VOLATILE LOCK BITS	N/A	E1h

Table 4: Command Set Differences (Continued)

Command	Command Code	
	W25Q	MT25Q
INTERFACE ACTIVATION	N/A	9Bh
CYCLIC REDUNDANCY CHECK	N/A	9Bh/27h
WRITE ENABLE FOR VOLATILE STATUS REGISTER	50h	N/A
READ STATUS REGISTER 2	35h	N/A
WRITE STATUS REGISTER 2	31h	N/A
READ STATUS REGISTER 3	15h	N/A
WRITE STATUS REGISTER 3	11h	N/A
GLOBAL BLOCK LOCK	7Eh	N/A
GLOBAL BLOCK UNLOCK	98h	N/A
ENTER QPI MODE	38h	N/A
READ SECURITY REGISTER	48h	N/A
PROGRAM SECURITY REGISTER	42h	N/A
ERASE SECURITY REGISTER	44h	N/A
READ LOCK REGISTER	3Dh	N/A
INDIVIDUAL BLOCK LOCK	36h	N/A
INDIVIDUAL BLOCK UNLOCK	39h	N/A
READ UNIQUE ID	4Bh	N/A
Read Manufacturer / Device ID Dual I/O	92h	N/A
Read Manufacturer / Device ID QUAD I/O	94h	N/A
Octal Word Read Quad I/O	E3h	N/A
SET BURST WITH WRAP	77h	N/A

Note: 1. Only differences between device commands are included. See the W25Q and MT25Q data sheets for a complete list of commands.

Table 5: Different Commands Sharing Same Command Code

Command Code	W25Q Command	MT25Q Command
3Dh	READ LOCK REGISTER	DUAL OUTPUT FAST READ DTR
50h	WRITE ENABLE FOR VOLATILE STATUS REGISTER	CLEAR FLAG STATUS REGISTER
4Bh	READ UNIQUE ID	READ OTP ARRAY
42h	PROGRAM SECURITY REGISTER	PROGRAM OTP ARRAY
35h	READ STATUS REGISTER 2	ENTER QUAD
E3h	Octal Word Read Quad I/O	WRITE NONVOLATILE LOCK BITS
38h	Enter QPI Mode	EXTENDED QUAD INPUT FAST PROGRAM

Table 6: Transfer Rate, and Protocol Differences

STR/DTR	Protocol	Reading Pattern	W25Q	MT25Q
Single transfer rate (STR)	Extended SPI	READ, FASTREAD, DUAL OUTPUT FAST READ, QUAD OUTPUT FAST READ	Yes	Yes
	Dual input/output SPI	All dual input/output commands	Yes	Yes
	Quad input/output SPI	All quad input/output commands	Yes	Yes
Double transfer rate (DTR)	Extended SPI	DUAL OUTPUT FAST READ, QUAD OUTPUT FAST READ	Yes[1]	Yes[2]
	Dual input/output SPI	All dual input/output commands	Yes[1]	Yes[2]
	Quad input/output SPI	All quad input/output commands	Yes[1]	Yes[2]

Notes:
1. W25Q devices have DTR available only for selected 3V part numbers.
2. MT25Q devices have dedicated DTR commands available, as well as full DTR protocols that can be enabled by the relevant volatile or nonvolatile registers.

Command Considerations

The READ command set for the MT25Q and W25Q devices is identical, and each device follows the standard 3-byte address protocol. 4-byte addressing is also available to for memory sizes larger than 128Mb.

The W25Q has a fixed dummy cycle READ, but the MT25Q dummy cycles can be configured and controlled in the nonvolatile configuration register (NVCR), bits 12 to 15, or in the volatile configuration register (VCR), bits 7 to 4.

W25Q requires a nonvolatile quad-enable (QE) bit in status register 2 (SR2) to enable the quad I/O functionality; when the QE bit is set, the W and HOLD pins are disabled. VECR or NVCR enables the quad-SPI protocol (refer to the data sheet for more details). Quad commands are available without any register setting. When VECR or NVCR bits are set, W and HOLD are still functional. With NVCR set (bit 3 = 0), the device can be powered up or down with quad I/O functionality.

The W25Q and MT25Q manufacturer ID, memory type, and memory capacity can be read out by issuing a 9Fh command. MT25Q will output the same data when the 9Eh command is issued; the W25Q does not support the 9Eh command.

The W25Q has commands that output the memory capacity (ABh), memory type and capacity (90h), and additional READ commands, including OCTAL WORD READ QUAD I/ O (E3h) and CONTINUOUS READ MODE (FFh). MT25Q does not support ABh, 90h, E3h, or FFh commands.

The MT25Q also has dual I/O commands (A2h) that are not supported by the W25Q.

XIP Mode

The MT25Q device enters and exits execute-in-place (XIP) mode via the volatile and nonvolatile configuration registers settings. When enabled, XIP management in the MT25Q matches that of the W25Q XIP usage mode. Winbond uses one confirmation nibble to enter or exit XIP mode. The solution is fully compatible with the MT35Q XIP

methodology; other bits are "Don't Care." The table below compares XIP read configuration at power-on for both devices.

Table 7: XIP Mode

Protocol	W25Q	MT25Q
Fast read	N/A	Yes
Dual output fast read	N/A	Yes
Dual I/O fast read	Yes	Yes
Quad output fast read	N/A	Yes
Quad I/O fast read	Yes	Yes

Figure 1: XIP Timing

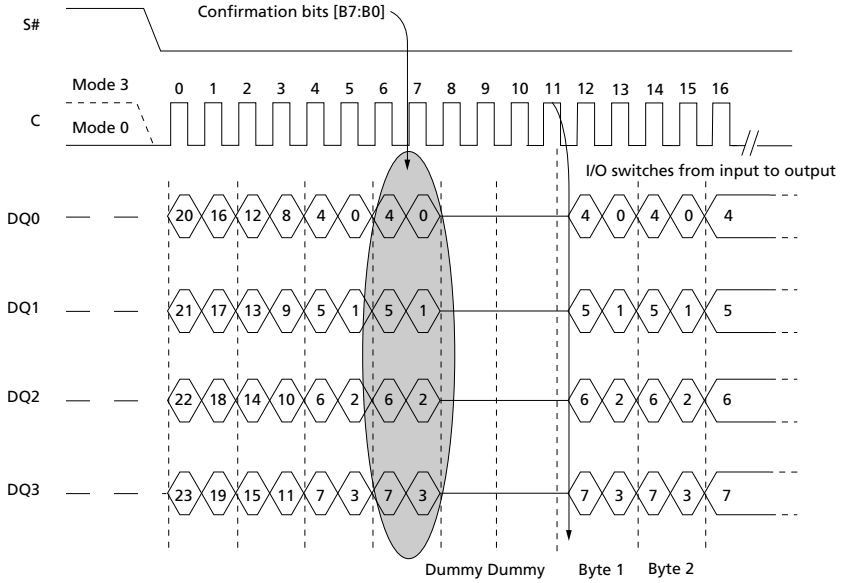

Table 8: XIP Confirmation Bit Software Commands

Description	W25Q	MT25Q
Enter/confirm XIP mode	B5–B4 = 1–0	B4 = 0 (B7.B5 and B3.B0 = "Don't Care")
Exit XIP mode	B5–B4 ≠ 1–0	B4 = 1 (B7.B5 and B3.B0 = "Don't Care")

Electrical Characteristics

Table 9: DC Characteristics – 1.8V (128Mb only)

Parameter	Symbol	Test Conditions	W25Q		MT25Q		Units	Note
			Typ	Max	Typ	Max		
Standby current	I_{CC1}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	10	50	12	50	µA	
Standby current (automotive)	I_{CC1}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	N/A	N/A	20	80	µA	
Deep power-down current	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	1	20	2	30	µA	
Deep power-down current (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	N/A	N/A	2	50	µA	
Operating current (fast-read extended I/O)	I_{CC3}	MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 166 MHz, DQ1 = open	N/A	N/A	–	20	mA	1
		C = 0.1V_{CC}/0.9V_{CC} at 54 MHz, DQ1 = open	N/A	N/A	–	8	mA	1
Operating current (fast-read dual I/O)	I_{CC3}	W25Q: C = 0.1V_{CC}/0.9V_{CC} at 104 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 166 MHz, DQ1 = open	–	20	–	25	mA	1
Operating current (fast-read quad I/O)	I_{CC3}	W25Q: C = 0.1V_{CC}/0.9V_{CC} at 104 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 166 MHz STR or 80 MHz DTR, DQ1 = open	–	20	–	28	mA	1
Operating current (fast-read quad I/O)	I_{CC3}	MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 90 MHz DTR, DQ1 = open	–	N/A	–	31	mA	1
Operating current (page program)	I_{CC4}	S# = V_{CC}	20	25	–	35	mA	
Operating current (write status register)	I_{CC5}	S# = V_{CC}	8	12	–	35	mA	
Operating current (erase)	I_{CC6}	S# = V_{CC}	20	25	–	35	mA	

Note: 1. Because of different frequencies in test conditions, the MT25Q device has a maximum operating current (I_{CC3}) slightly higher than the W25Q device.

Table 10: DC Characteristics – 3.0V

Parameter	Symbol	Test Conditions	W25Q		MT25Q		Units	Note
			Typ	Max	Typ	Max		
Standby current 128Mb	I_{CC1}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	10	60	15	50	µA	
Standby current 128Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	N/A	N/A	30	80	µA	
Standby current 256Mb	I_{CC1}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	10	60	30	75	µA	
Standby current 256Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	30	120	µA	
Standby current 512Mb	I_{CC1}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	20	120	30	100	µA	1
Standby current 512Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	N/A	30	200	µA	
Deep power-down current 128Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	1	20	5	30	µA	
Deep power-down current 128Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	50	µA	
Deep power-down current 256Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	1	20	5	35	µA	
Deep power-down current 256Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	80	µA	
Deep power-down current 512Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	2	40	5	50	µA	1
Deep power-down current 512Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	100	µA	
Operating current (fast-read extended I/O)	I_{CC3}	MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 133 MHz, DQ1 = open	–	N/A	–	20	mA	2
		C = 0.1V_{CC}/0.9V_{CC} at 54 MHz, DQ1 = open	–	N/A	–	8	mA	2
Operating current (fast-read dual I/O)	I_{CC3}	W25Q: C = 0.1V_{CC}/0.9V_{CC} at 104 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 133 MHz, DQ1 = open	–	20	–	25	mA	2
Operating current (fast-read quad I/O)	I_{CC3}	W25Q: C = 0.1V_{CC}/0.9V_{CC} at 104 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 133 MHz STR DQ1 = open	–	20	–	22	mA	2

Table 10: DC Characteristics – 3.0V (Continued)

Parameter	Symbol	Test Conditions	W25Q		MT25Q		Units	Note
			Typ	Max	Typ	Max		
Operating current (fast-read quad I/O)	I_{CC3}	MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 80 MHz DTR, DQ1 = open	–	N/A	–	28	mA	2
Operating current (fast-read quad I/O)	I_{CC3}	MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 90 MHz DTR, DQ1 = open	–	N/A	–	28	mA	2
Operating current (page program)	I_{CC4}	S# = V_{CC}	20	25	–	35	mA	
Operating current (write status register)	I_{CC5}	S# = V_{CC}	8	12	–	35	mA	
Operating current (erase)	I_{CC6}	S# = V_{CC}	20	25	–	35	mA	

Notes:
1. The W25Q device is stacked (2 × 256Mb).
2. Because of different frequencies in test conditions, the MT25Q device has a maximum operating current (I_{CC3}) slightly higher than the W25Q device.

Table 11: AC Specifications – 1.8V

Parameter	Symbol	Transfer Rate	W25Q		MT25Q		Units
			Min	Max	Min	Max	
Clock frequency for all commands other than READ (extended-SPI, DIO-SPI, and QIO-SPI protocols)	^{f}C	STR	DC	104	DC	166	MHz
		DTR	DC	N/A	DC	90	MHz
Clock frequency for READ commands	^{f}R	STR	DC	50	DC	54	MHz
		DTR	DC	N/A	DC	27	MHz
Clock HIGH time	^{t}CH	STR	4	–	2.7	–	ns
		DTR	N/A	–	5	–	ns
Clock LOW time	^{t}CL	STR	4	–	2.7	–	ns
		DTR	N/A	–	5	–	ns
Clock HIGH, LOW time for READ DATA (03h) instruction	$^{t}CRLH$	STR	8	–	2.7	–	ns
S# active setup time	$^{t}SLCH$	STR/DTR	5	–	2.7	–	ns
S# not active hold time (relative to clock)	$^{t}CHSL$	STR/DTR	5	–	2.7	–	ns
Data in setup time	$^{t}DVCH$	STR/DTR	2	–	1.75	–	ns
	$^{t}DVCL$	DTR only	–	–	1.75	–	ns
Data in hold time	$^{t}CHDX$	STR/DTR	3	–	2	–	ns
	$^{t}CLDX$	DTR only	3	–	2.75	–	ns
S# active hold time (relative to clock)	$^{t}CHSH$	STR	3	–	2.7	–	ns
		DTR	N/A	–	5	–	ns
S# active hold time (relative to clock LOW) Only for writes in DTR	$^{t}CLSH$	DTR only	N/A	–	3.375	–	ns
S# not active setup time (relative to clock)	$^{t}SHCH$	STR	3	–	2.7	–	ns
		DTR	N/A	–	5	–	ns
Output disable time	$^{t}SHQZ$	STR/DTR	–	7	–	6	ns
Clock LOW to output valid (under 30pF)	$^{t}CLQV$	STR/DTR	–	6	–	6	ns
Clock LOW to output valid (under 30pF)	$^{t}CHQV$	DTR only	–	N/A	–	6	ns
Output hold time (clock LOW)	$^{t}CLQX$	STR/DTR	2	-	1	–	ns
Output hold time (clock HIGH)	$^{t}CHQX$	DTR only	N/A	-	1	–	ns
HOLD setup time (relative to clock)	$^{t}HLCH$	STR/DTR	5	–	2.7	–	ns
HOLD hold time (relative to clock)	$^{t}CHHH$	STR/DTR	5	–	2.7	–	ns
HOLD setup time (relative to clock)	$^{t}HHCH$	STR/DTR	5	–	2.7	–	ns
HOLD hold time (relative to clock)	$^{t}CHHL$	STR/DTR	5	–	2.7	–	ns
HOLD to output Low-Z	$^{t}HHQX$	STR/DTR	–	7	–	5	ns
HOLD to output High-Z	$^{t}HLQZ$	STR/DTR	–	12	–	5	ns
Write protect setup time	$^{t}WHSL$	STR/DTR	20	–	20	–	ns
Write protect hold time	$^{t}SHWL$	STR/DTR	100	–	100	–	ns

Table 12: AC Specifications – 3.0V

Parameter	Symbol	Transfer Rate	W25Q		MT25Q		Units
			Min	Max	Min	Max	
Clock frequency for all commands other than READ (extended-SPI, DIO-SPI, and QIO-SPI protocols)	^{f}C	STR	DC	104	DC	133	MHz
		DTR	DC	66	DC	90	MHz
Clock frequency for READ commands	^{f}R	STR	DC	50	DC	54	MHz
		DTR	DC	N/A	DC	27	MHz
Clock HIGH time	^{t}CH	STR	4.3	–	3.375	–	ns
		DTR	6.8	–	5	–	ns
Clock LOW time	^{t}CL	STR	4.3	–	3.375	–	ns
		DTR	6.8	–	5	–	ns
S# active setup time	$^{t}SLCH$	STR/DTR	5	–	3.375	–	ns
S# not active hold time (relative to clock)	$^{t}CHSL$	STR/DTR	5	–	3.375	–	ns
Data in setup time	$^{t}DVCH$	STR	2	–	1.75	–	ns
		DTR	2	–	1.5	–	ns
	$^{t}DVCL$	DTR only	–	–	1.5	–	ns
Data in hold time	$^{t}CHDX$	STR/DTR	3	–	2.3	–	ns
	$^{t}CLDX$	DTR only	N/A	–	2.3	–	ns
S# active hold time (relative to clock)	$^{t}CHSH$	STR	3	–	3.375	–	ns
		DTR	N/A	–	5	–	ns
S# active hold time (relative to clock LOW) Only for writes in DTR	$^{t}CLSH$	DTR only	N/A	–	3.375	–	ns
S# not active setup time (relative to clock)	$^{t}SHCH$	STR	3	–	3.375	–	ns
		DTR	N/A	–	5	–	ns
Output disable time	$^{t}SHQZ$	STR/DTR	–	7	–	7	ns
Clock LOW to output valid (under 30pF)	$^{t}CLQV$	STR/DTR	–	6	–	6	ns
Clock LOW to output valid (under 30pF)	$^{t}CHQV$	DTR only	–	N/A	–	6	ns
Output hold time (clock LOW)	$^{t}CLQX$	STR/DTR	1.5	–	1.5	–	ns
Output hold time (clock HIGH)	$^{t}CHQX$	DTR only	N/A	–	1.5	–	ns
HOLD setup time (relative to clock)	$^{t}HLCH$	STR/DTR	5	–	3.375	–	ns
HOLD hold time (relative to clock)	$^{t}CHHH$	STR/DTR	5	–	3.375	–	ns
HOLD setup time (relative to clock)	$^{t}HHCH$	STR/DTR	5	–	3.375	–	ns
HOLD hold time (relative to clock)	$^{t}CHHL$	STR/DTR	5	–	3.375	–	ns
HOLD to output Low-Z	$^{t}HHQX$	STR/DTR	–	7	–	8	ns
HOLD to output High-Z	$^{t}HLQZ$	STR/DTR	–	12	–	8	ns
Write protect setup time	$^{t}WHSL$	STR/DTR	20	–	20	–	ns
Write protect hold time	$^{t}SHWL$	STR/DTR	100	–	100	–	ns

Table 13: WRITE Cycle, PROGRAM, ERASE Times – 1.8V

Parameter	Symbol	W25Q		MT25Q		Units
		Typ	Max	Typ	Max	
WRITE STATUS REGISTER cycle time	^{t}W	10	25	1.3	8	ms
PAGE PROGRAM (256 bytes)	^{t}PP	0.7	5	0.2	2.8	ms
64KB SECTOR ERASE	^{t}SE	0.15	2	0.15	1	s
4KB SECTOR ERASE	^{t}SSE	0.1	0.4	0.05	0.4	s
32KB SUBSECTOR ERASE	^{t}SSE	0.12	1.6	0.1	1	s
128Mb BULK ERASE	^{t}BE	40	200	38	114	s
256Mb BULK ERASE	^{t}BE	N/A	N/A	77	231	s

Table 14: WRITE Cycle, PROGRAM, ERASE Times – 3.0V

Parameter	Symbol	W25Q		MT25Q		Units
		Typ	Max	Typ	Max	
WRITE STATUS REGISTER cycle time	^{t}W	10	15	1.3	8	ms
PAGE PROGRAM (256 bytes)	^{t}PP	0.7	3	0.2	2.8	ms
64KB SECTOR ERASE	^{t}SE	0.15	2	0.15	1	s
4KB SECTOR ERASE	^{t}SSE	0.045	0.4	0.05	0.4	s
32KB SUBSECTOR ERASE	^{t}SSE	0.12	1.6	0.1	1	s
128Mb BULK ERASE	^{t}BE	40	200	38	114	s
256Mb BULK ERASE	^{t}BE	80	400	77	231	s
512Mb BULK ERASE [1]	^{t}BE	160	800	153	460	s

Note: 1. The W25Q device is stacked (2 × 256Mb).

Part Numbers

Table 15: Part Number Cross-Reference – 128Mb

W25Q Part Number	MT25Q Part Number	Package	Voltage	Auto	Note
W25Q128JVSIx	MT25QL128ABA1ESE-0SIT	SO8 Wide	2.7V–3.6V	No	
W25Q128FWSIx	MT25QU128ABA1ESE-0SIT	SO8 Wide	1.7V–2.0V	No	
W25Q128JVFIx	MT25QL128ABA8ESF-0SIT	SO16 Wide	2.7V–3.6V	No	1
N/A	MT25QL128ABA8ESF-0AAT	SO16 Wide	2.7V–3.6V	Yes	1
W25Q128FWFIx	MT25QU128ABA8ESF-0SIT	SO16 Wide	1.7V–2.0V	No	1
W25Q128JVBIx	MT25QL128ABA8E12-0SIT	T-PBGA	2.7V–3.6V	No	1
N/A	MT25QL128ABA8E12-0AAT	T-PBGA	2.7V–3.6V	Yes	1
W25Q128JVCIx	MT25QL128ABA8E14-0SIT	T-PBGA	2.7V–3.6V	No	
W25Q128FWBIx	MT25QU128ABA8E12-0SIT	T-PBGA	1.7V–2.0V	No	1
N/A	MT25QU128ABA8E12-0AAT	T-PBGA	1.7V–2.0V	Yes	
W25Q128FWCIx	MT25QU128ABA8E14-0SIT	T-PBGA	1.7V–2.0V	No	
N/A	MT25QU128ABA8E14-1SIT	T-PBGA	1.7V–2.0V	No	1
W25Q128JVPIx	MT25QL128ABA1EW7-0SIT	DFN-8	2.7V–3.6V	No	
W25Q128JVEIx	MT25QL128ABA1EW9-0SIT	DFN-8	2.7V–3.6V	No	
W25Q128FWPIx	MT25QU128ABA1EW7-0SIT	DFN-8	1.7V–2.0V	No	
W25Q128FWEIx	MT25QU128ABA1EW9-0SIT	DFN-8	1.7V–2.0V	No	
W25Q128FWYIx	MT25QU128ABA8E54-0SIT	XFWLBGA 0.5P	1.7V–2.0V	No	

Note: 1. MT25Q has a dedicated #RESET pin with internal pull-up resistor.

Table 16: Part Number Cross-Reference – 256Mb

W25Q Part Number	MT25Q Part Number	Package	Voltage[2]	Auto	Note
W25Q256JVFIx	MT25QL256ABA8ESF-0SIT	SO16 Wide	2.7V–3.6V	No	1
N/A	MT25QL256ABA8ESF-0AAT	SO16 Wide	2.7V–3.6V	Yes	1
W25Q256FJBIx	MT25QL256ABA8E12-0SIT	T-PBGA	2.7V–3.6V	No	1
W25Q256FJCI	MT25QL256ABA8E14-0SIT	T-PBGA	2.7V–3.6V	No	1
N/A	MT25QL256ABA8E12-0AAT	T-PBGA	2.7V–3.6V	Yes	1
W25Q256FJEIx	MT25QL256ABA1EW9-0SIT	DFN-8	2.7V–3.6V	No	
N/A	MT25QL256ABA1EW7-0SIT	PDIP	2.7V–3.6V	No	
N/A	MT25QL256ABA1EW9-0AAT	DFN-8	2.7V–3.6V	Yes	
W25Q256FJAI	N/A	DFN-8	2.7V–3.6V	No	

Notes: 1. The MT25Q has a dedicated #RESET pin with internal pull-up resistor.
2. The comparison is only for the 2.7V–3.6V voltage range, because the W25Q device doesn't have any product in the 1.7V–2.0V voltage range.

Table 17: Part Number Cross-Reference – 512Mb

W25Q Part Number	MT25Q Part Number	Package	Voltage[2]	Auto	Note
W25M512JVFIQ	MT25QL512ABB8ESF-0SIT	SO16 Wide	2.7V–3.6V	No	1
N/A	MT25QL512ABB8ESF-0AAT	SO16 Wide	2.7V–3.6V	Yes	1
W25M512JVBIQ	MT25QL512ABB8E12-0SIT	T-PBGA	2.7V–3.6V	No	1
N/A	MT25QL512ABB8E12-1SIT	T-PBGA	2.7V–3.6V	Yes	1
W25M512JVCIQ	MT25QL512ABB8E14-0SIT	T-PBGA	2.7V–3.6V	No	1
W25M512JVEIQ	MT25QL512ABB1EW9-0SIT	DFN-8	2.7V–3.6V	No	

Notes:
1. The MT25Q has a dedicated #RESET pin with internal pull-up resistor.
2. The comparison is only for the 2.7V–3.6V voltage range, because the W25Q device doesn't have any product in the 1.7V–2.0V voltage range. The W25Q device is stacked (2 × 256Mb).

Revision History

Rev. A – 03/17

- Initial release

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