GateMate™ FPGA

PHY Interface for the PCIe Architecture

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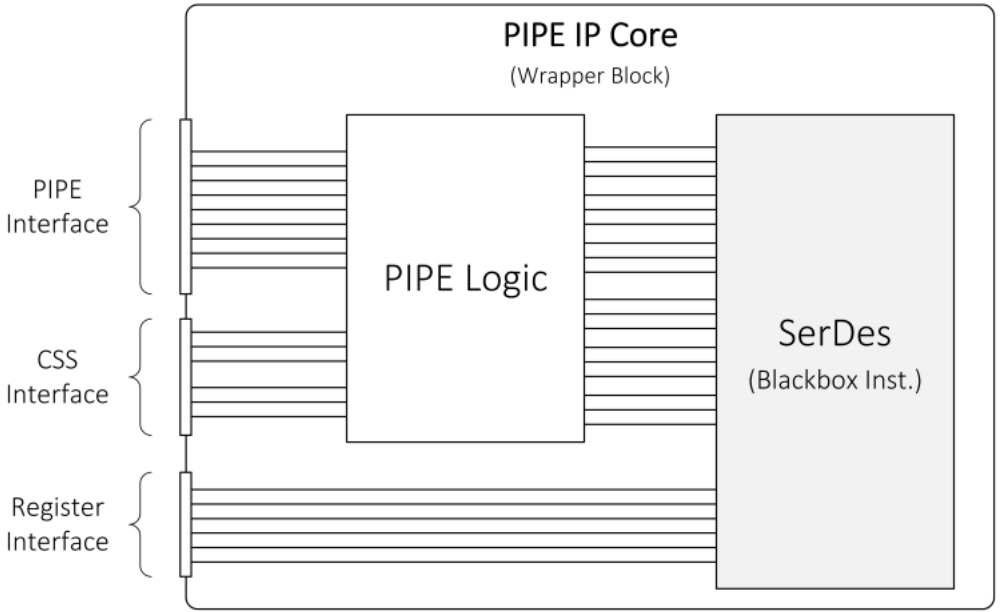
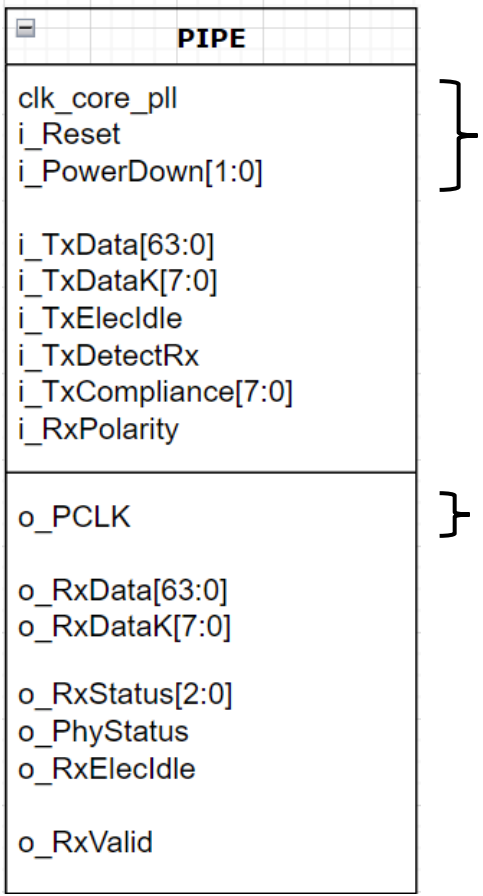
PIPE Overview



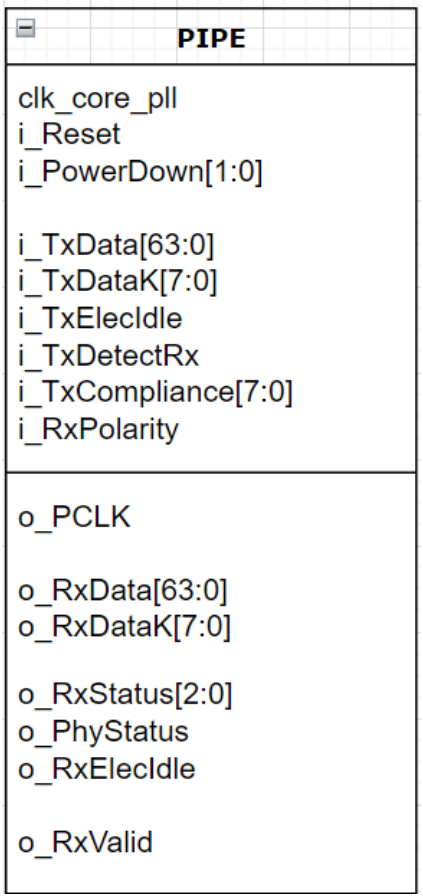
- PIPE Interface with MAC layer.
- Custom Support Signals (CSS) Interface for internal PIPE IP Core logic. These signals are mainly used for simulation purposes or to generate signals for PIPE Interface.
- Register interface for SerDes configuration.

PIPE Interface



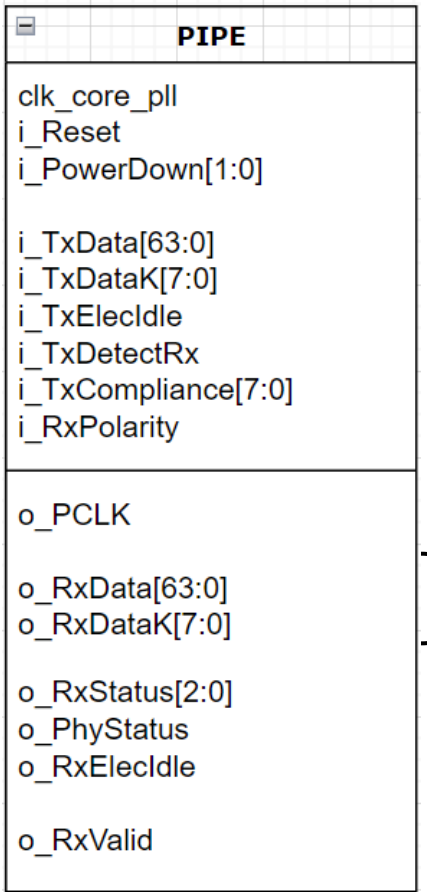
- Reference clock from ADPLL.
- Parallel Interface Clock for MAC and PHY synchronization.
- Asynchronous Reset for Transceiver.
- Power states.

PIPE Interface



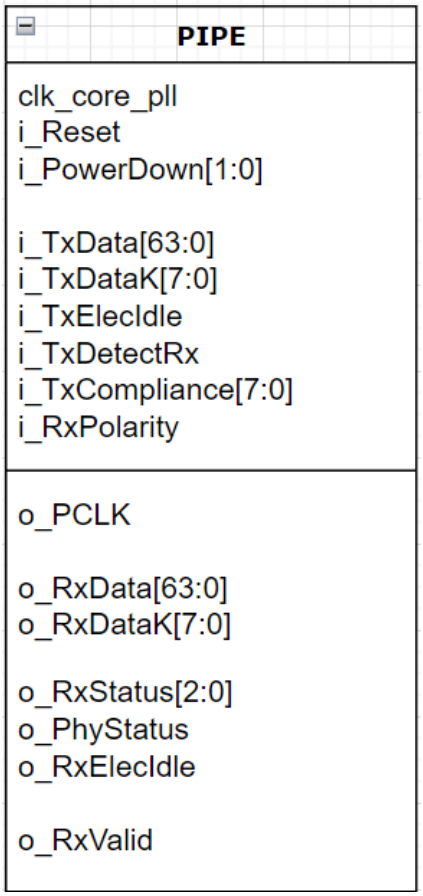
- Data from MAC for SerDes Transmitter.
- Control signals triggered by MAC layer.

PIPE Interface

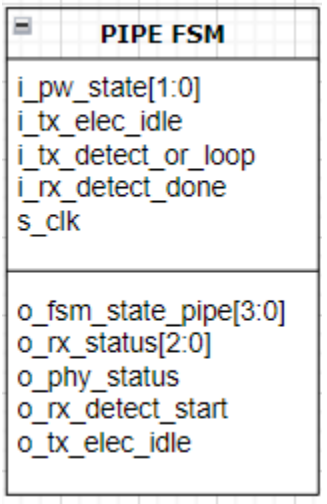


- Data from SerDes Receiver.

PIPE Interface

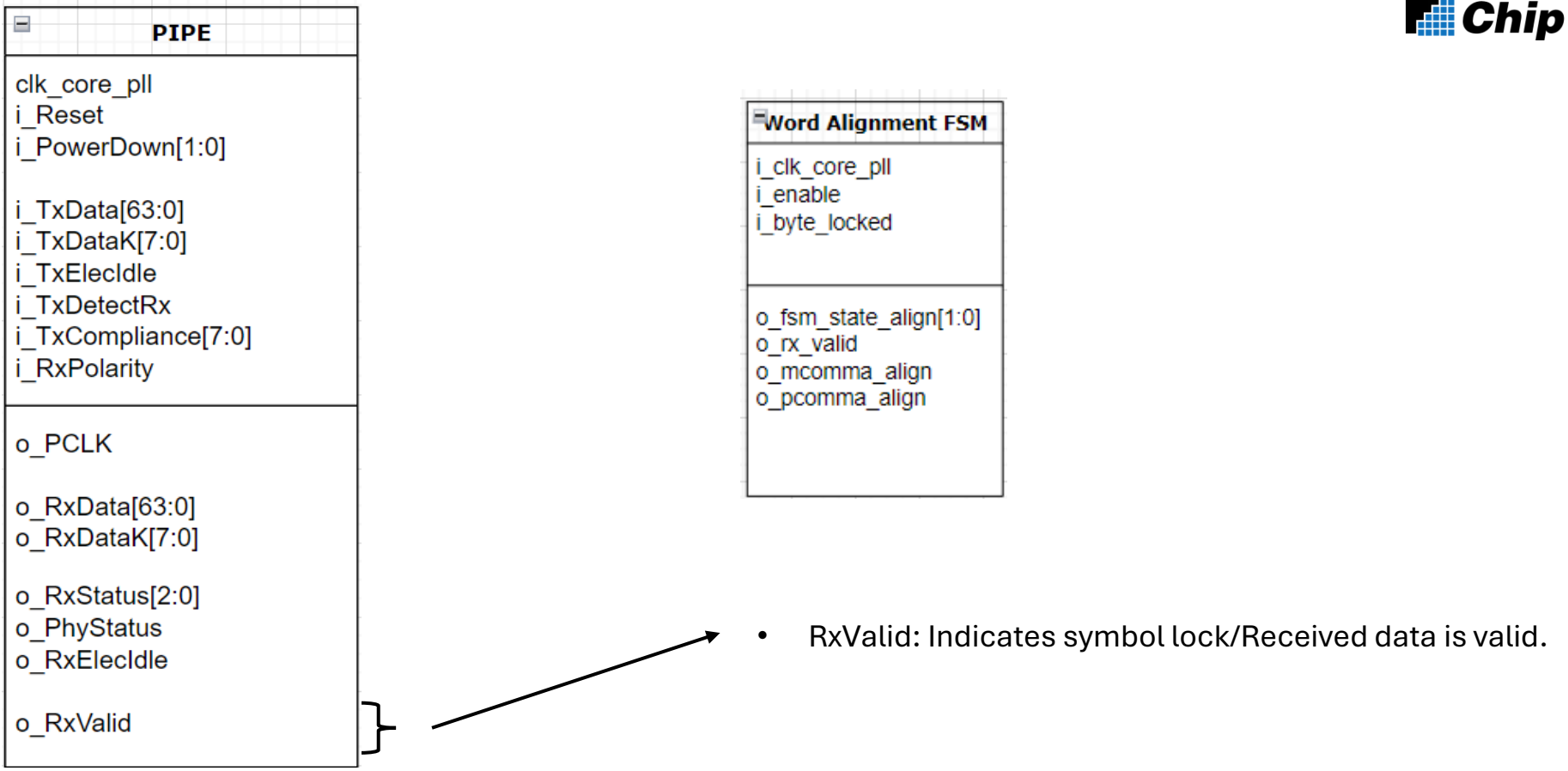


RxStatus	Description
000	Received Data OK (P0), Receiver not detected (P1)
001	SKP added
010	SKP removed
011	Receiver detected (P1)
100	8b/10b Error and optionally Disparity Error
101	Elastic Buffer Overflow
110	Elastic Buffer Underflow
111	Disparity Error. Unused if reported together with 8b/10b Error (100).



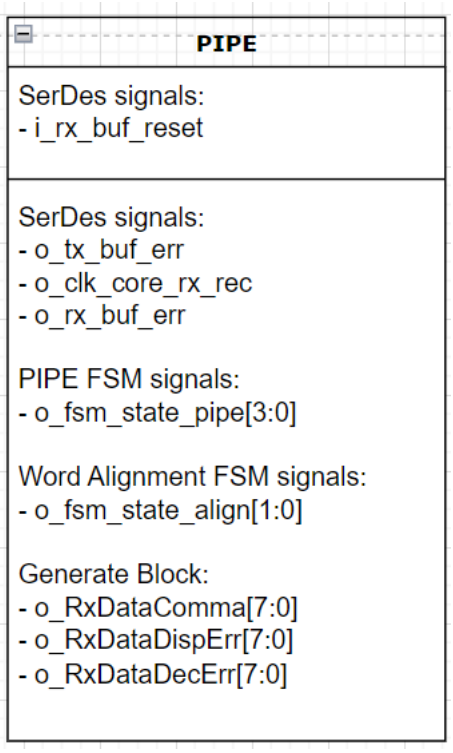
- RxStatus: Status of the received data.
- PhyStatus: Successful power state change or finished Receiver Detection.

PIPE Interface



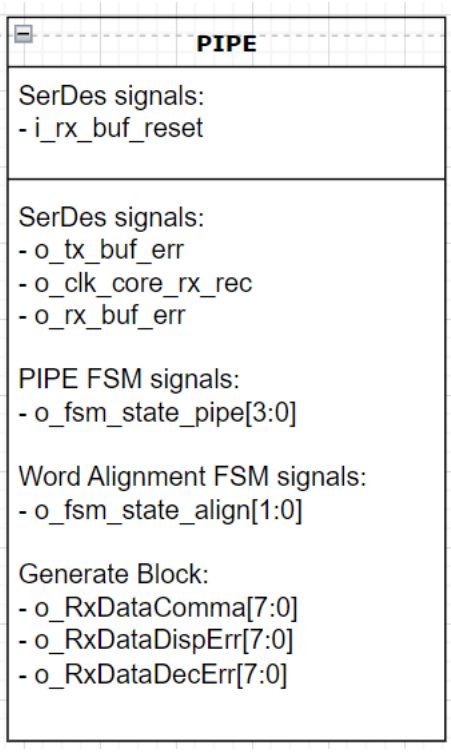
- RxValid: Indicates symbol lock/Received data is valid.

CSS Interface



- SerDes signals:
  - i_rx_buf_reset: trigger a reset for the elastic buffer.
  - o_tx_buf_err: Overflow or Underflow in Transmitter buffer.
  - o_clk_core_rx_rec: Recovered Clock from the received data.
  - o_rx_buf_err: Overflow or Underflow in Elastic Buffer of SerDes Receiver.

CSS Interface



- PIPE FSM:
  - o_fsm_state_pipe [3:0]: current state of the PIPE FSM.
- Word Alignment FSM:
  - o_fsm_state_align [1:0]: current state of the Word Alignment FSM.
- Generate Block: Module that has received and transmitted data along with their error flags as inputs and generate status signals accordingly.
  - o_RxDataComma [7:0]: Each bit represents if the symbol at that position is a COM or not.
  - o_RxDataDispErr [7:0]: Each bit represents if the symbol at that position has disparity error or not.
  - o_RxDataDecErr [7:0]: Each bit represents if the symbol at that position has 8b/10b Decode error or not.

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