

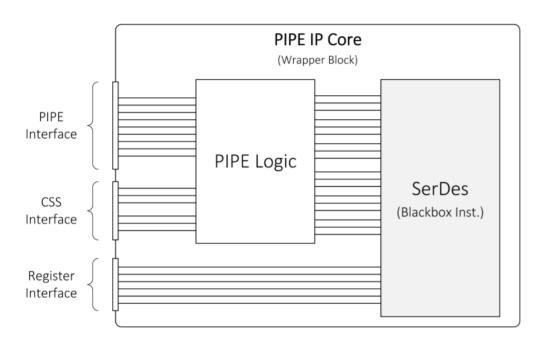
# **GateMate<sup>TM</sup> FPGA**PHY Interface for the PCIe Architecture

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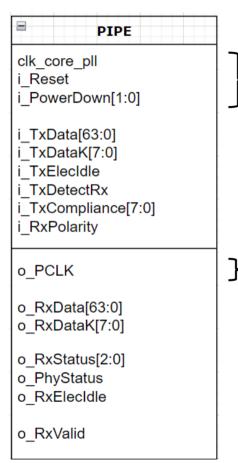
### PIPE Overview





- PIPE Interface with MAC layer.
- Custom Support Signals (CSS) Interface for internal PIPE IP Core logic. These signals are mainly used for simulation purposes or to generate signals for PIPE Interface.
- Register interface for SerDes configuration.



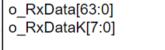


- Reference clock from ADPLL.
  - Parallel Interface Clock for MAC and PHY synchronization.
  - Asynchronous Reset for Transceiver.
  - Power states.



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PIPE	
clk_core_pll i_Reset i_PowerDown[1:0]	
i_TxData[63:0] i_TxDataK[7:0] i_TxElecIdle i_TxDetectRx i_TxCompliance[7:0] i_RxPolarity	
o_PCLK	

- Data from MAC for SerDes Transmitter.
- Control signals triggered by MAC layer.



- o\_RxStatus[2:0]
- o PhyStatus
- o RxElecIdle
- o\_RxValid

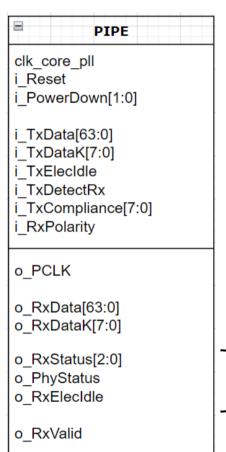




PIPE clk\_core\_pll i Reset i PowerDown[1:0] i TxData[63:0] i TxDataK[7:0] i TxElecIdle i TxDetectRx i\_TxCompliance[7:0] i RxPolarity o PCLK o\_RxData[63:0] o RxDataK[7:0] o\_RxStatus[2:0] o PhyStatus o RxElecIdle

o\_RxValid

• Data from SerDes Receiver.



RxStatus	Description
000	Received Data OK (P0), Receiver not detected (P1)
001	SKP added
010	SKP removed
011	Receiver detected (P1)
100	8b/10b Error and optionally Disparity Error
101	Elastic Buffer Overflow
110	Elastic Buffer Underflow
111	Disparity Error. Unused if reported together with 8b/10b Error (100).



PIPE FSM	
i_pw_state[1:0] i_tx_elec_idle i_tx_detect_or_loop i_rx_detect_done s_clk	
o_fsm_state_pipe[3:0] o_rx_status[2:0] o_phy_status o_rx_detect_start o_tx_elec_idle	

- RxStatus: Status of the received data.
- PhyStatus: Successful power state change or finished Receiver Detection.



PIPE
clk_core_pll i_Reset i_PowerDown[1:0]
i_TxData[63:0] i_TxDataK[7:0] i_TxElecIdle i_TxDetectRx i_TxCompliance[7:0] i_RxPolarity
o_PCLK
o_RxData[63:0] o_RxDataK[7:0]
o_RxStatus[2:0] o_PhyStatus o_RxElecIdle
o_RxValid

i\_clk\_core\_pll
i\_enable
i\_byte\_locked

o\_fsm\_state\_align[1:0]
o\_rx\_valid
o\_mcomma\_align
o\_pcomma\_align

RxValid: Indicates symbol lock/Received data is valid.

# **CSS** Interface



### PIPE

### SerDes signals:

i\_rx\_buf\_reset

#### SerDes signals:

- o\_tx\_buf\_err
- o clk core rx rec
- o\_rx\_buf\_err

#### PIPE FSM signals:

- o fsm state pipe[3:0]

#### Word Alignment FSM signals:

- o\_fsm\_state\_align[1:0]

#### Generate Block:

- o\_RxDataComma[7:0]
- o\_RxDataDispErr[7:0]
- o\_RxDataDecErr[7:0]

### SerDes signals:

- i\_rx\_buf\_reset: trigger a reset for the elastic buffer.
- o\_tx\_buf\_err: Overflow or Underflow in Transmitter buffer.
- o\_clk\_core\_rx\_rec: Recovered Clock from the received data.
- o\_rx\_buf\_err: Overflow or Underflow in Elastic Buffer of SerDes Receiver.

# **CSS** Interface



### PIPE

### SerDes signals:

i\_rx\_buf\_reset

#### SerDes signals:

- o\_tx\_buf\_err
- o\_clk\_core\_rx\_rec
- o\_rx\_buf\_err

#### PIPE FSM signals:

- o\_fsm\_state\_pipe[3:0]

#### Word Alignment FSM signals:

- o\_fsm\_state\_align[1:0]

#### Generate Block:

- o\_RxDataComma[7:0]
- o\_RxDataDispErr[7:0]
- o\_RxDataDecErr[7:0]

#### PIPF FSM:

- o\_fsm\_state\_pipe [3:0]: current state of the PIPE FSM.
- Word Alignment FSM:
  - o\_fsm\_state\_align [1:0]: current state of the Word Alignment FSM.
- Generate Block: Module that has received and transmitted data along with their error flags as inputs and generate status signals accordingly.
  - o\_RxDataComma [7:0]: Each bit represents if the symbol at that position is a COM or not.
  - o\_RxDataDispErr [7:0]: Each bit represents if the symbol at that position has disparity error or not.
  - o\_RxDataDecErr [7:0]: Each bit represents if the symbol at that position has 8b/10b Decode error or not.



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