GateMate™ FPGA

PHY Interface for the PCIe Architecture

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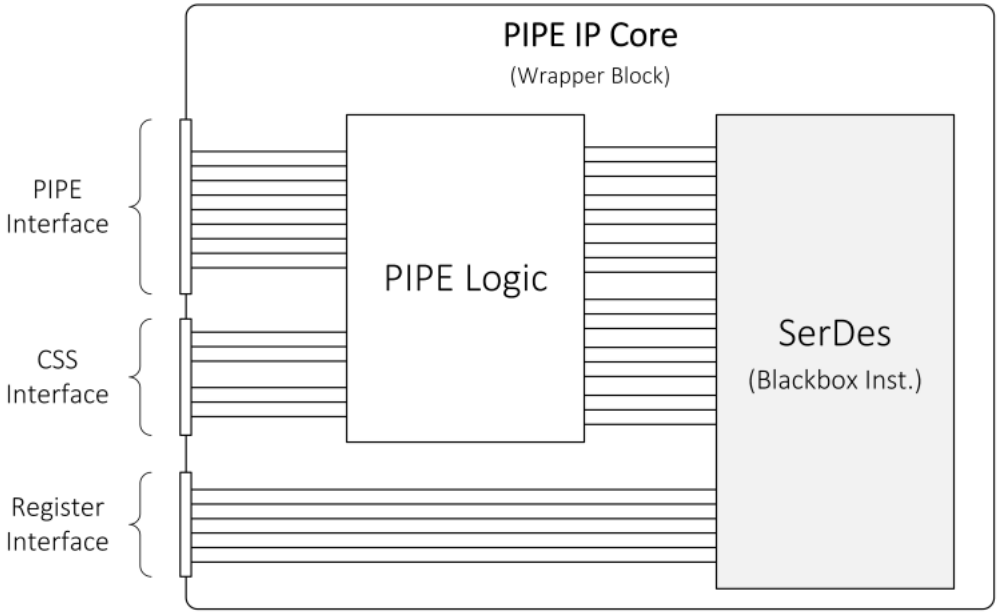
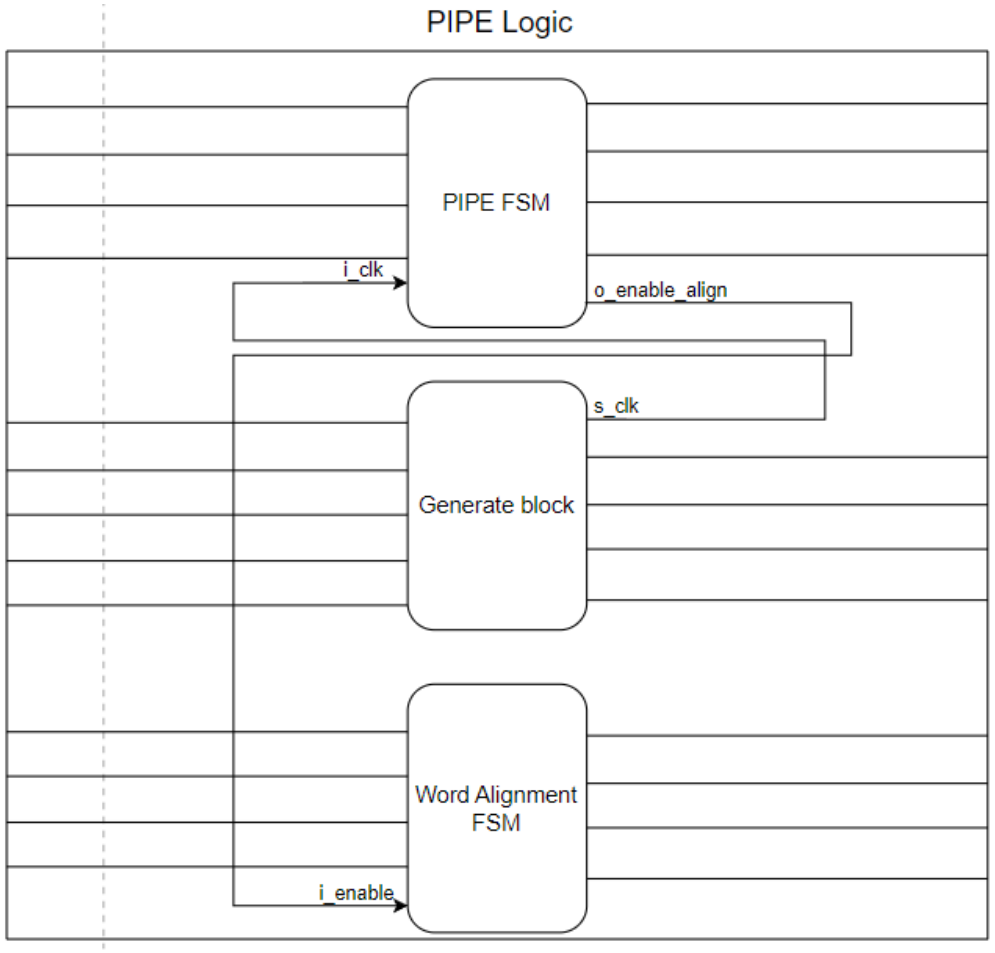
July 2025

PIPE Overview

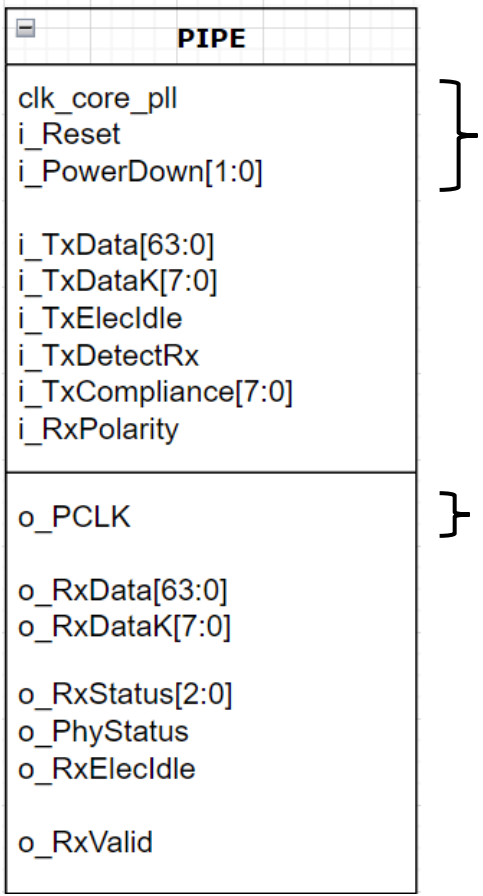


- PIPE Interface with MAC layer.
- Custom Support Signals (CSS) Interface for internal PIPE IP Core logic. These signals are mainly used for simulation purposes or to generate signals for PIPE Interface.
- Register interface for SerDes configuration.

General PIPE Logic Block diagram

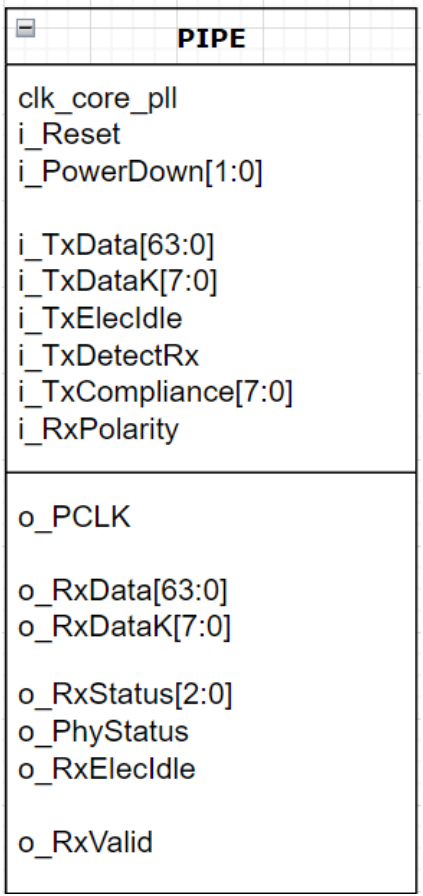


PIPE Interface



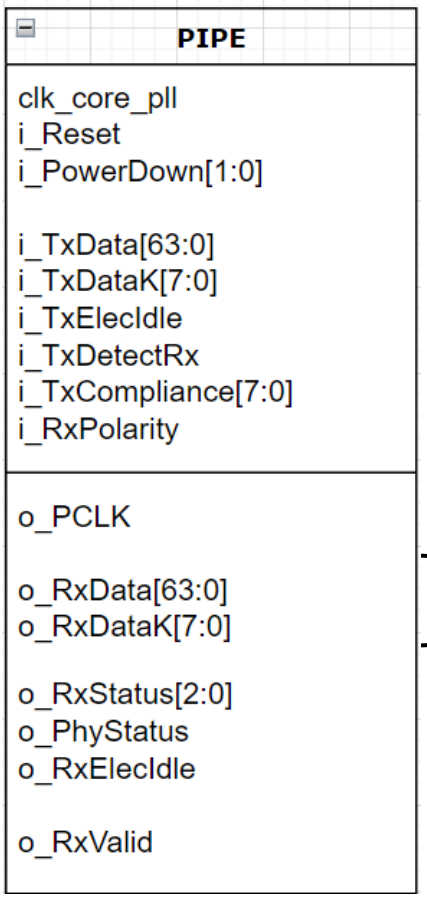
- Reference clock from ADPLL.
- Parallel Interface Clock for MAC and PHY synchronization.
- Asynchronous Reset for Transceiver.
- Power states.

PIPE Interface



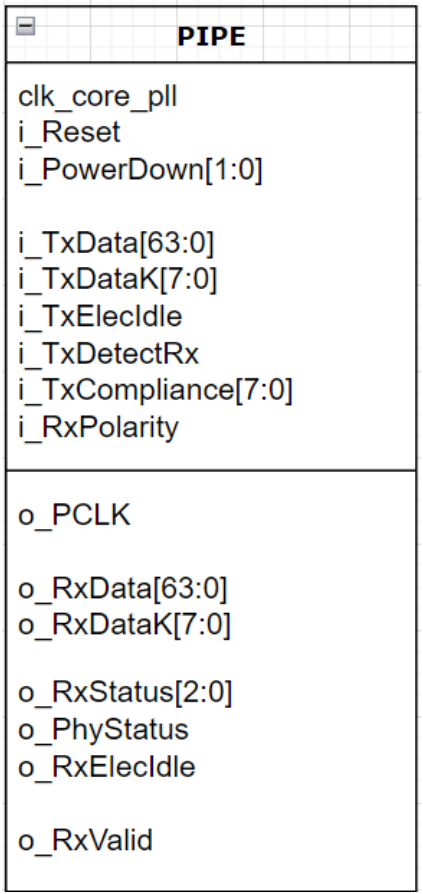
- Data from MAC for SerDes Transmitter.
- Control signals triggered by MAC layer.

PIPE Interface



- Data from SerDes Receiver.

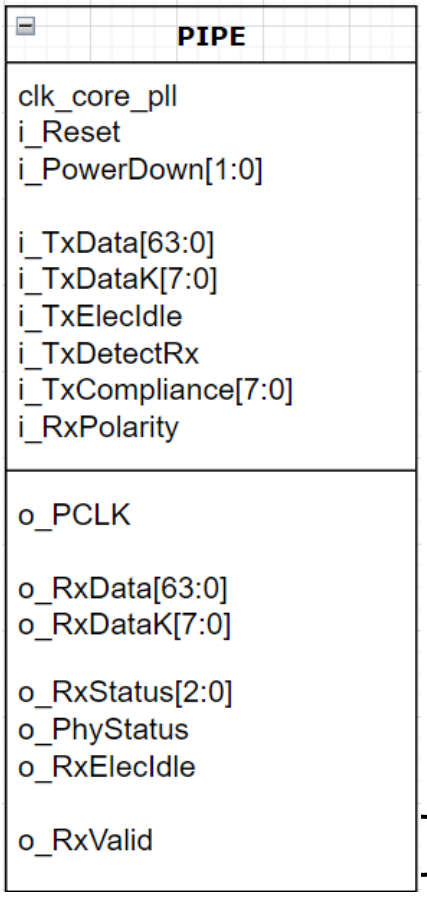
PIPE Interface



RxStatus	Description
000	Received Data OK (P0), Receiver not detected (P1)
001	SKP added
010	SKP removed
011	Receiver detected (P1)
100	8b/10b Error and optionally Disparity Error
101	Elastic Buffer Overflow
110	Elastic Buffer Underflow
111	Disparity Error. Unused if reported together with 8b/10b Error (100).

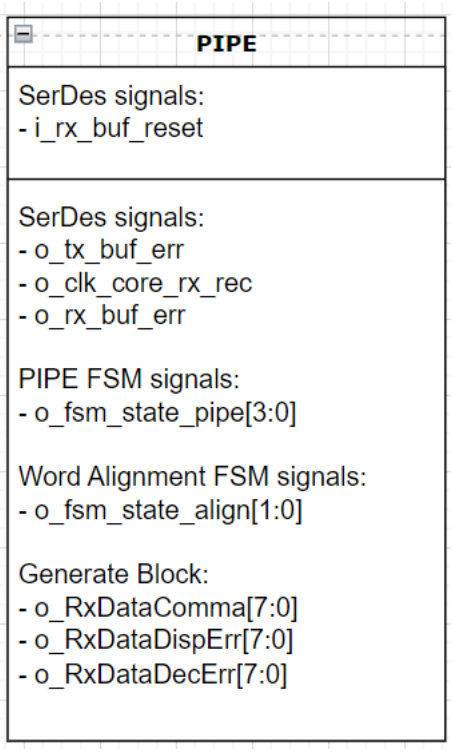
- RxStatus: Status of the received data.
- PhyStatus: Successful power state change or finished Receiver Detection.

PIPE Interface



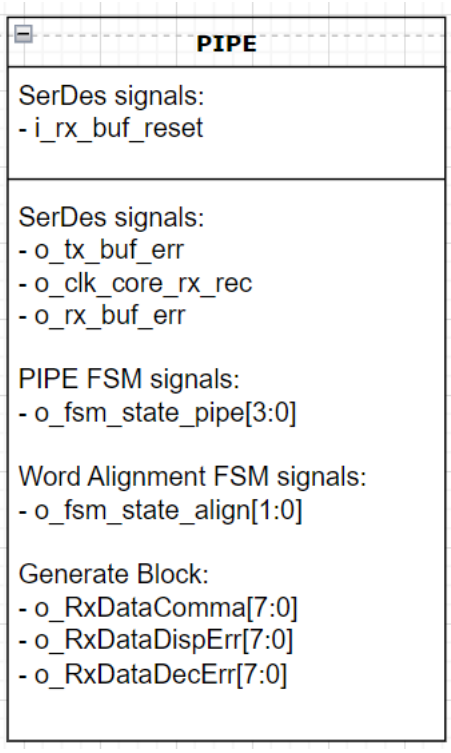
- RxValid: Indicates symbol lock/Received data is valid.

CSS Interface



- SerDes signals:
  - i_rx_buf_reset: trigger a reset for the elastic buffer.
  - o_tx_buf_err: Overflow or Underflow in Transmitter buffer.
  - o_clk_core_rx_rec: Recovered Clock from the received data.
  - o_rx_buf_err: Overflow or Underflow in Elastic Buffer of SerDes Receiver.

CSS Interface



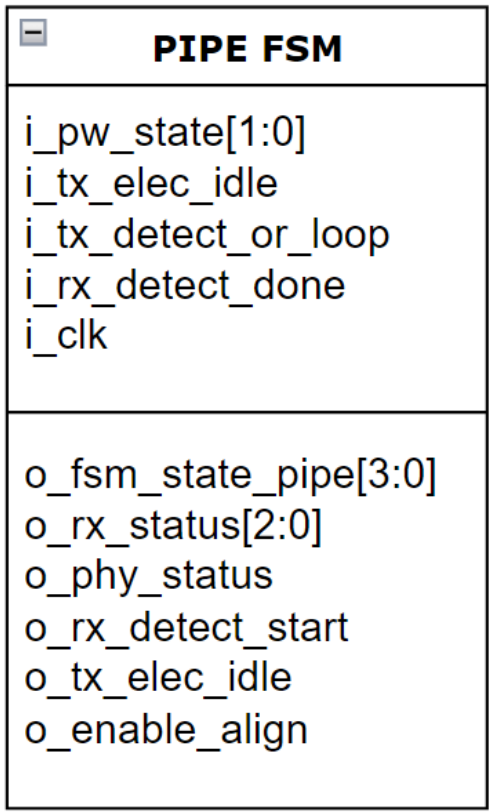
- PIPE FSM:
  - o_fsm_state_pipe [3:0]: current state of the PIPE FSM.
- Word Alignment FSM:
  - o_fsm_state_align [1:0]: current state of the Word Alignment FSM.
- Generate Block: Module that has received and transmitted data along with their error flags as inputs and generate status signals accordingly.
  - o_RxDataComma [7:0]: Each bit represents if the symbol at that position is a COM or not.
  - o_RxDataDispErr [7:0]: Each bit represents if the symbol at that position has disparity error or not.
  - o_RxDataDecErr [7:0]: Each bit represents if the symbol at that position has 8b/10b Decode error or not.

Register Interface

- clk_reg: reference clock for the dynamic reconfiguration port.
- regfile_en: enable control signal to access the dynamic reconfiguration feature.
- regfile_we: provides the write enable control signal to write the data on the data input port into the register selected by the address bus.
- regfile_addr: dynamic reconfiguration address.
- regfile_di: provides reconfiguration data that writes into a specified address of the register set.
- regfile_do: provides data output of the register selected by the address bus.
- regfile_rdy: provides the response to the enable signal for the PLL's dynamic reconfiguration feature. This signal is pulsed High when a write or read operation is successful.

- Register mapping can be found in Gatemate datasheet (Page 90-97).

PIPE FSM



- Inputs:
  - i_pw_state [1:0]: current power state.
  - i_tx_elec_idle: set transmitter in electrical idle state when set.
  - i_detect_or_loop: trigger receiver detection or loopback mode when set.
  - i_rx_detect_done: receiver detection is done.
  - i_clk: input clock.
- Outputs:
  - o_fsm_state_pipe [3:0]: current state of PIPE FSM.
  - o_rx_status [2:0]: receiver status.
  - o_phy_status: physical status flag.
  - o_rx_detect_start: initiate receiver detection.
  - o_tx_elec_idle: set transmitter in electrical idle state.
  - o_enable_align: enable word alignment.

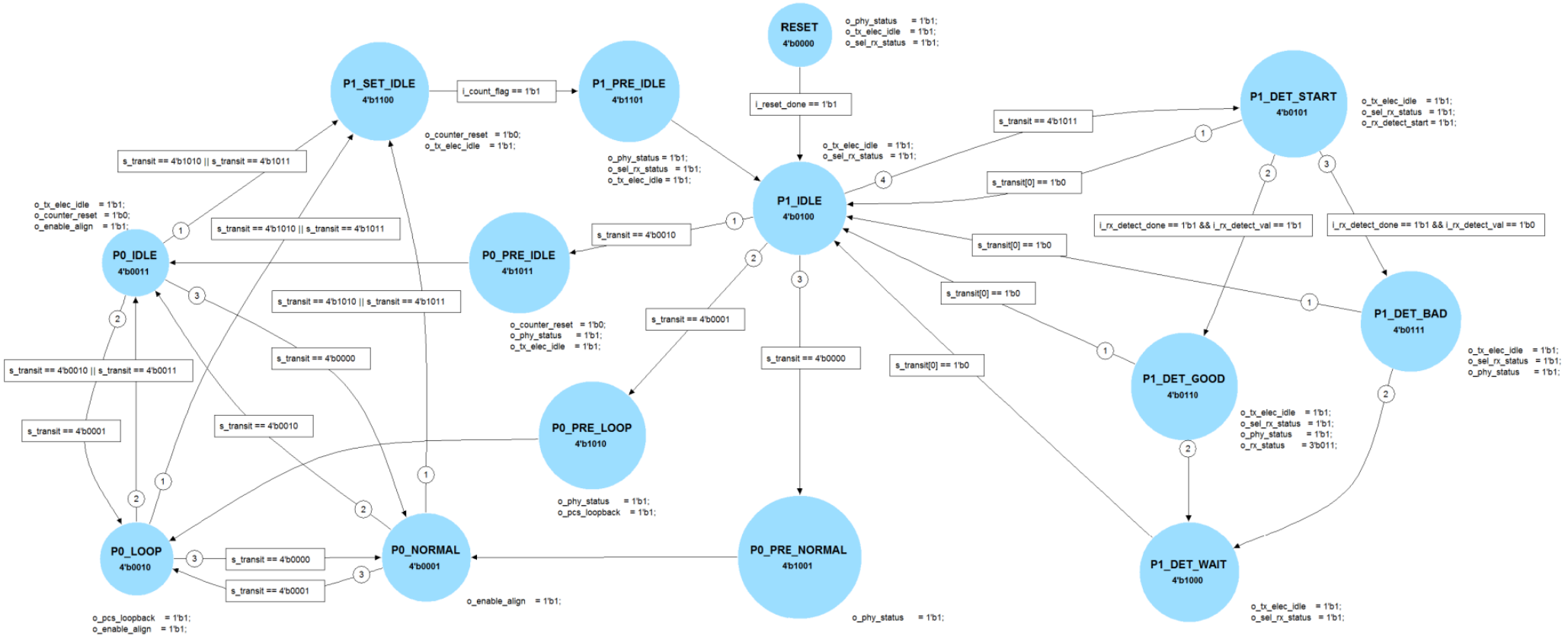
States in PIPE FSM

PIPE FSM	
RESET	Reset state
P1_IDLE	Transmitter in Electrical Idle state
P1_DET_START	Trigger Receiver Detection operation, set i_TxDetectRx to 1
P1_DET_GOOD	Receiver detected (RxStatus = 011)
P1_DET_BAD	Receiver not detected (RxStatus = 000)
P1_DET_WAIT	Wait for i_TxDetectRx back to 0
P0_NORMAL	Normal operation
P0_LOOP	Loopback mode
P0_IDLE	Transmitter in Electrical Idle state
P1_SET_IDLE	Trigger transition from power state P0 to P1

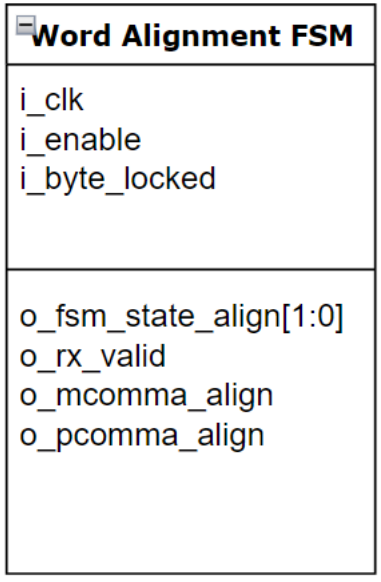
- Prefix Px represents the current power state.
- Each state transition where a power state change is possible would also require a PRE-state in between. This state will set the PhyStatus flag to 1'b1. The flag is deasserted when the power state change is successfully completed. The behavior follows the PIPE Specs.
- Power state change possible for:
  - From P1_IDLE to all P0 states.
  - From P0 states through P1_SET_IDLE to P1_IDLE.

States in PIPE FSM

s_transit = { i_pw_state , i_tx_elec_idle , i_tx_detect_or_loop }



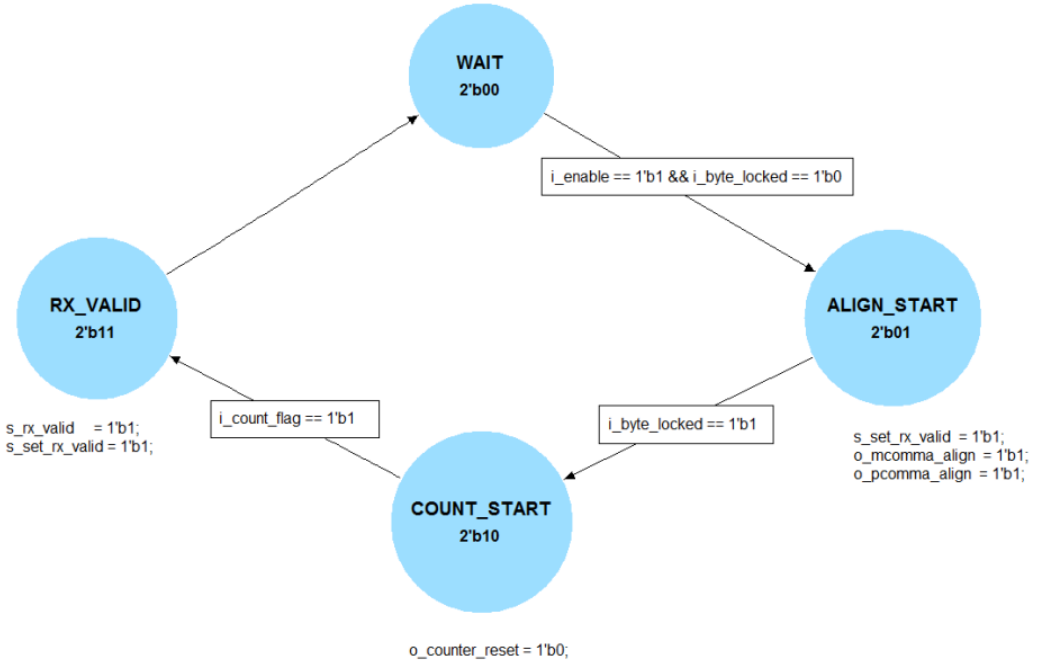
Word Alignment FSM



- Inputs:
  - i_enable: enable word alignment.
  - i_byte_locked: byte is locked.
  - i_clk: input clock.
- Outputs:
  - o_fsm_state_align [1:0]: current state of Word Alignment FSM.
  - o_rx_valid: received data is valid.
  - o_mcomma_align: activate word alignment of SerDes (negative comma sequence).
  - o_pcomma_align: activate word alignment of SerDes (positive comma sequence).

States in Word Alignment FSM

Word Alignment FSM	
WAIT	Reset state
ALIGN_START	Alignment enabled but byte is not locked
COUNT_START	Byte is locked, start counter
RX_VALID	Target value reached, received data is valid



References

- PHY Interface for the PCI Express* Architecture (PIPE) Specs
- AMD DRP Definition
- Philipp Ledüc’s Masterthesis

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