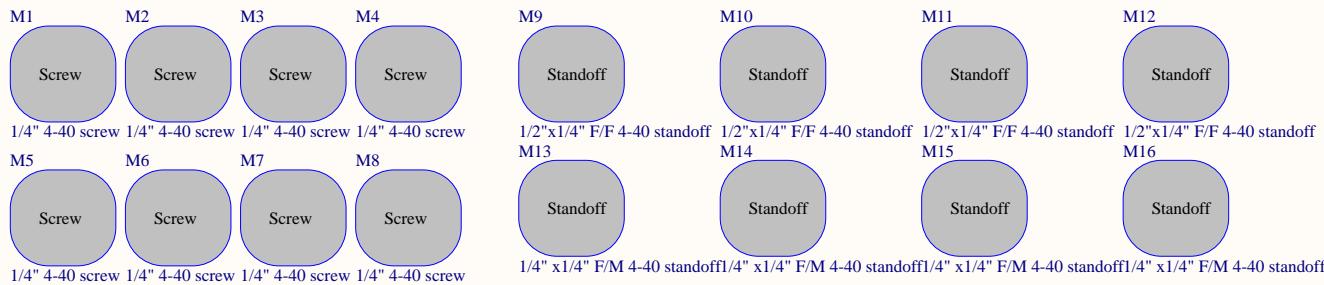


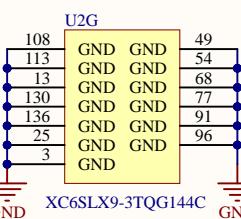
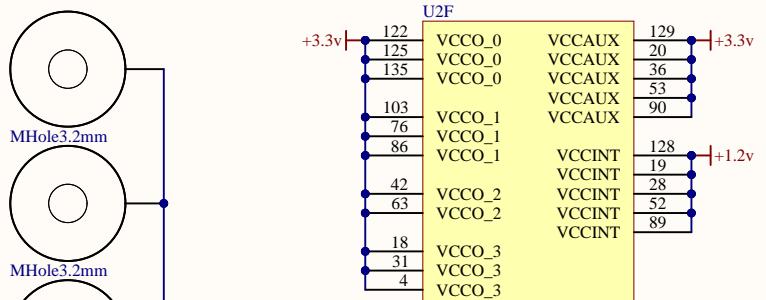
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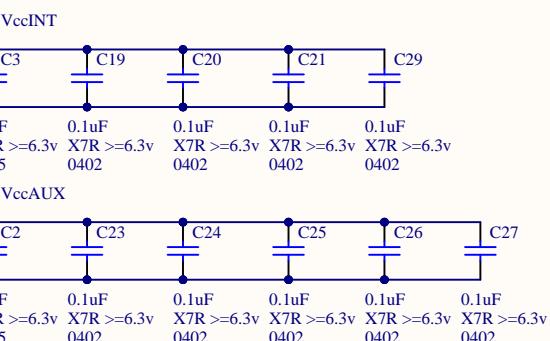
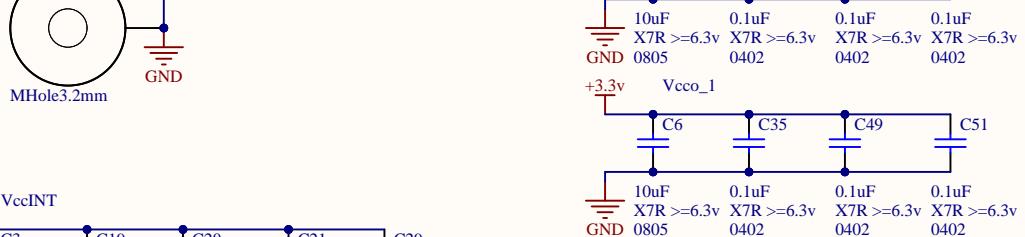
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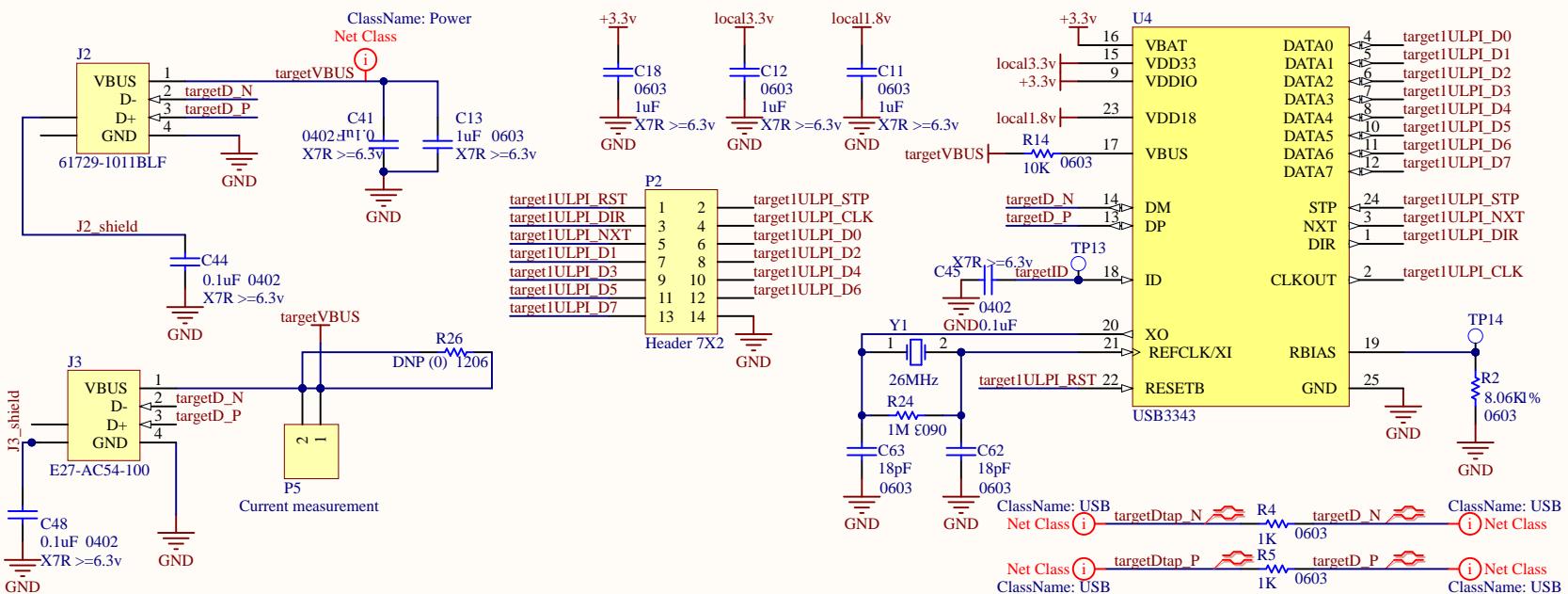
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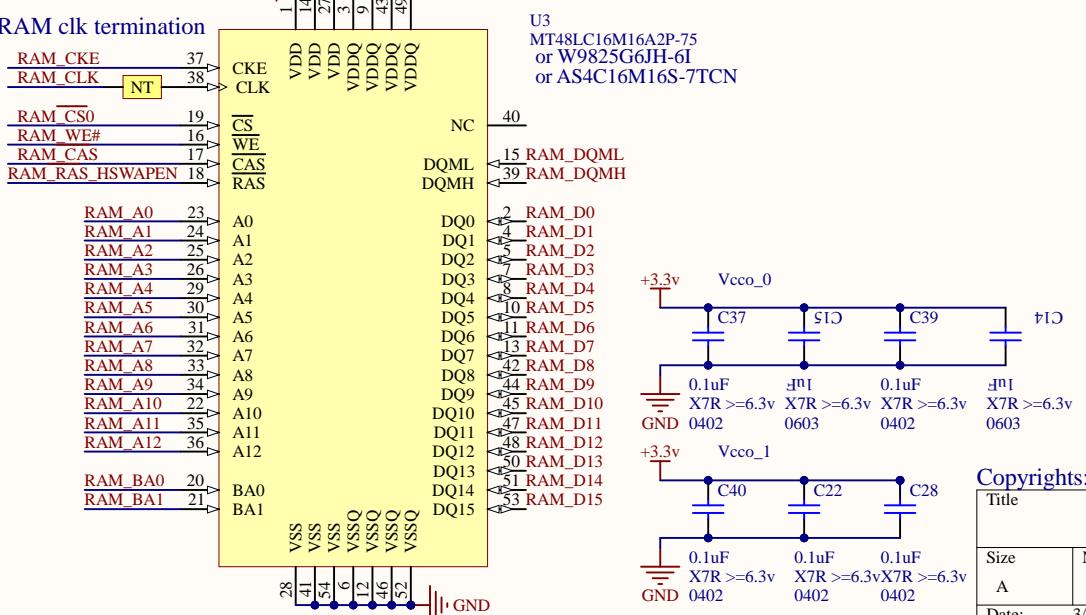


B

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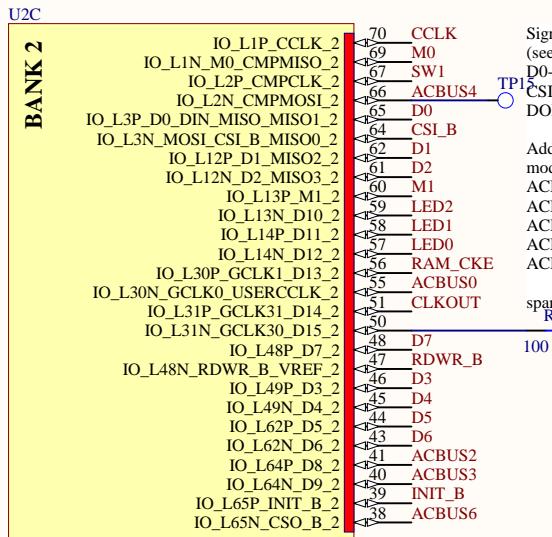
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optional RAM clk termination



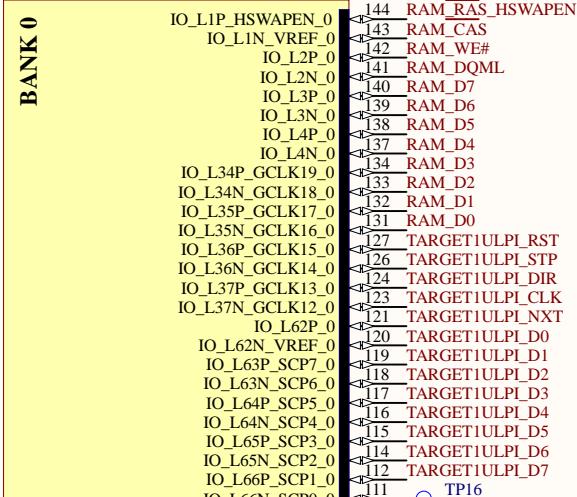
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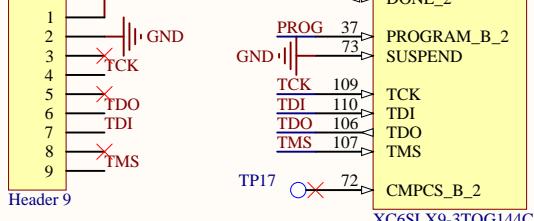
XC6SLX9-3TQG144C

U2A



XC6SLX9-3TQG144C

P1

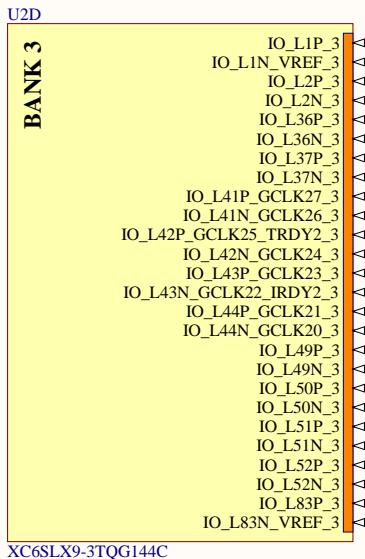


AC03EX9-51QG144C

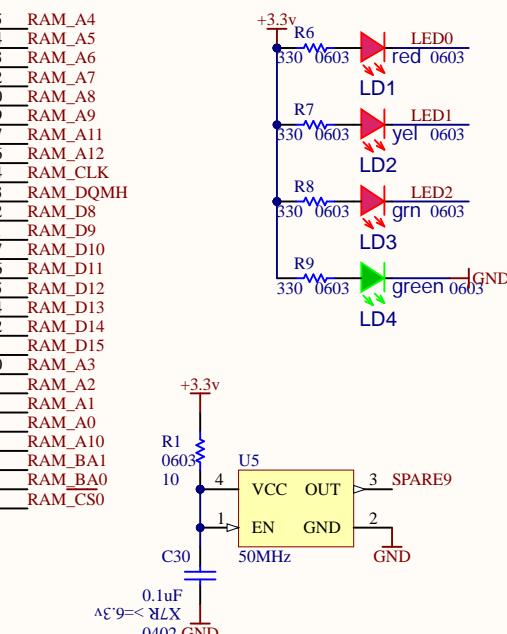
Signals used during FPGA configuration
(see XAPP502):
P15 D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBU55 (CLKOUT)
ACBUS6 (OE#)

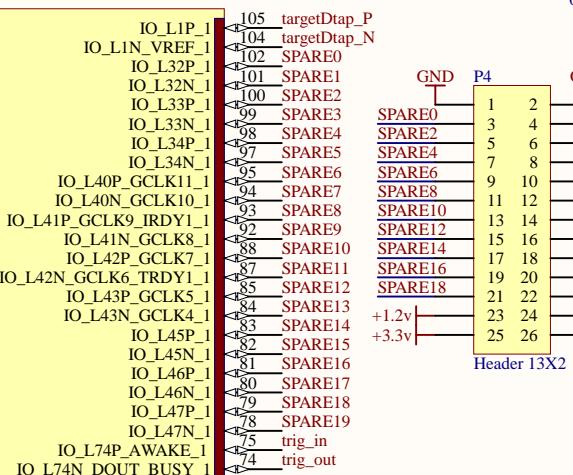
spare I/Os:
R3 ... OSCO



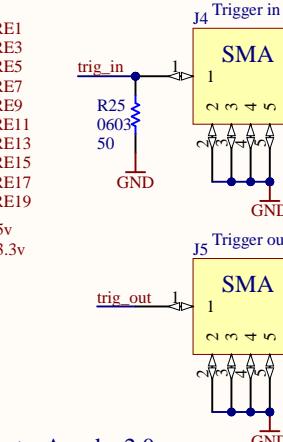
XC6SLX9-3TQG144C



Spare 50MHz clock for bringup



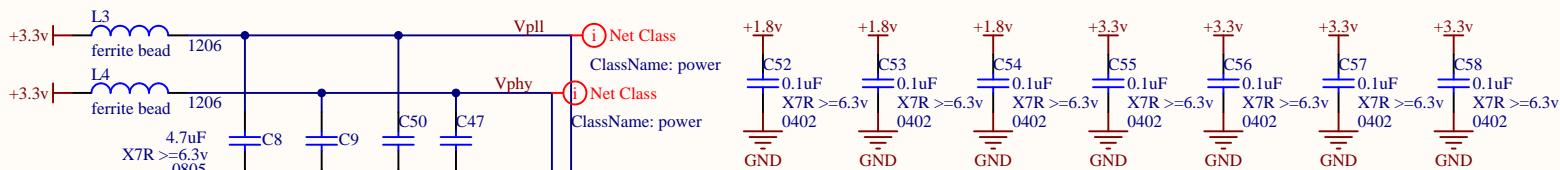
144C



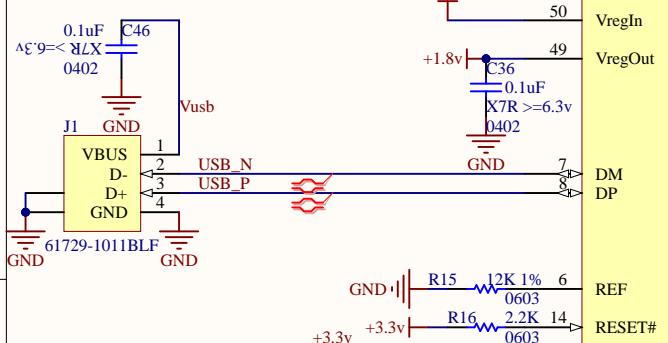
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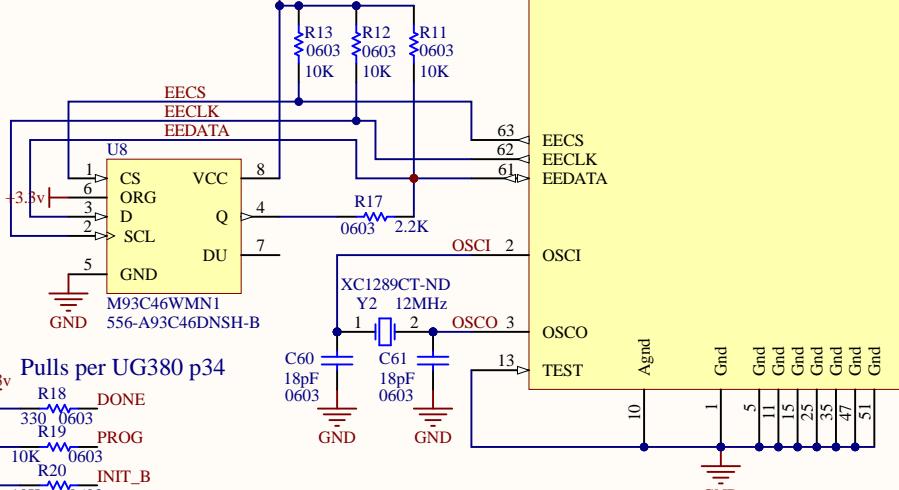
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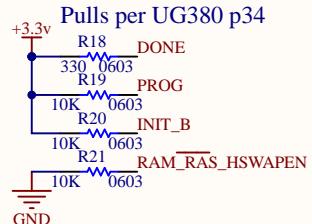
B



C



D



FT2232H

Configuration / FIFO to FPGA

Signals used during FPGA configuration
(see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

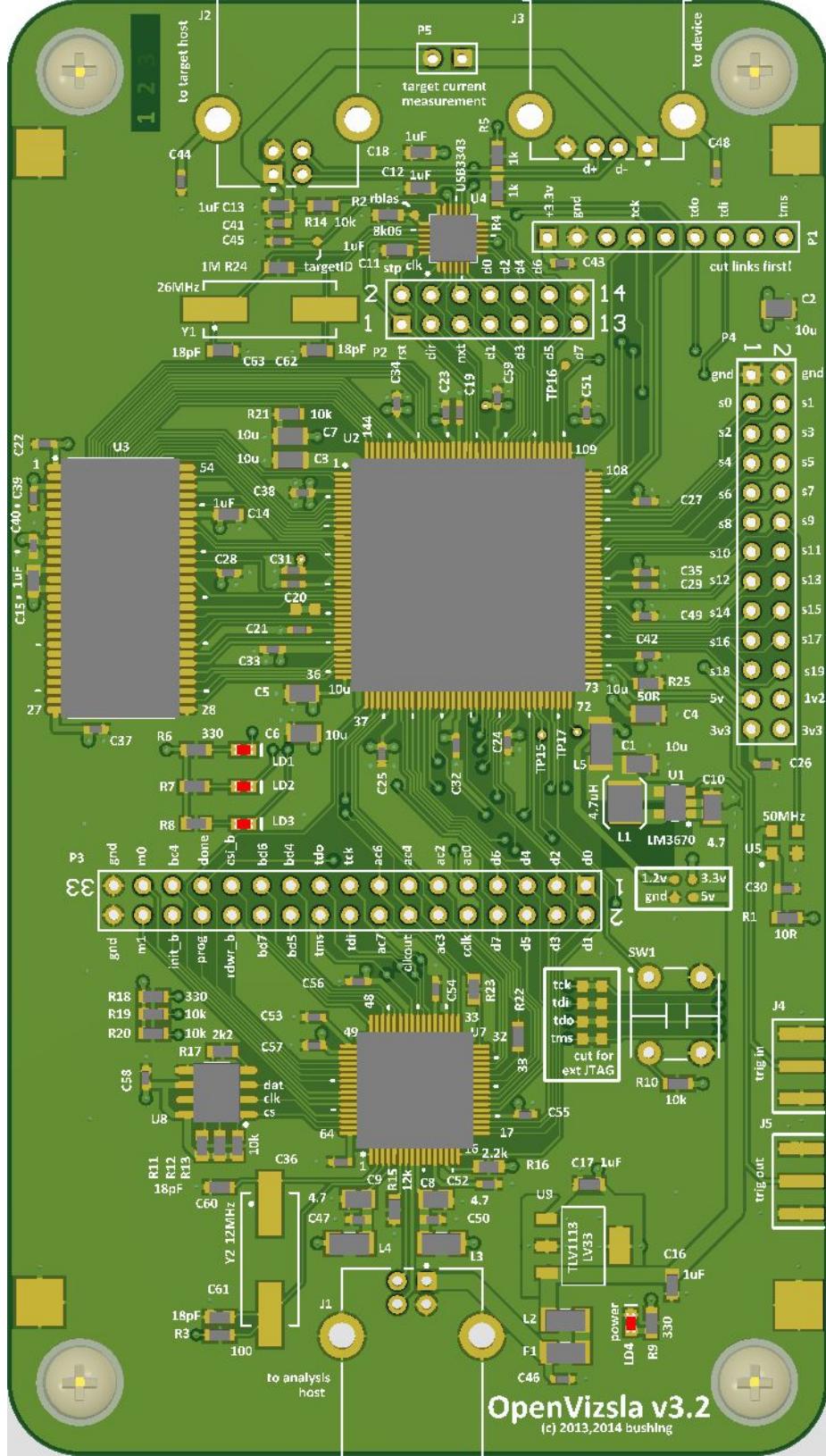
spare I/Os:

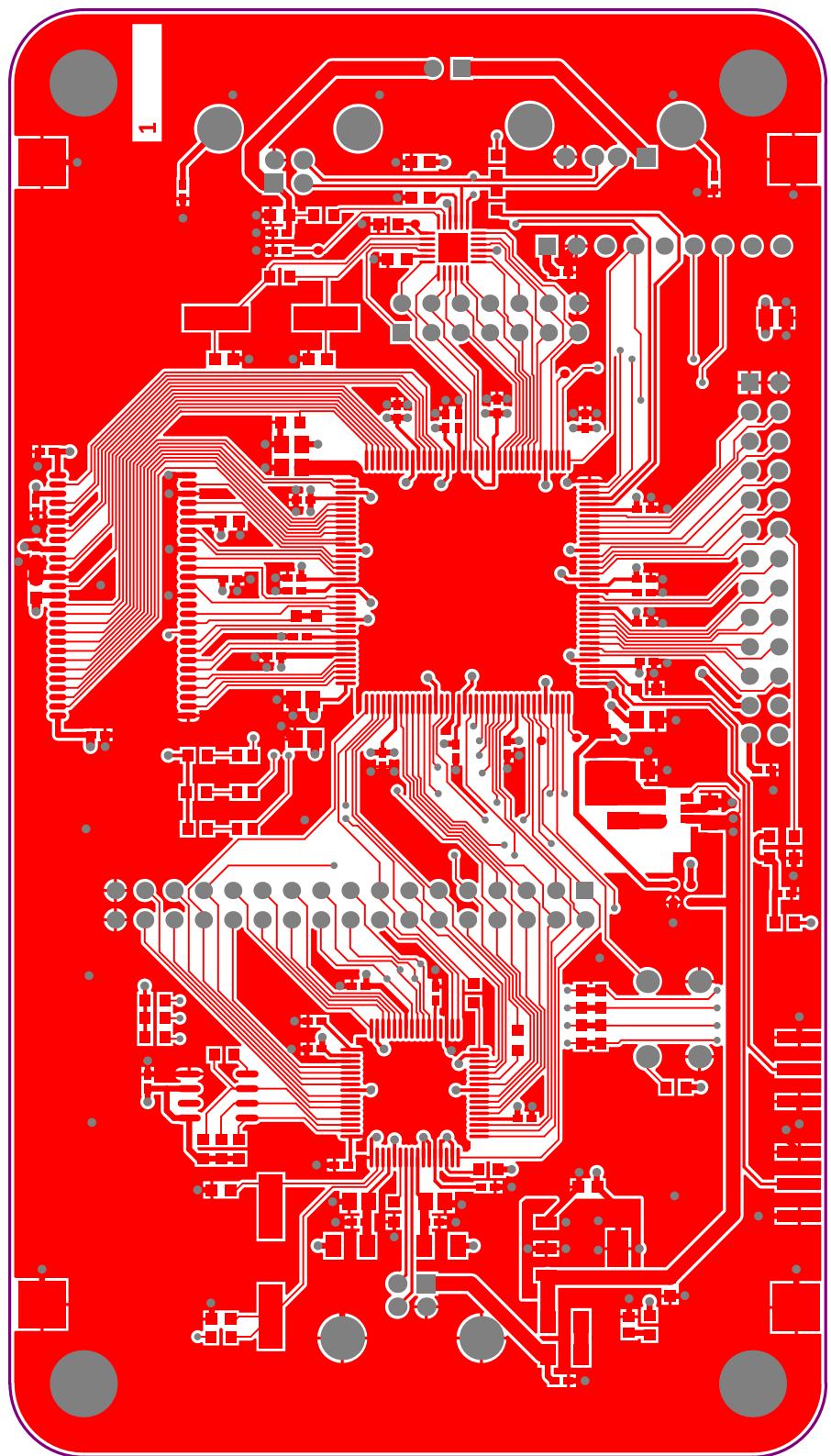
P3	D0	D1	D2	D3	D4	D5	D6	D7	CCLK	CLKOUT
	1	2	3	4	5	6	7	8	0603	0603
	D0	D1	D2	D3	D4	D5	D6	D7	ACBUS0	ACBUS1
	ACBUS1	ACBUS2	ACBUS3	ACBUS4	ACBUS5	ACBUS6	ACBUS7		ACBUS0	ACBUS1
	ACBUS2	ACBUS3	ACBUS4	ACBUS5	ACBUS6	ACBUS7			ACBUS0	ACBUS1
	ACBUS3	ACBUS4	ACBUS5	ACBUS6	ACBUS7				ACBUS0	ACBUS1
	ACBUS4	ACBUS5	ACBUS6	ACBUS7					ACBUS0	ACBUS1
	ACBUS5	ACBUS6	ACBUS7						ACBUS0	ACBUS1
	ACBUS6	ACBUS7							ACBUS0	ACBUS1
									ACBUS0	ACBUS1
									ACBUS2	ACBUS3
									ACBUS4	ACBUS5
									ACBUS6	ACBUS7
									FTDI_TCK	FTDI_TDI
									FTDI_TDO	FTDI_TMS

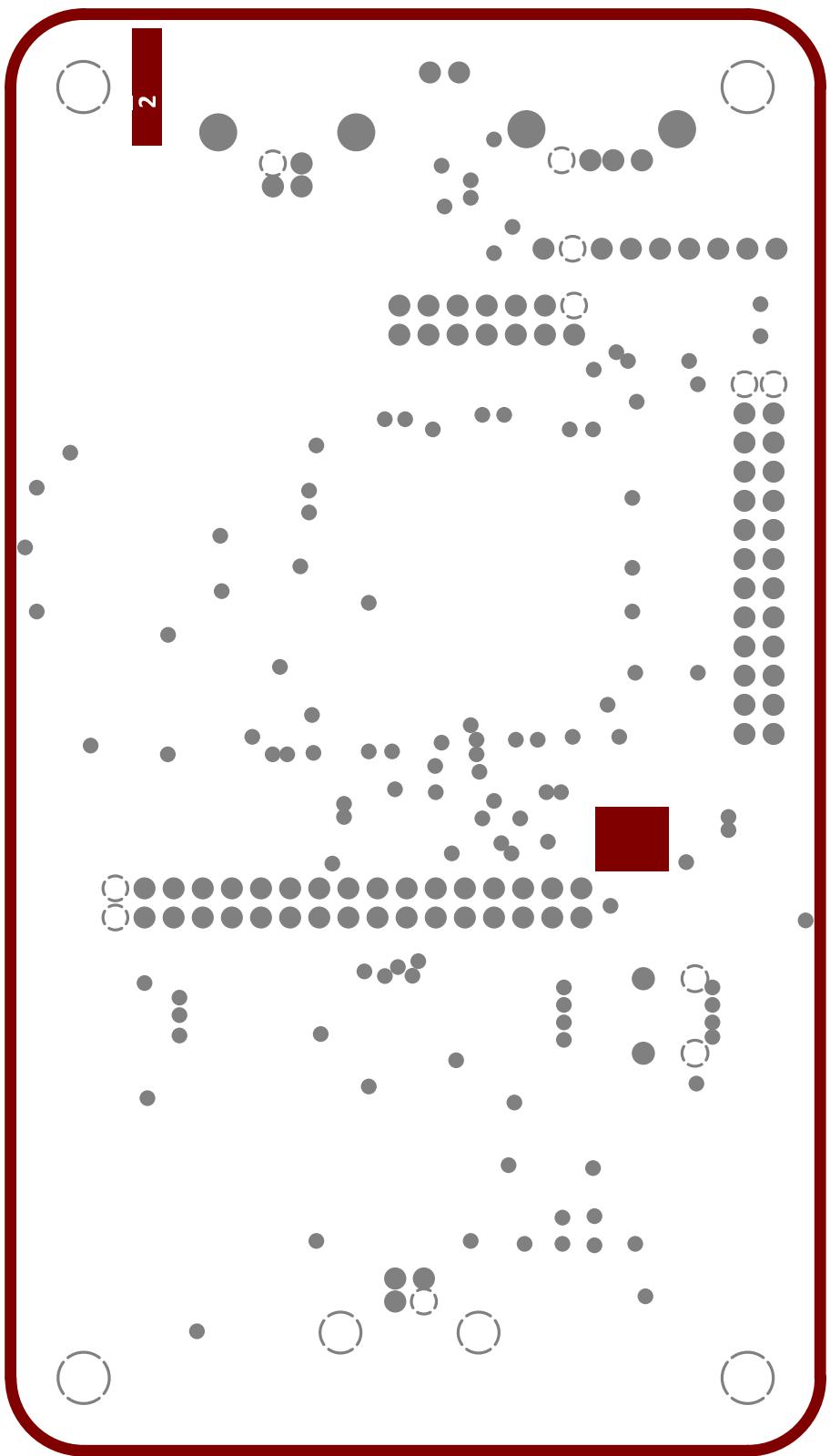
FTDI_TCK	TCK
FTDI_TDI	TDI
FTDI_TDO	TDO
FTDI_TMS	TMS

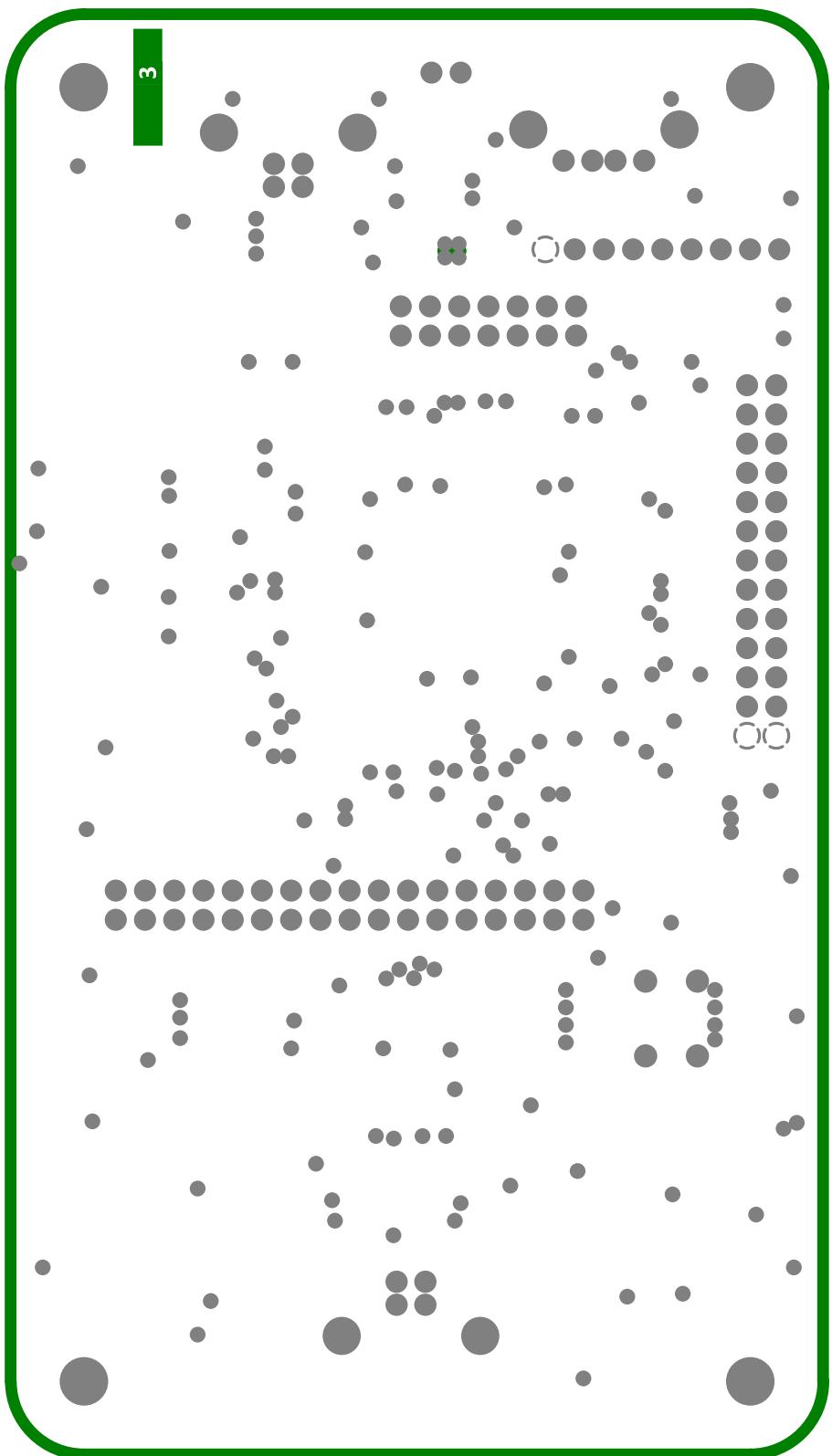
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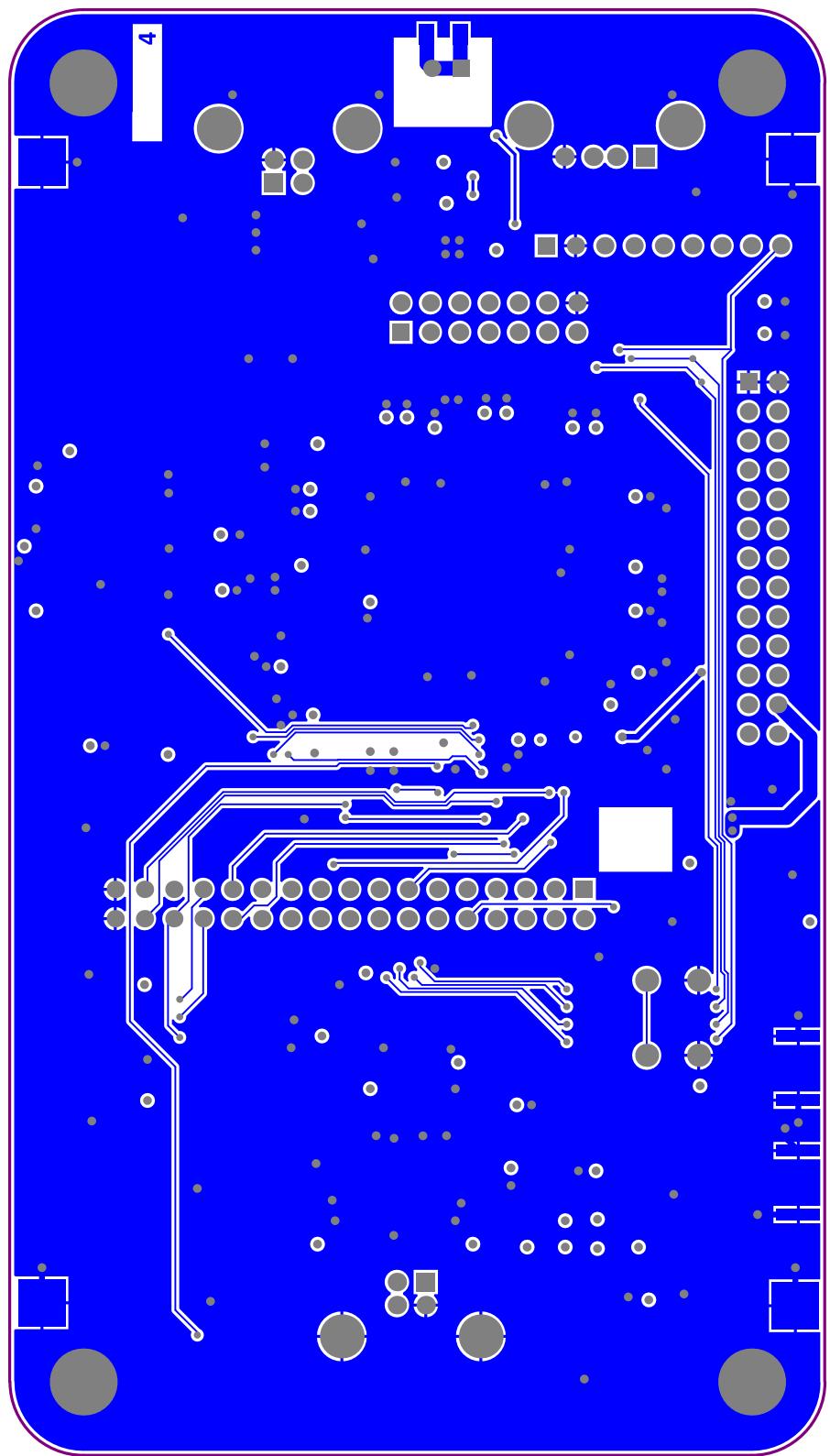
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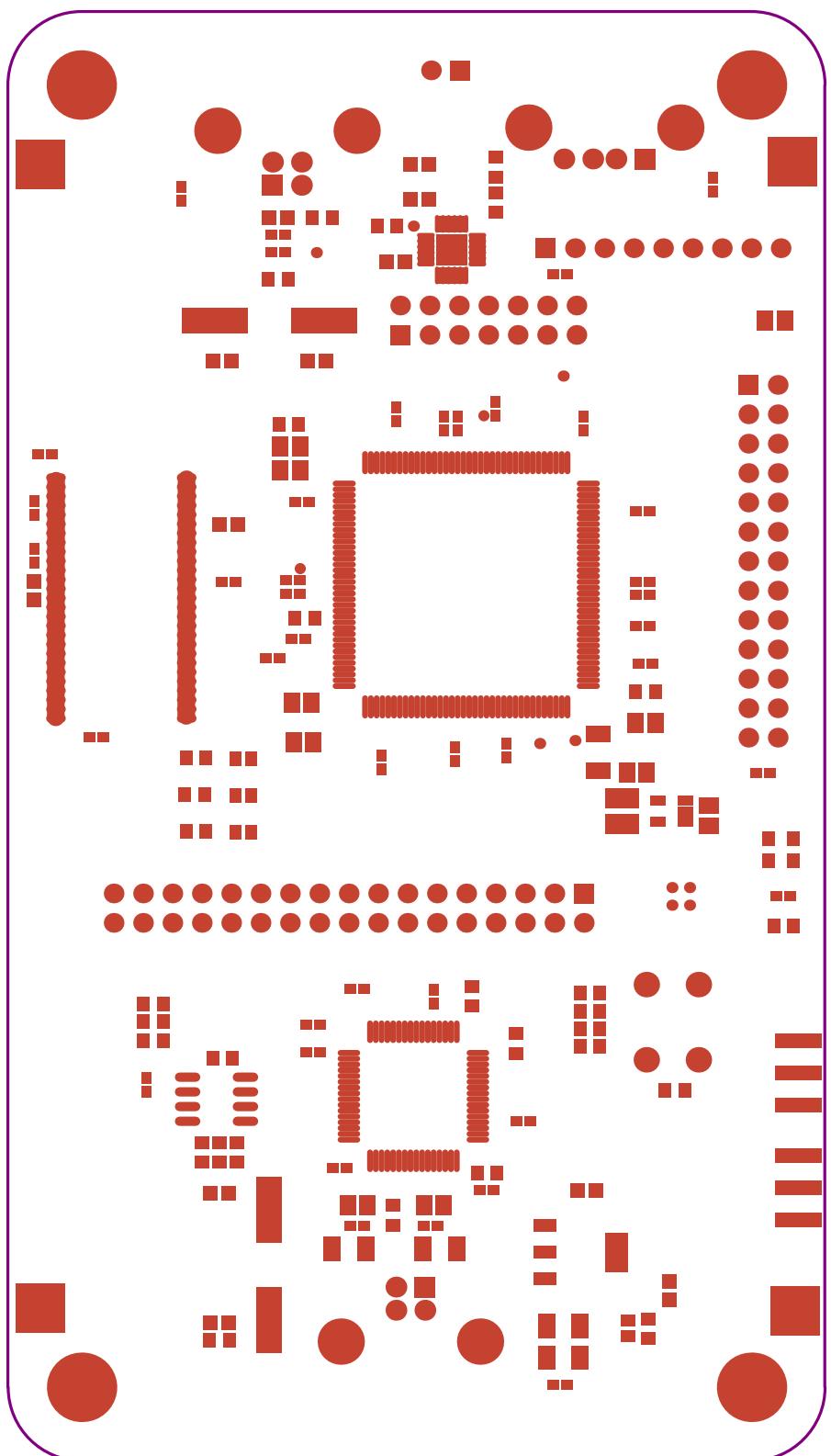


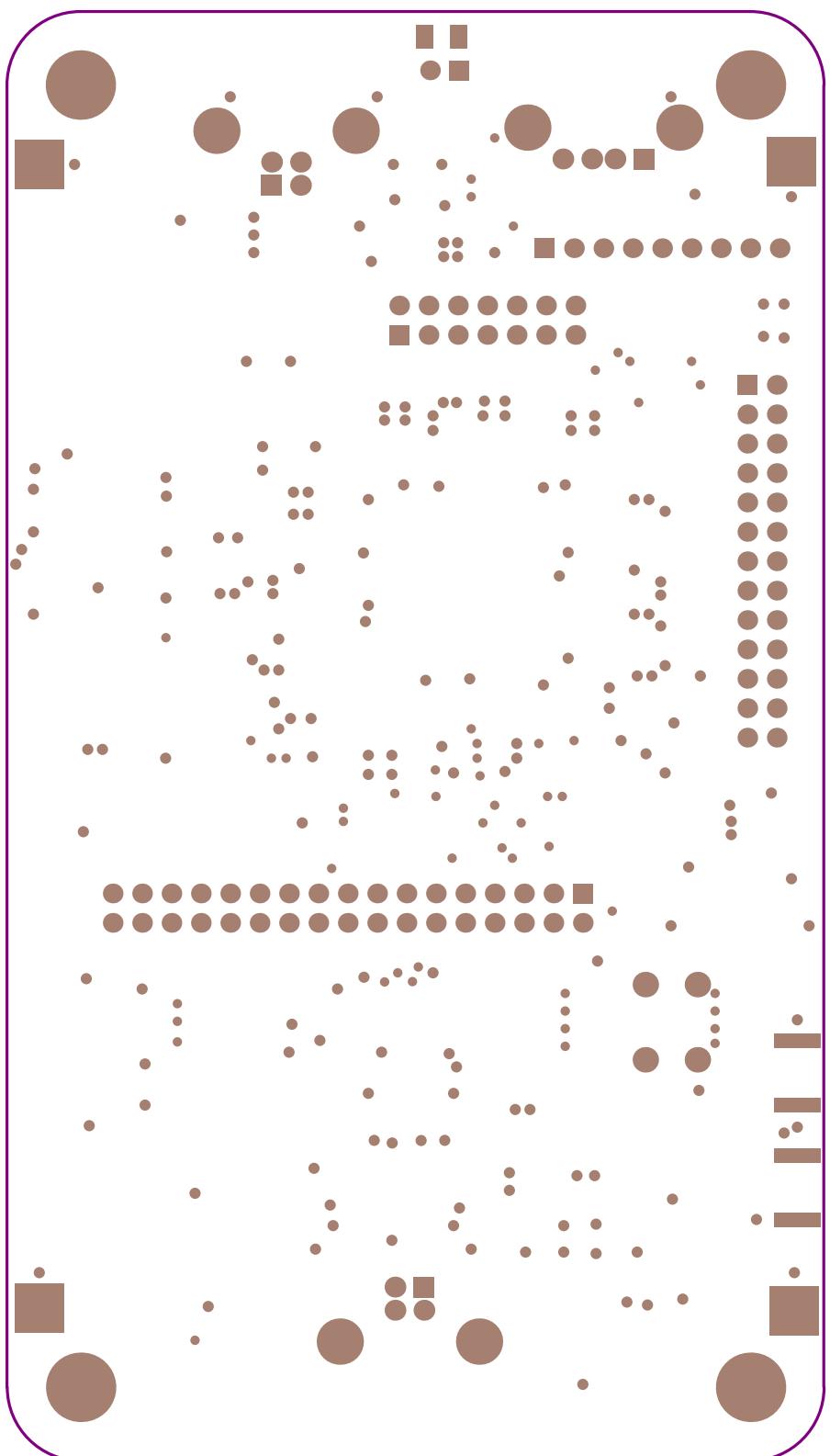


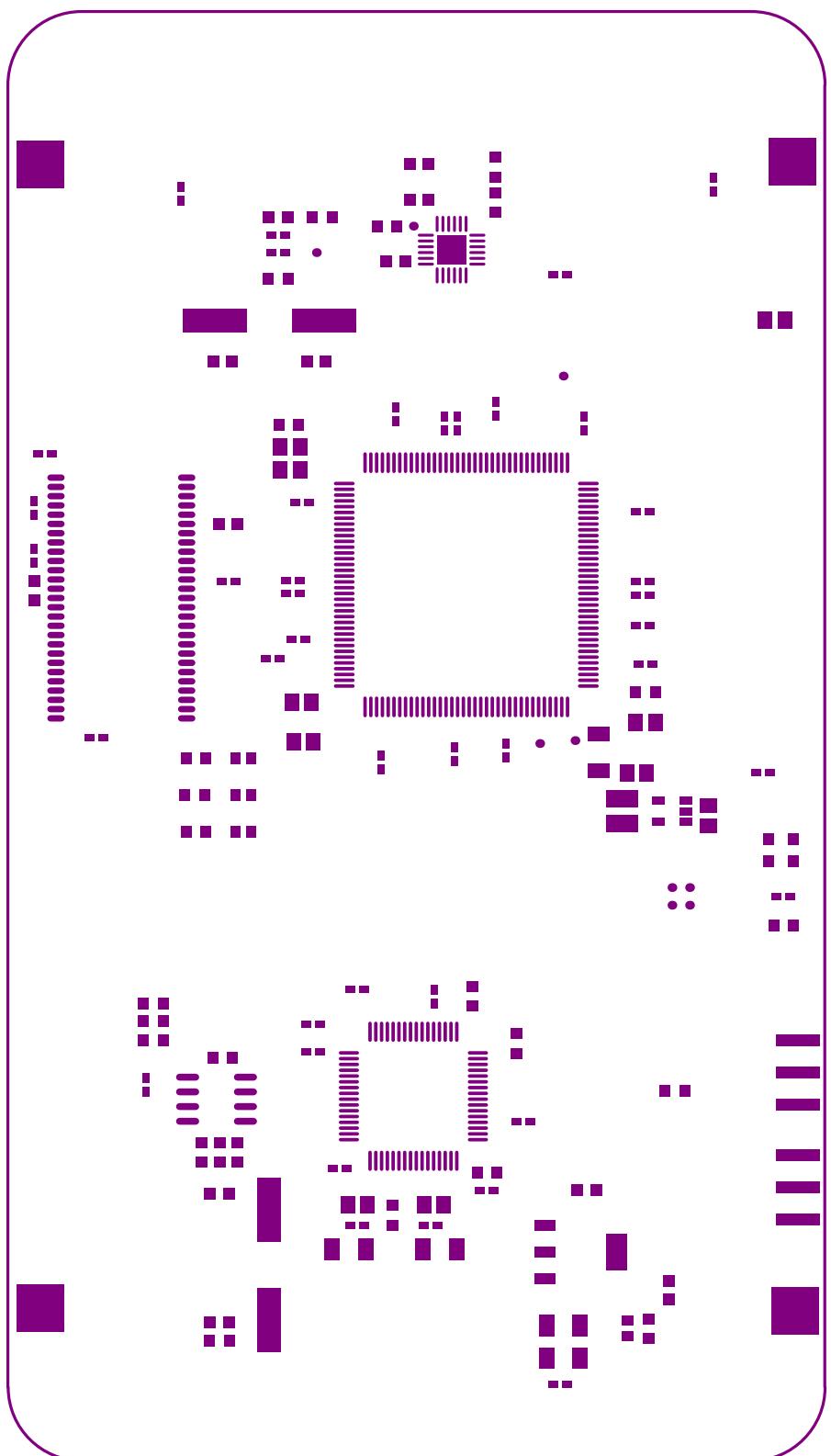


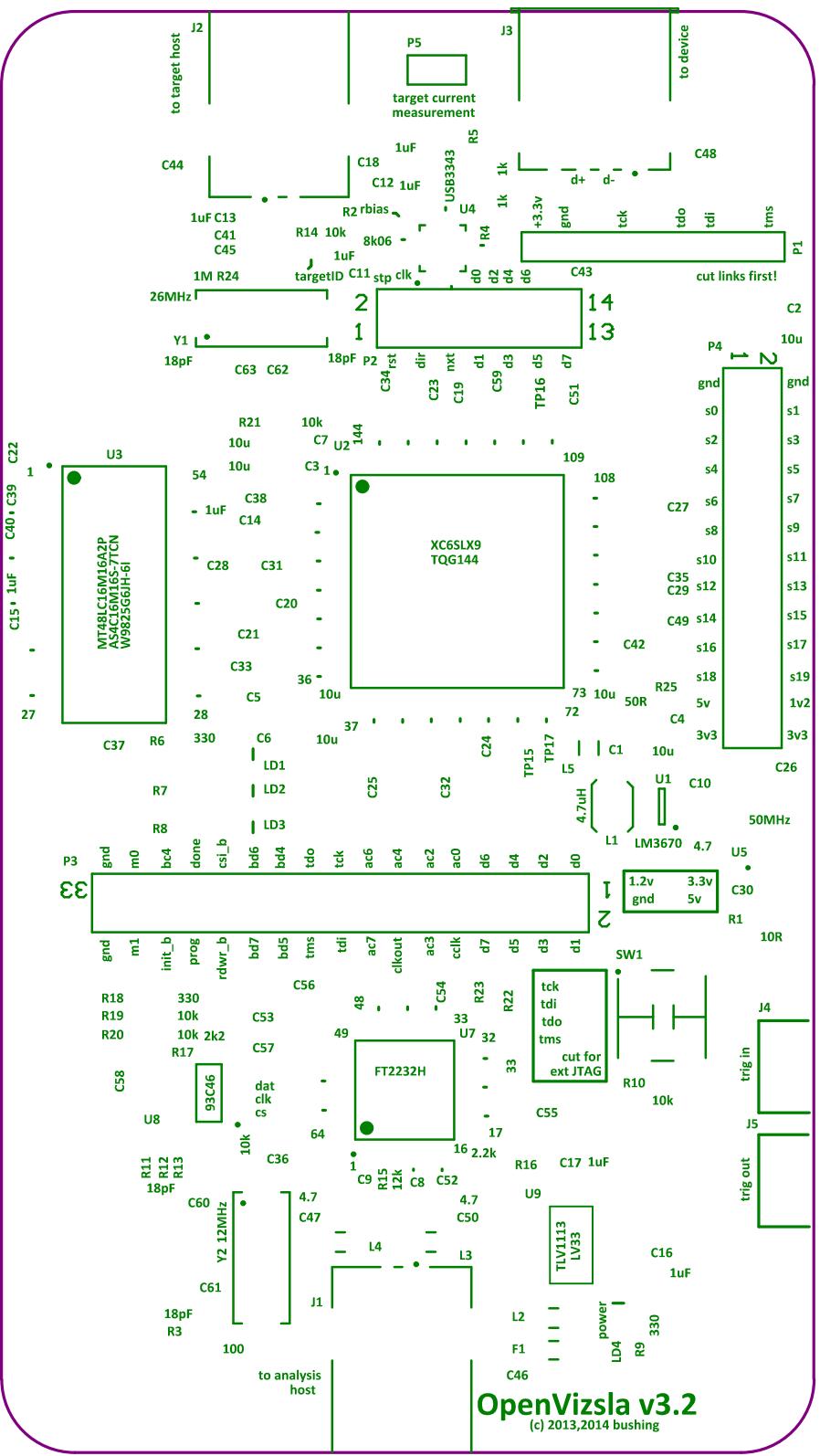












measures must reflect
current practice for

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D+

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fcj
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fug

bng	bng
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qCt	qC5	qC0	qE	qN	qS	q0
qCjent	qC3	ccjk	qJ	q2	q3	qJ

cikonf

aww_	big
um	uh
uh	uh
um	uh
uh	uh

10

