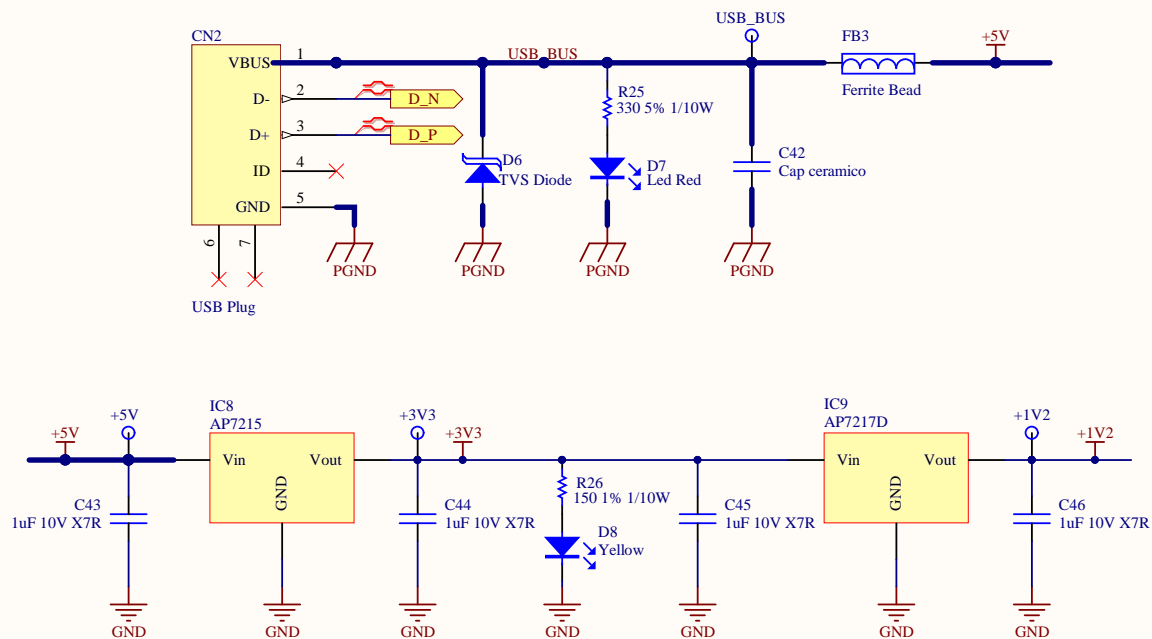


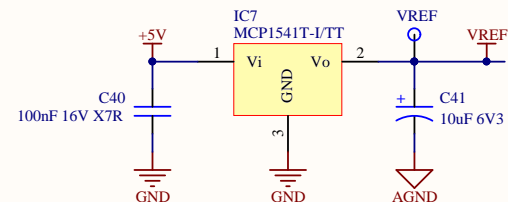
Title MercurialSDR - Block Diagram		
Size A4	Number	Revision Rev2.0
Date: 8/2/2020	Sheet 1 of 6	
File: C:\Users\...\MercurialSDR_BLK.SchDoc	Drawn By: Andres Hojnadel	

Power Stage

USB to +3V3 and +1V2



Reference Voltage

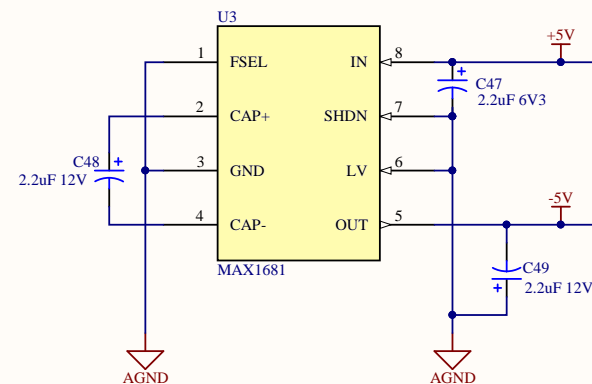


This is a precision voltage reference for DAC (IC1).

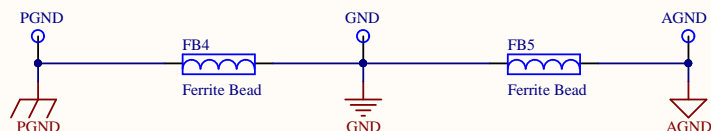
Them must be close.

Inverter Voltage

Es muy importante el ESR de los capacitores para el ripple

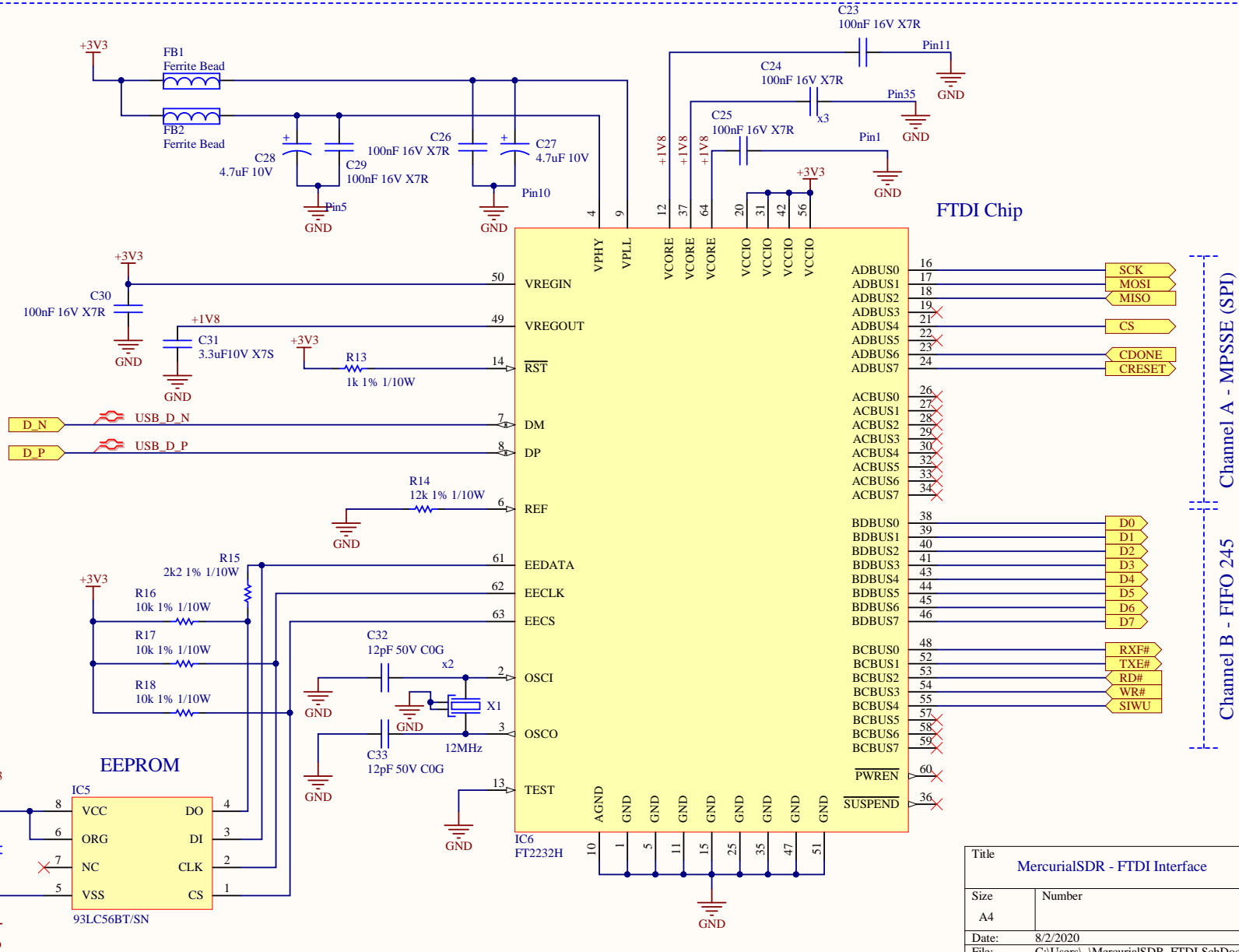


Ground Connections



Title		
MercurialSDR - Power Stage		
Size	Number	Revision
A4		Rev2.0
Date:	8/2/2020	Sheet 2 of 6
File:	C:\Users\...\MercurialSDR_PWR.SchDoc	Drawn By: Andres Hojnadel

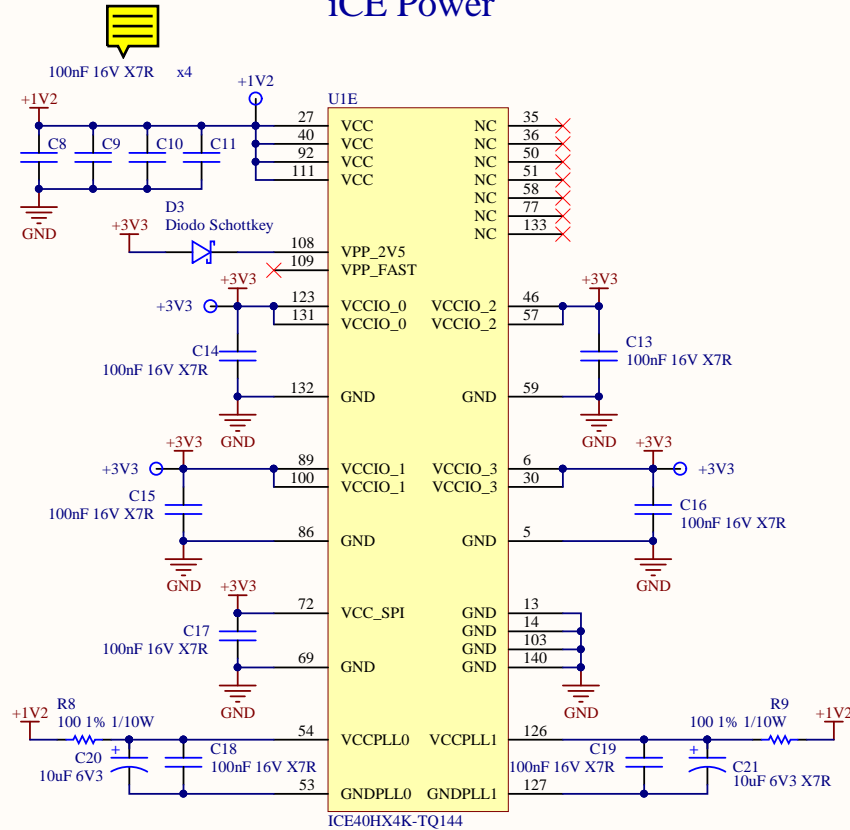
FTDI Interface



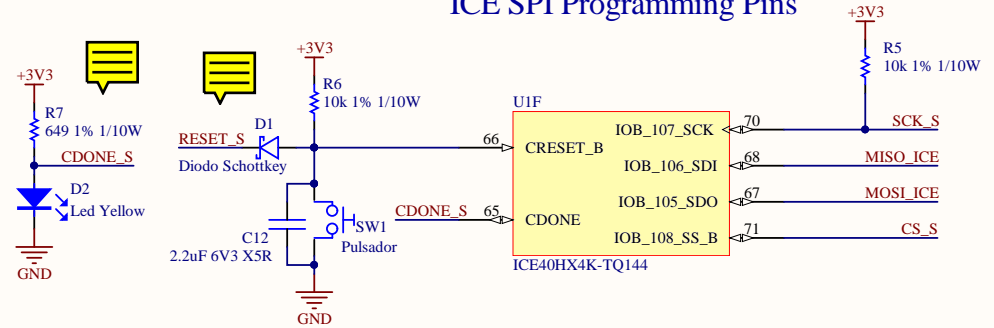
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Size	Number		Revision	
A4			Rev2.0	
Date:	8/2/2020		Sheet 3 of 6	
File:	C:\Users\...\MercurialSDR_FTDI.SchDoc		Drawn By:	Andres Hojnadel

ICE Programming & Power

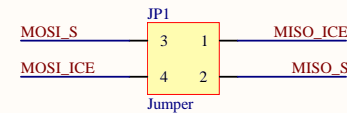
iCE Power



ICE SPI Programming Pins

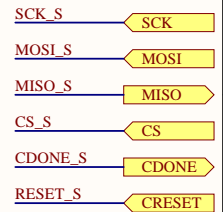


ICE/Flash programming selection

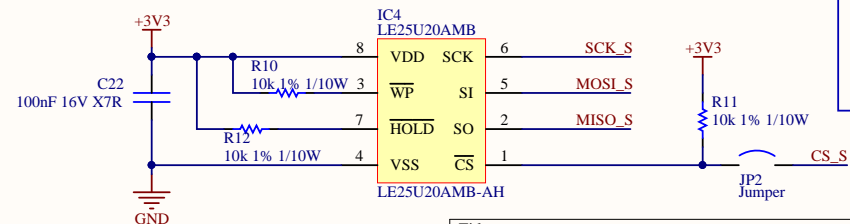


For programming ICE: shunt 1-3 & 2-4
For programming Flash: shunt 1-2 & 3-4

FTDI Ports



Flash Memory

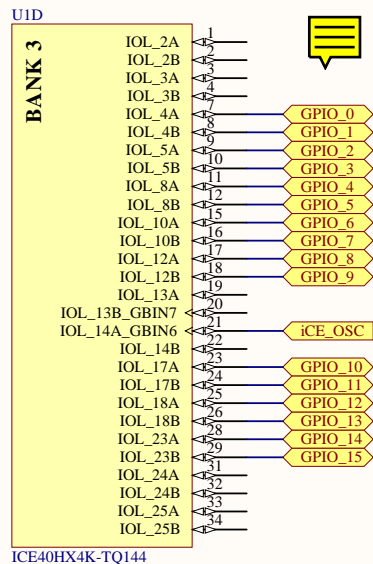
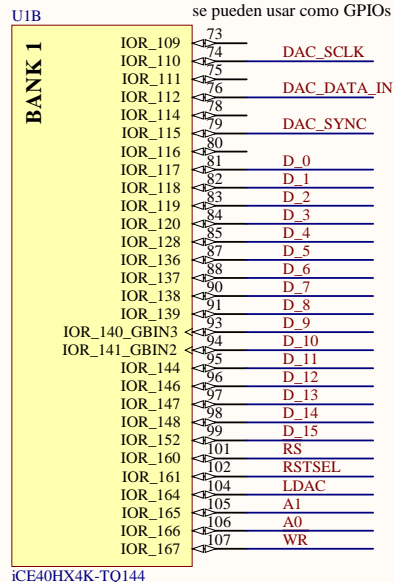


Remove JP2 only for programming ICE
Shunt JP2 for Flash programming or normal operation

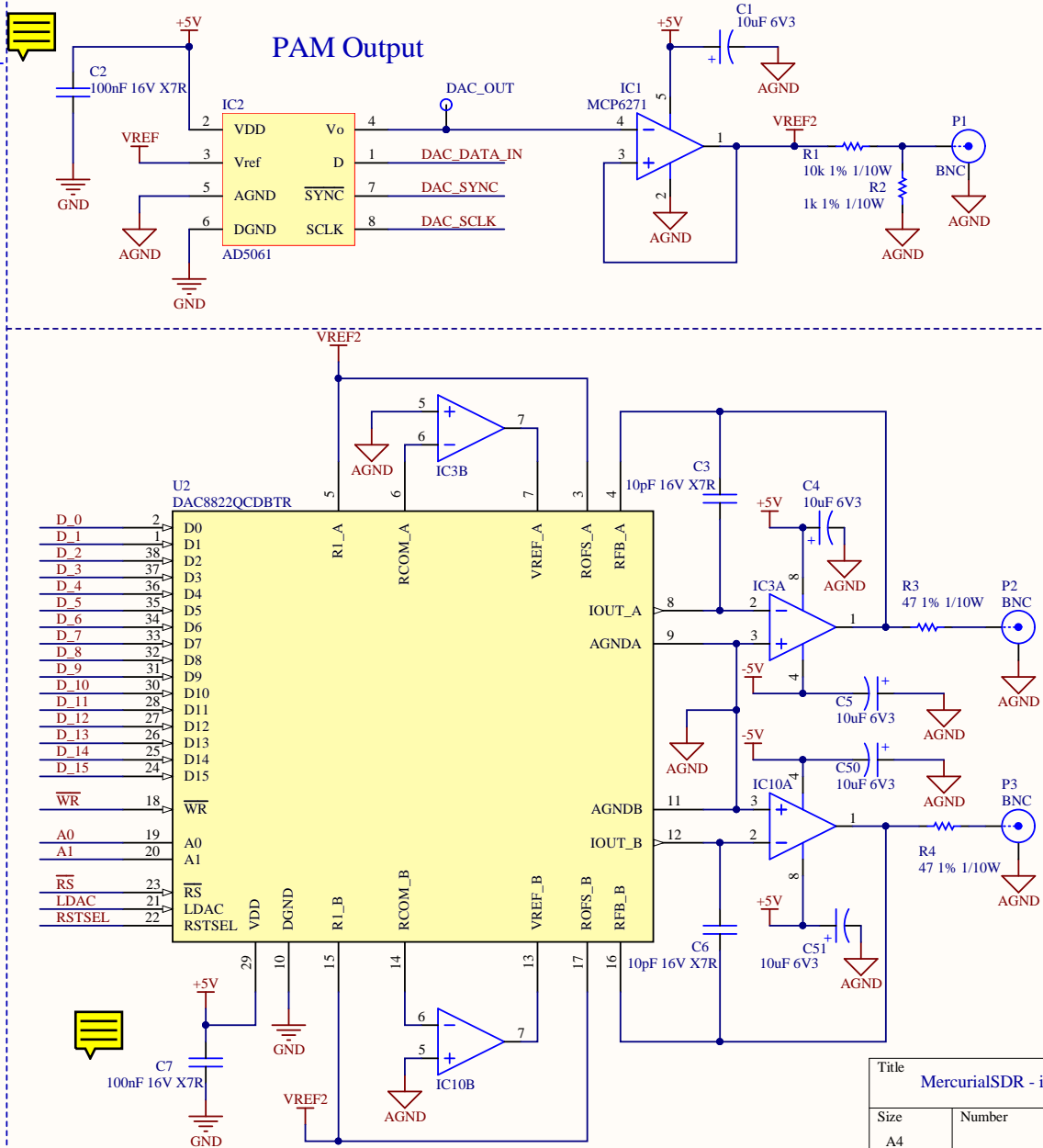
Title MercurialSDR - iCE Power & Program.		
Size A4	Number	Revision Rev2.0
Date: 8/2/2020	Sheet 4 of 6	
File: C:\Users\...\MercurialSDR_FPGA_P&P.Sch	Down By: Andres Hojnadel	

FPGA Banks

PIN93y94 son GlobalPins, pero se pueden usar como GPIOs



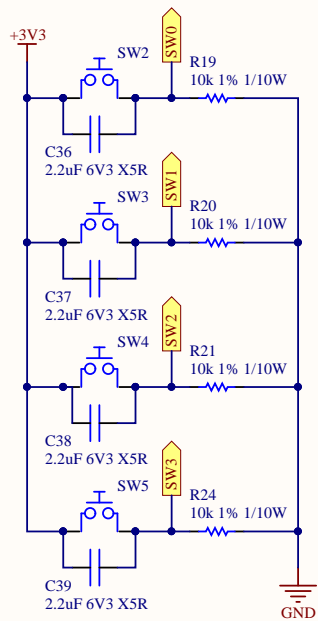
PAM Output



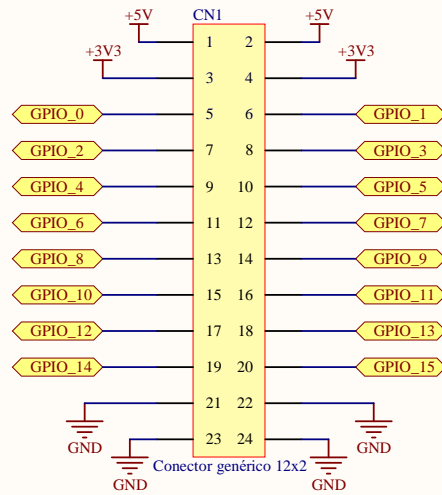
Title		
MercurialSDR - iCE Banks		
Size	Number	Revision
A4		Rev2.0
Date:	8/2/2020	Sheet 5 of 6
File:	C:\Users\...\MercurialSDR_FPGA_BNK_SchDown By:	Andres Hojnadel

Miscellaneous

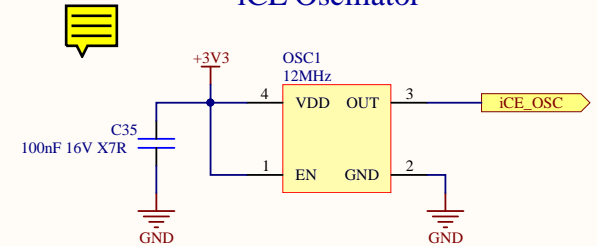
Buttons



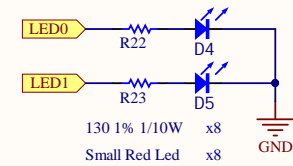
GPIO Ports



iCE Oscillator



Leds



Title MercurialSDR - Miscellaneous		
Size A4	Number	Revision Rev2.0
Date: 8/2/2020	Sheet6 of 6	Drawn By: Andres Hojnadel
File: C:\Users\...\MercurialSDR_MISC.SchDoc		

