SCD Instruction Scheduling

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Pipelined instruction scheduling to calculate half of the **alpha profile**:

Cycle	PE_0	PE_1	PE_2	PE_K	PE_K+1	PE127
32	X_0^T , Y_0^T					
32	MULT	X_1^T , Y_1^T				
160	FFT_32	MULT	X_2^T , Y_2^T			
16	Abs	FFT_32	MULT	……		
32	$\boldsymbol{X_0^T\ Y_1^T}$	Abs	FFT_32		……	
32	**MULT**	$\boldsymbol{X_1^T\ Y_2^T}$	Abs			
160	**FFT_32**	**MULT**	$\boldsymbol{X_2^T\ Y_3^T}$			
16	**Abs**	**FFT_32**	**MULT**	……		
16	**Max**	**Abs**	**FFT_32**		……	
8	**Forward**	**Max**	**Abs**			
32	$X_0^T\ Y_2^T$	**Forward**	**Max**			
	……	$X_1^T\ Y_3^T$	**Forward**			
		……	$X_2^T\ Y_4^T$			
			……			
				……		
					……	
						$X_{127}^T\ Y_{127}^T$
						MULT
						FFT_32
			$X_2^T\ Y_{255}^T$			Abs
		$X_1^T\ Y_{255}^T$	MULT			Max
32	$X_0^T\ Y_{255}^T$	MULT	FFT_32			alpha_127
32	MULT	FFT_32	Abs			
160	FFT_32	Abs	Max			
16	Abs	Max	alpha_2			
16	Max	alpha_1				
8	alpha_0					
32	X'^T_0 , Y'^T_0					
32	MULT	X'^T_1 , Y'^T_1				

(X, Y are the input signals of size 128*32, streaming into the PE array. alphas are the outputs of size 8*128, which are streaming out of the PE array after processing.)

latency = latency of PE_0

= latency of 1st iteration + latency of iteration 1-127

= (32 + 32 + 160 +16) + (32 + 32 + 160 + 16 + 16 + 8) * 127

= 33,768 cycles = 67.5 us (Fmax = 500MHz, Tmin = 2ns)

Throughput = 1 / 67.5 * 1000000 = 14,814 signals/sec

SIMD instruction scheduling to generate half of the SCD matrix:

Cycle	PE_0	PE_1	PE_2	PE_K	PE_K+1	PE127
32	X_0^T , Y_0^T					
32		X_1^T , Y_0^T				
32			X_2^T , Y_0^T			
32				……		
32					……	
……						
32						X_{127}^T Y_0^T
32	**MULT**					
160	**FFT_32**					
16	**Abs**					
16*128 = 2048	**Abs[0][0]**	**Abs[1][0]**	**Abs[2][0]**	**……**	**……**	**Abs[127][0]**
32	$\boldsymbol{X_0^T}$ $\boldsymbol{Y_1^T}$	$\boldsymbol{X_1^T}$ $\boldsymbol{Y_1^T}$	$\boldsymbol{X_2^T}$ $\boldsymbol{Y_1^T}$	**……**	**……**	$\boldsymbol{X_{127}^T}$ $\boldsymbol{Y_1^T}$
32	MULT					
160	FFT_32					
16	Abs					
16*128 = 2048	Abs[0][1]	Abs[1][1]	Abs[2][1]	……	……	Abs[127][1]
	……	……	……	……	……	……
32	X_0^T Y_{127}^T	X_1^T Y_{127}^T	X_2^T Y_{127}^T	……	……	X_{127}^T Y_{127}^T
32	MULT					
160	FFT_32					
16	Abs					
16*128 = 2048	Abs[0][127]	Abs[1][127]	Abs[2][127]	……	……	Abs[127][127]
32	$\boldsymbol{X'^T_0}$, $\boldsymbol{Y'^T_0}$					
32		$\boldsymbol{X'^T_1}$, $\boldsymbol{Y'^T_0}$				

No. of latency = load latency + (compute latency + output latency + shift latency)*128
= 32 * 128 + (32 + 16*128 + 32) * 128
= 274,432 cycles = 548.9 us (Fmax = 500MHz, Tmin = 2ns)
Throughput = 1 / 548.9 * 1000000 = 1,822 signals/sec