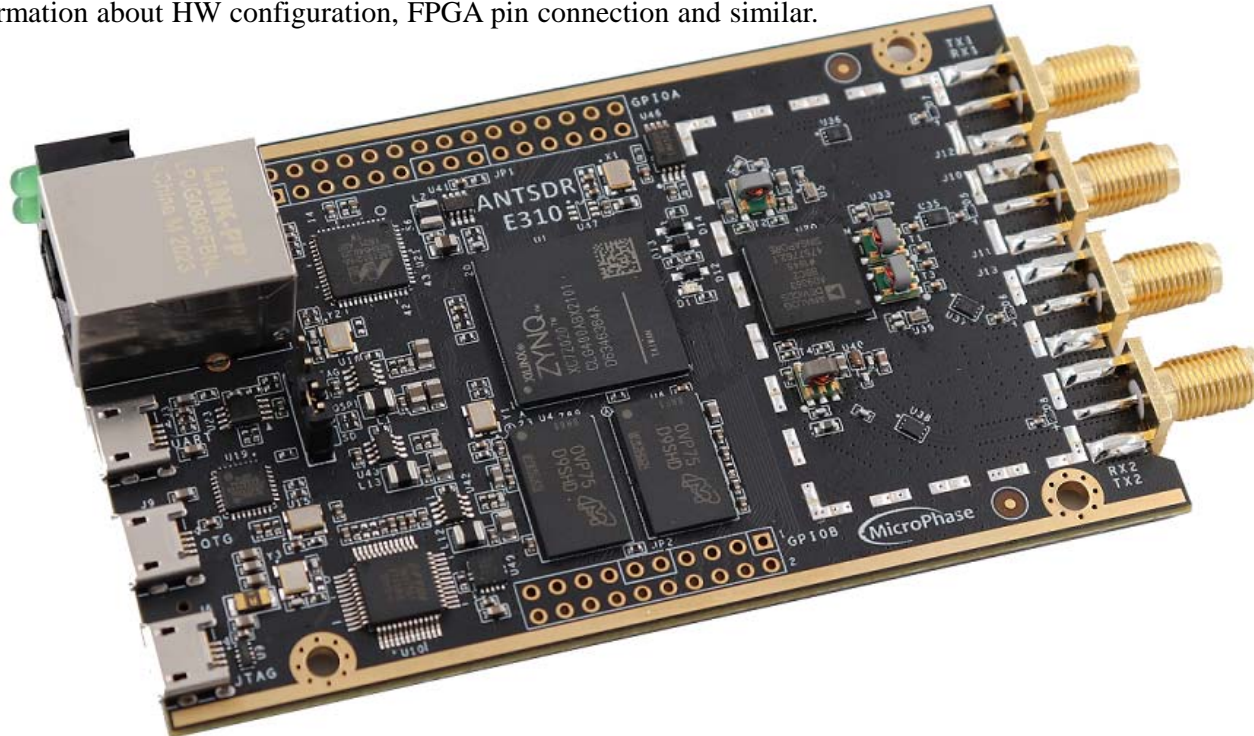


Cover Page

Note:
MicroPhase board HW FULL schematics are not available. MicroPhase has an open source code but not an open hardware schematics. Nonetheless, DEVELOPMENT schematics are available here .

This schematic will give you information about HW configuration, FPGA pin connection and similar.



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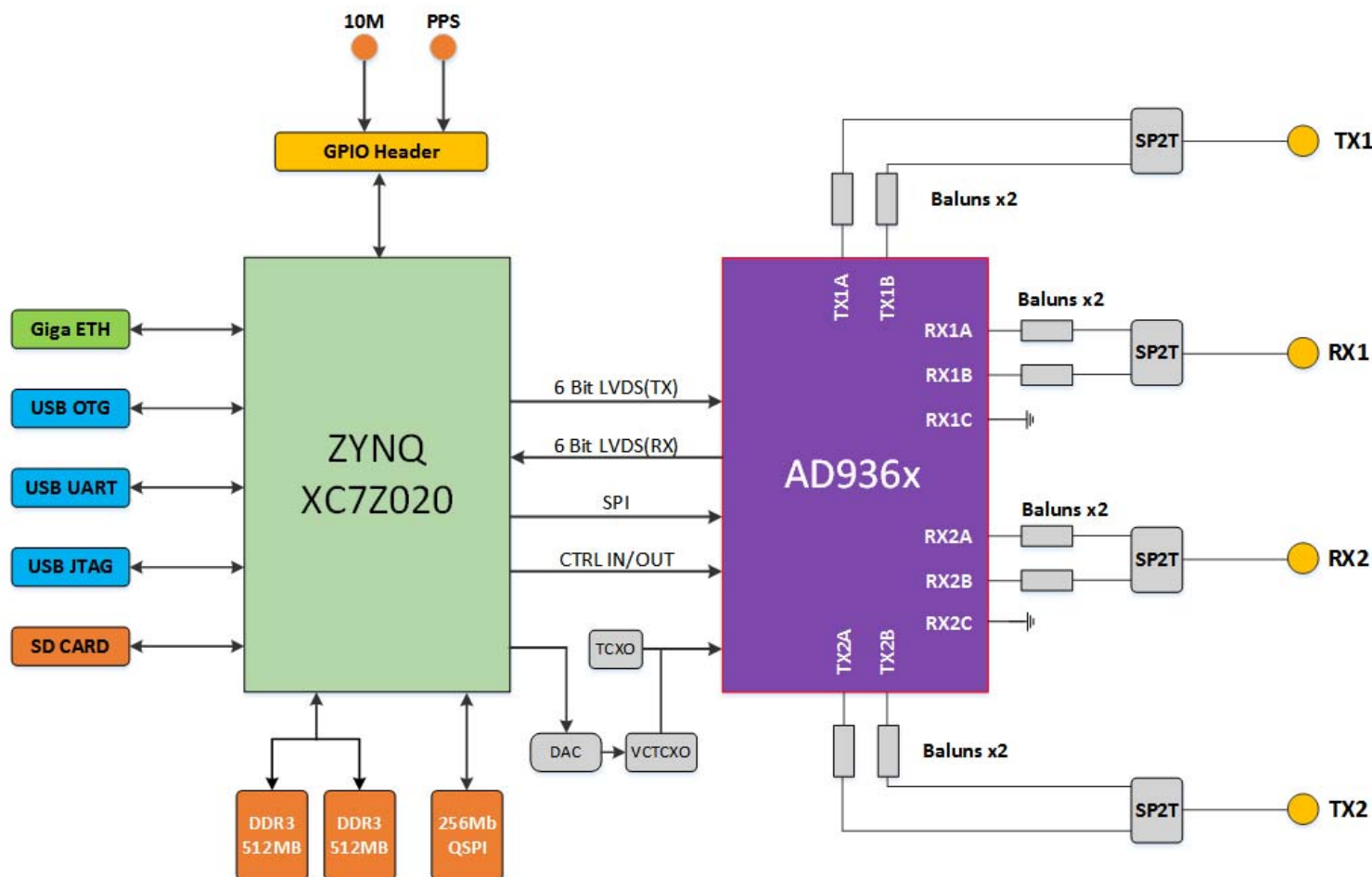
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ANTSDR E310 Block Diagram

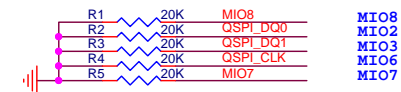
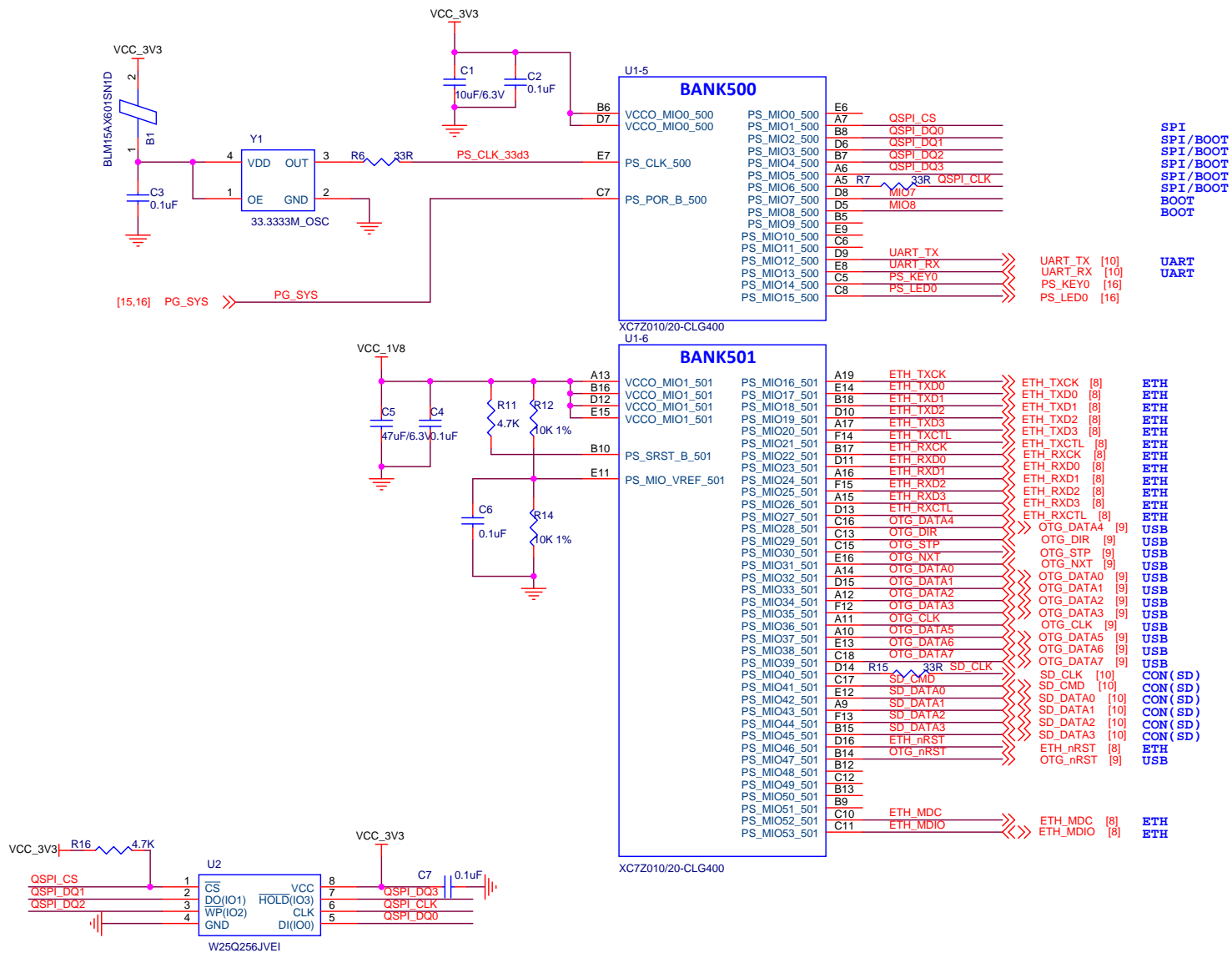
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1.0	07/08/2021	All	Rev 1.0 Release



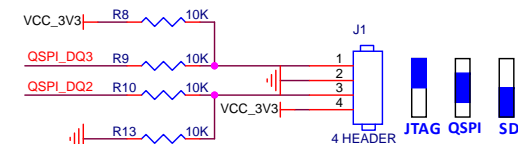
PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	PS BANK500&501
3	PS BANK502
4	PL BANK0&13
5	PL BANK34&35
6	ZYNQ Power
7	DDR3 RAM
8	PS USB
9	UART SD
10	AD936x
11	RF Switch & CON
12	Clock & EX IO
13	USB JTAG
14	Power
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PS B500 B501

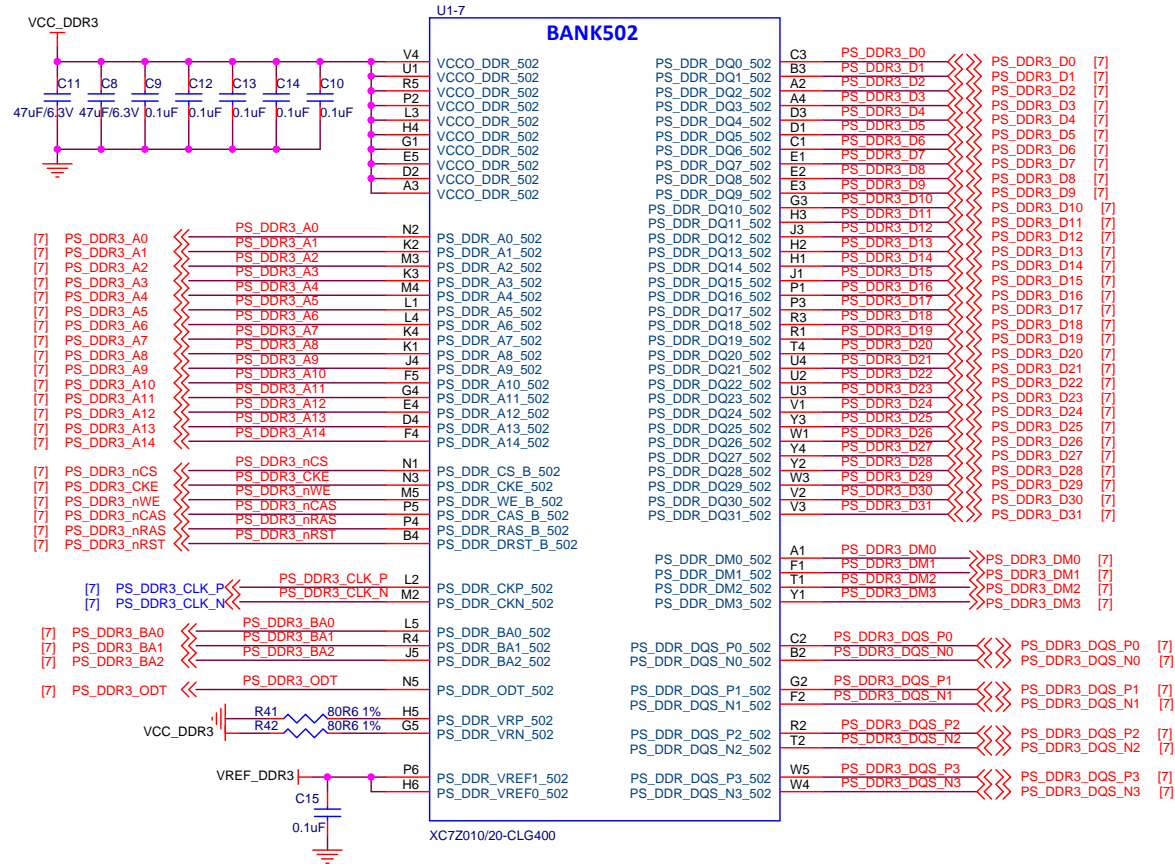


```
MIO[8] = 0 ---MIO bank1 voltage=3.3V
MIO[2] = 0 ---cascaded JTAG
MIO[3] = 0 ---JTAG/NAND/Quad-SPI/SD
MIO[6] = 0 ---PLL used
MIO[7] = 0 ---MIO bank0 voltage=3.3V
```

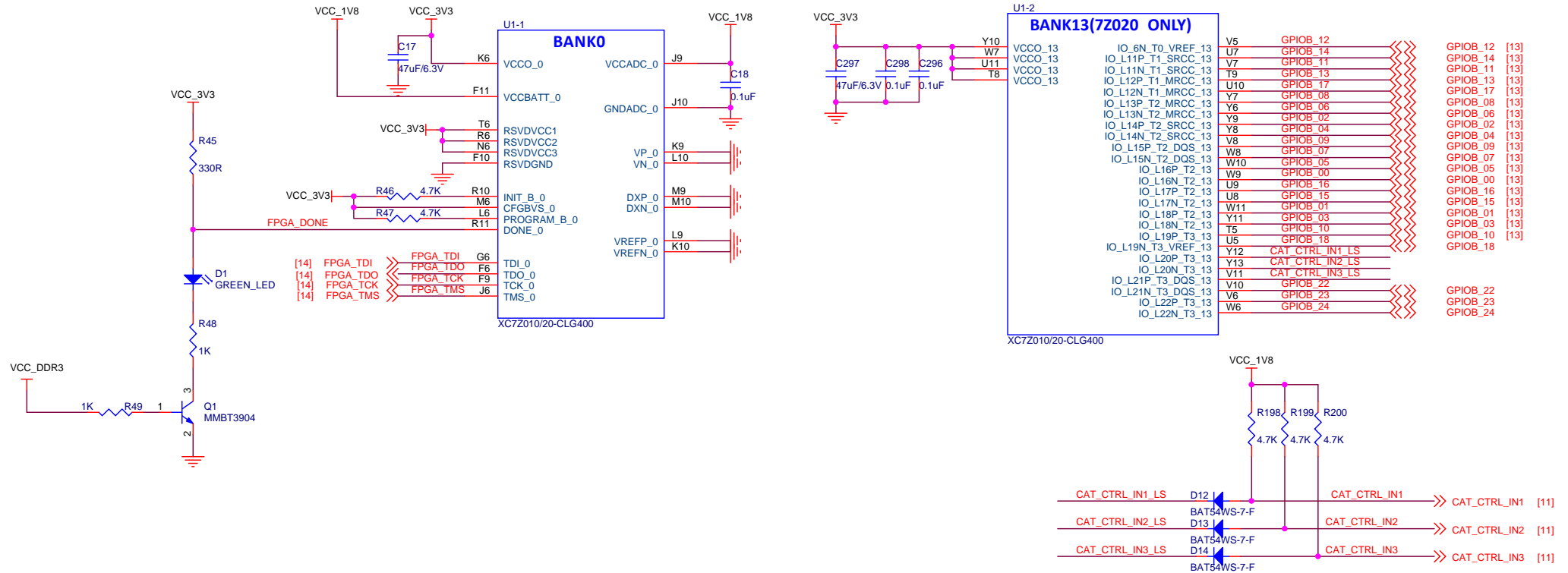


Boot Mode	MIO[5] (QSPI_DQ3)	MIO[4] (QSPI_DQ2)
JTAG	0	0
NAND	0	1
QSPI	1	0
SD Card	1	1

PS B502 DDR3



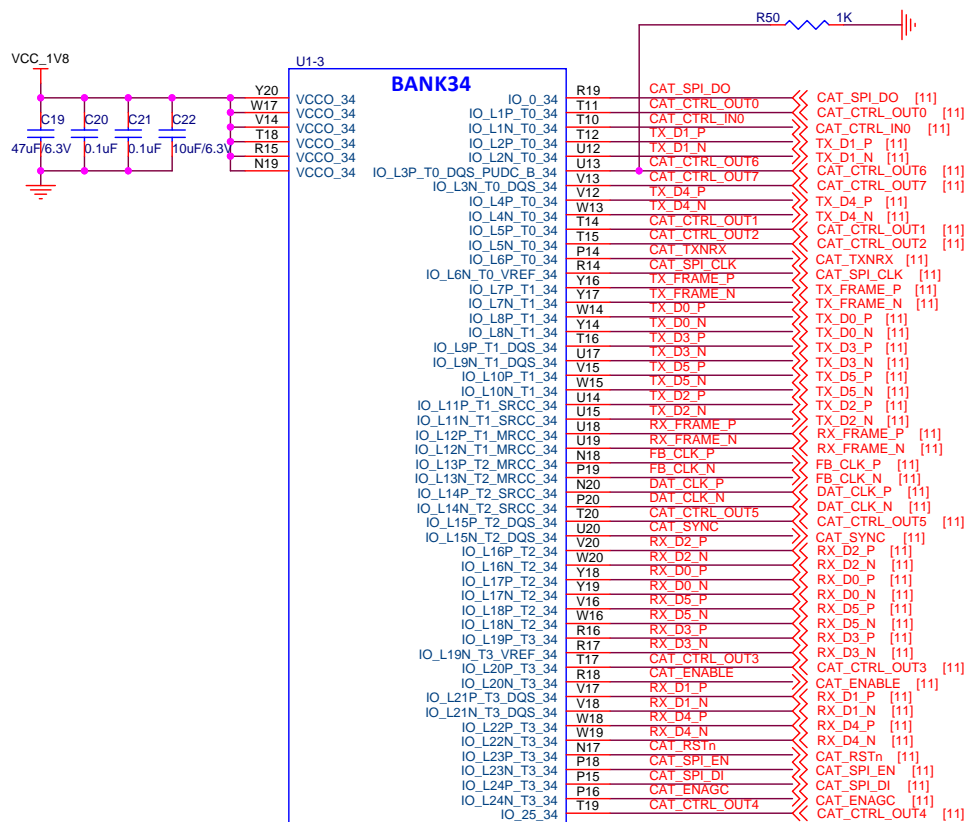
ZYNQ CONFIG



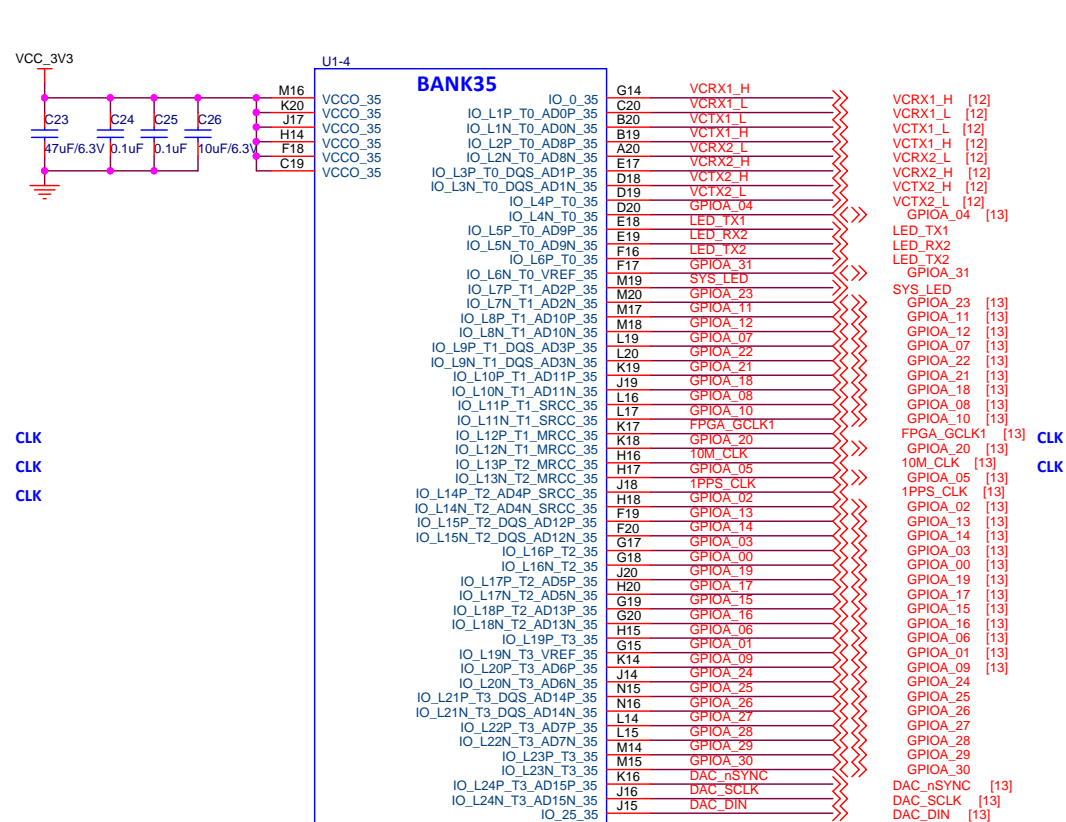
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Title		
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B	PL BANK0&13	1.0
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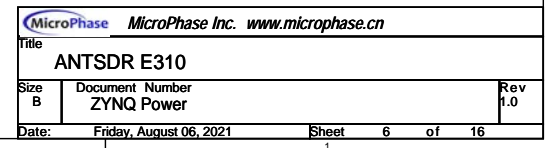
PL B34 B35



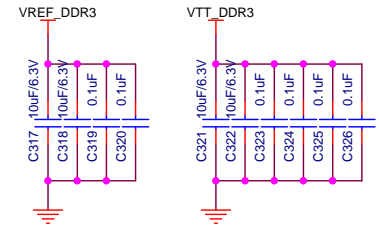
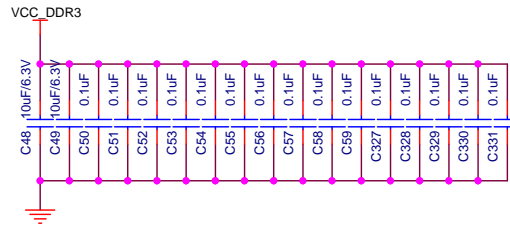
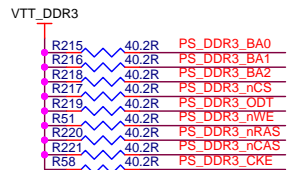
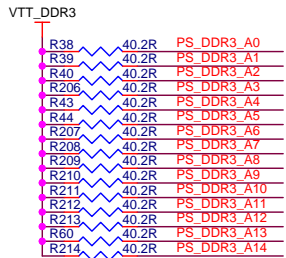
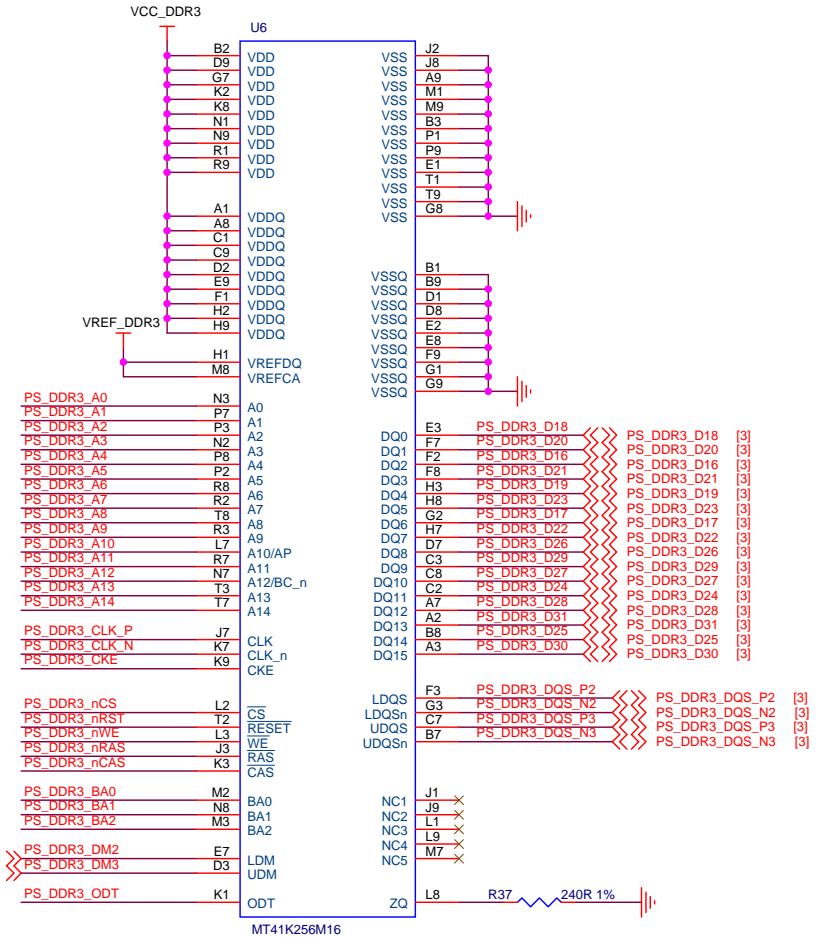
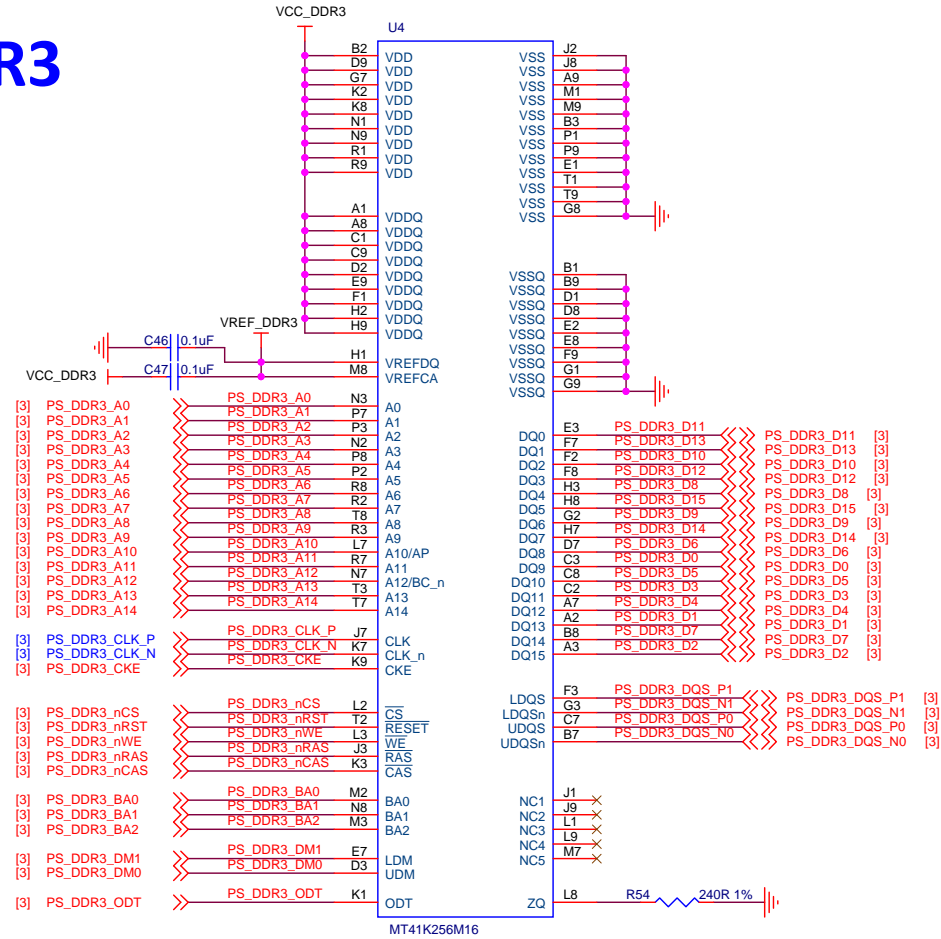
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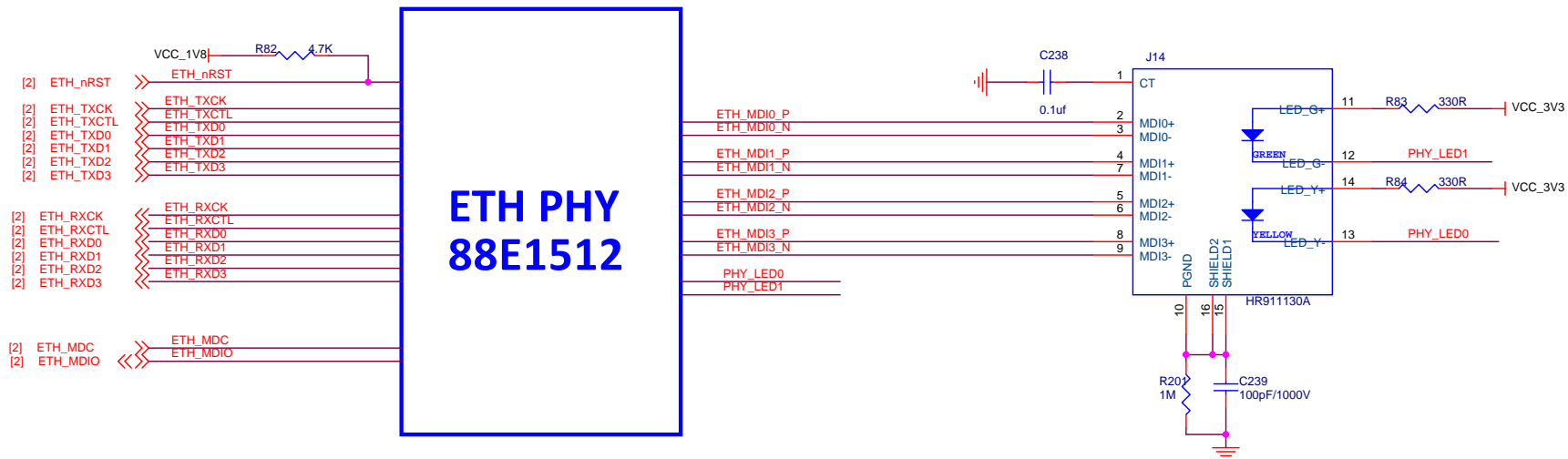
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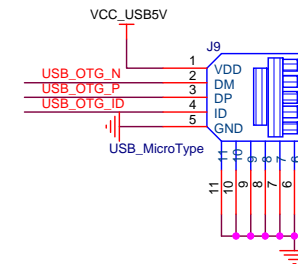
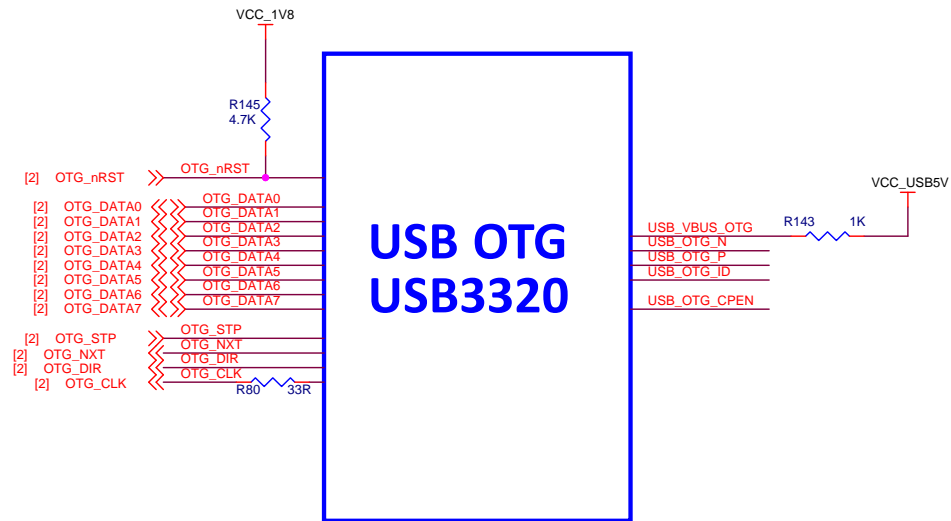
PS_DDR3



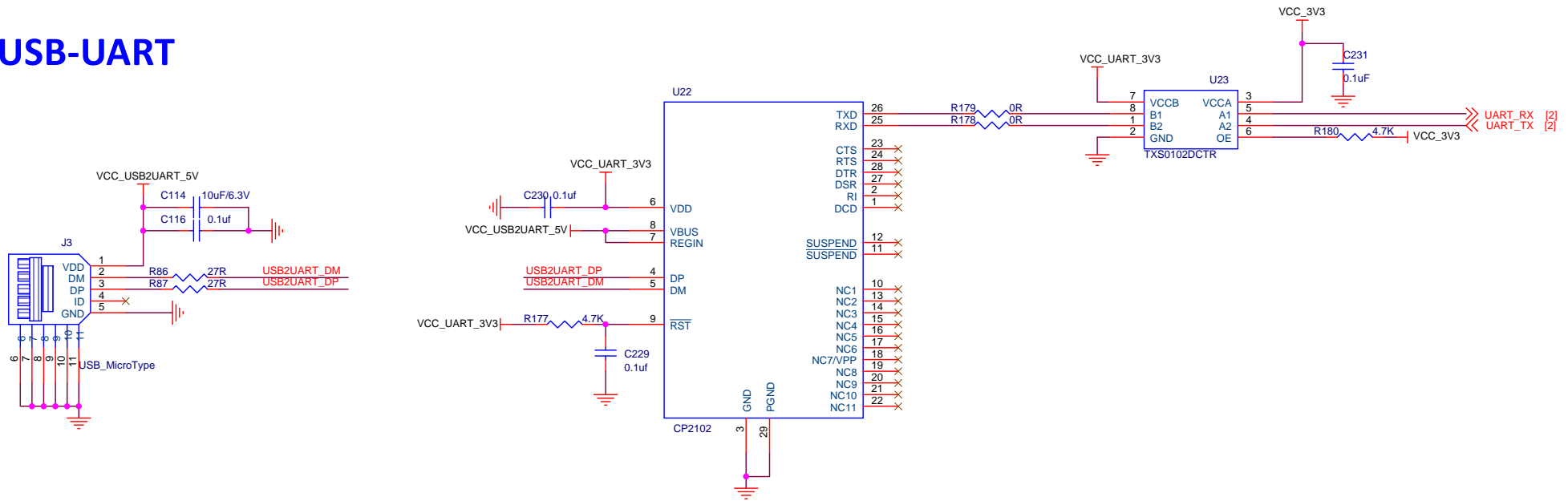
PS ETH



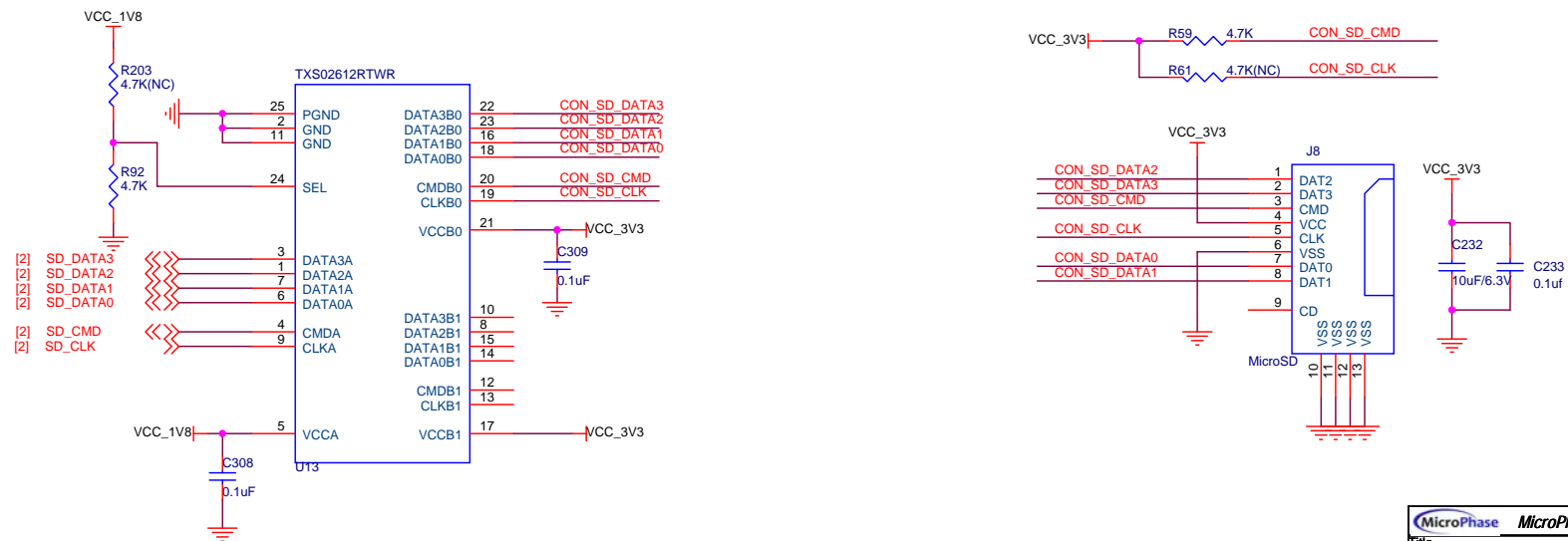
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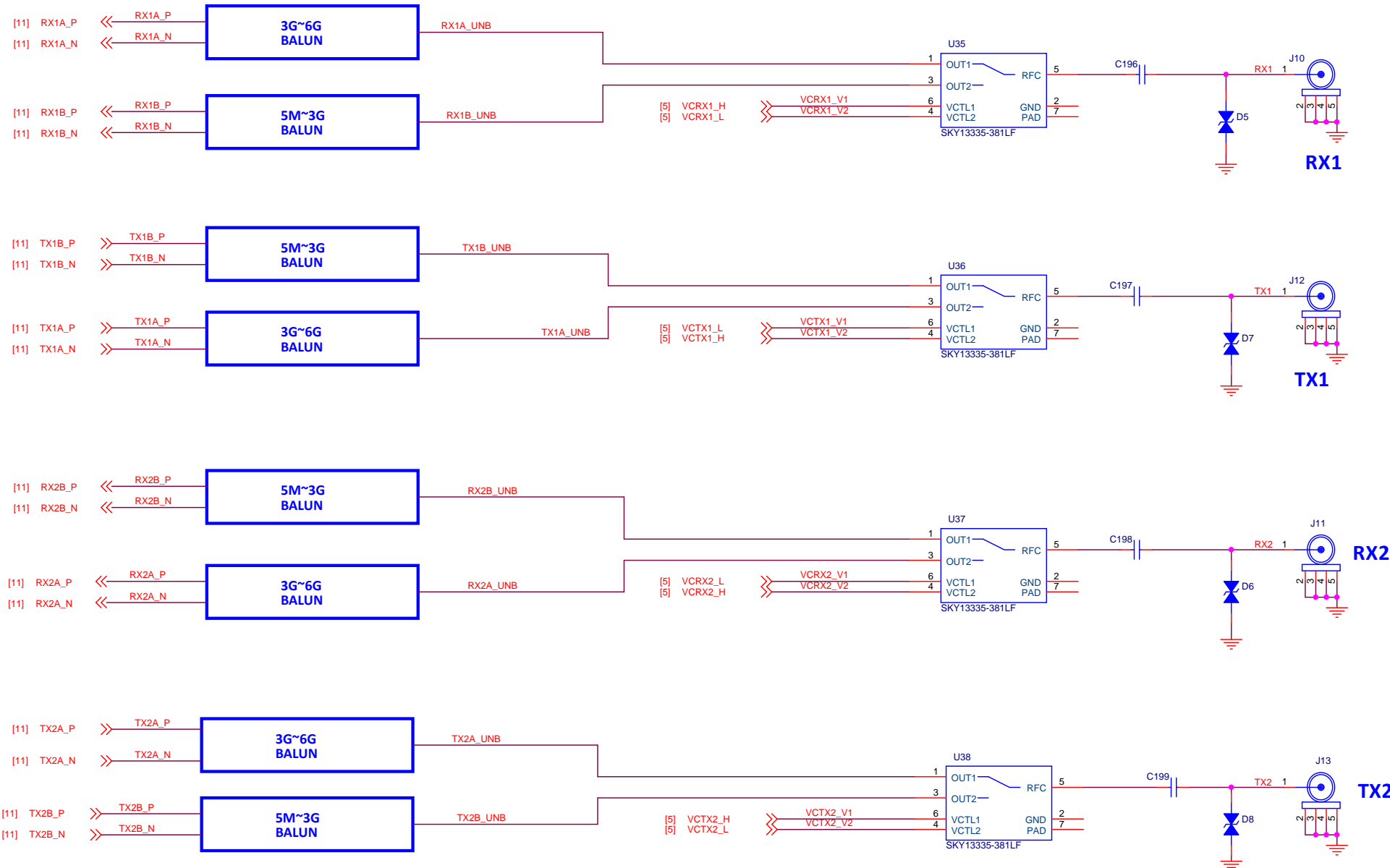


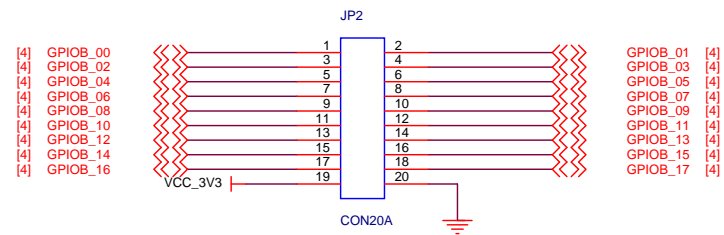
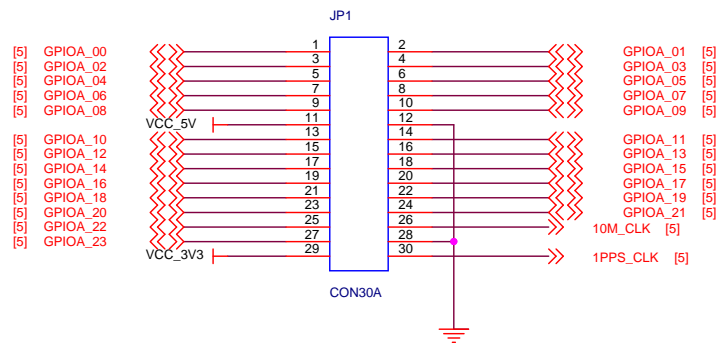
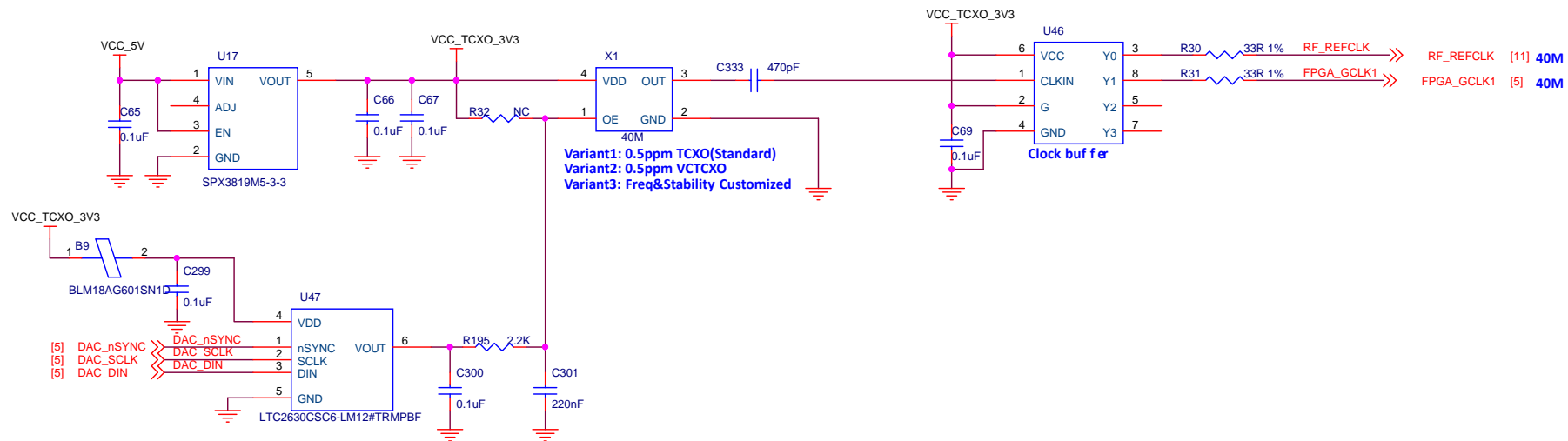
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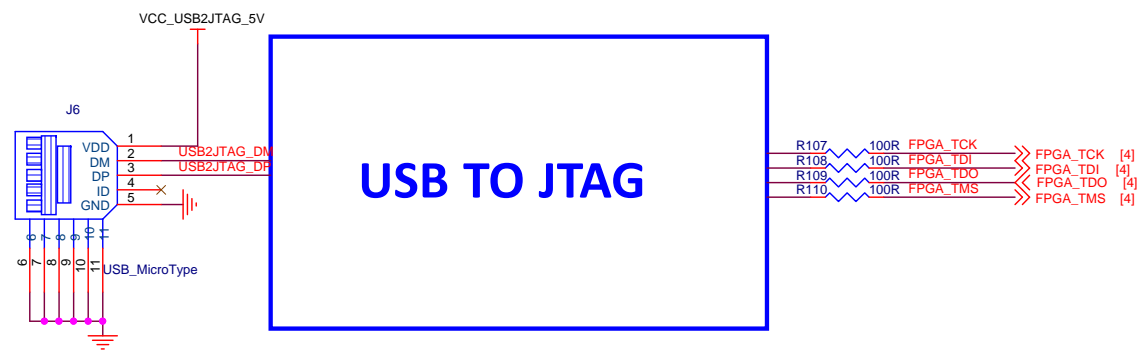
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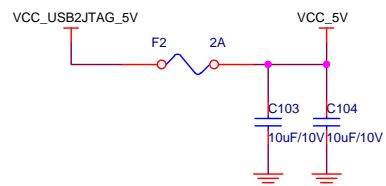





USB JTAG

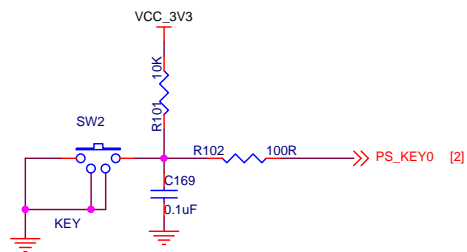


Power From USB Connector(J6)



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Panel KEY



Panel LED

