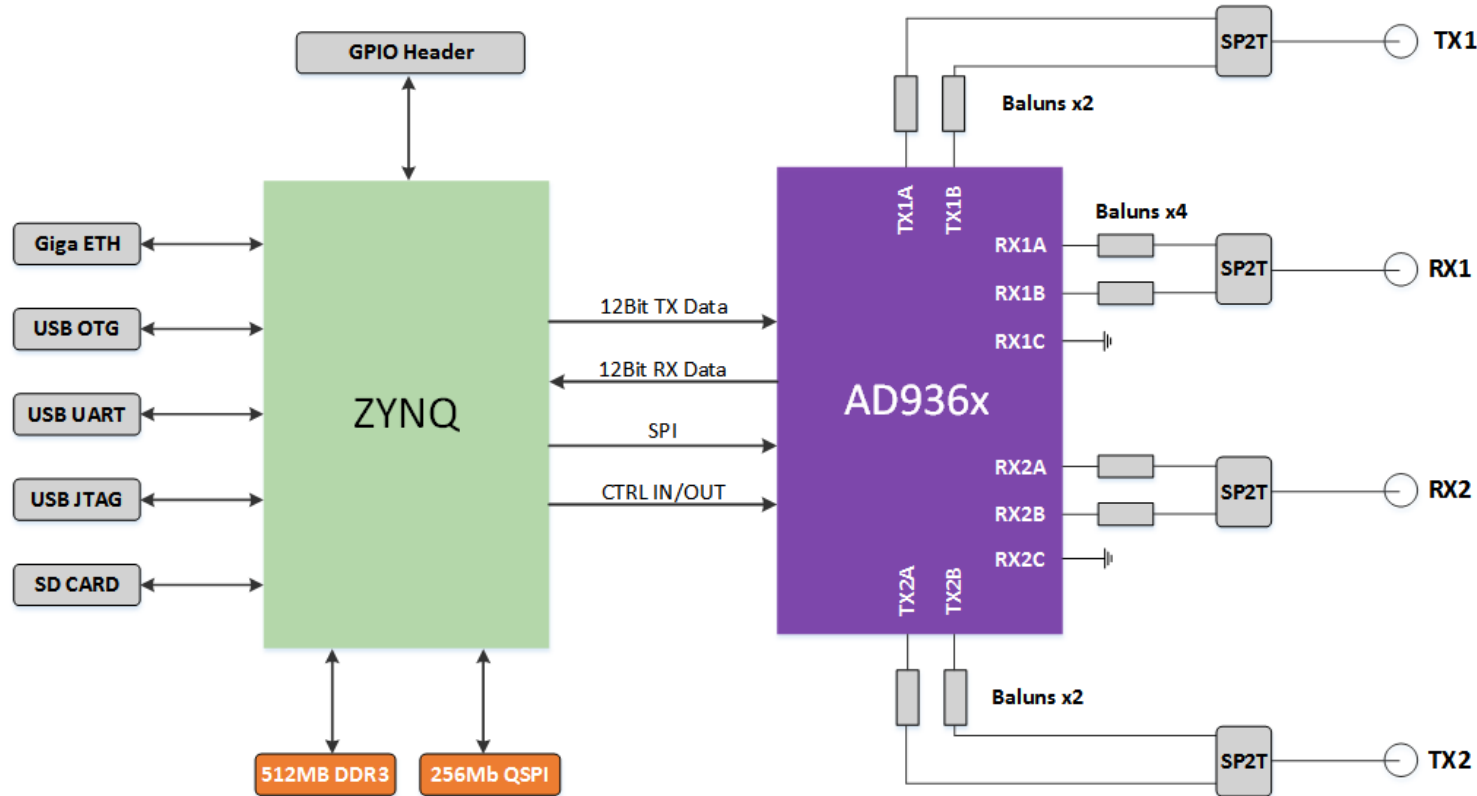


ANTSDR B220 Block Diagram




REV	DATE	PAGES	DESCRIPTION
1.0	27/03/2021	All	Rev 1.0 Release

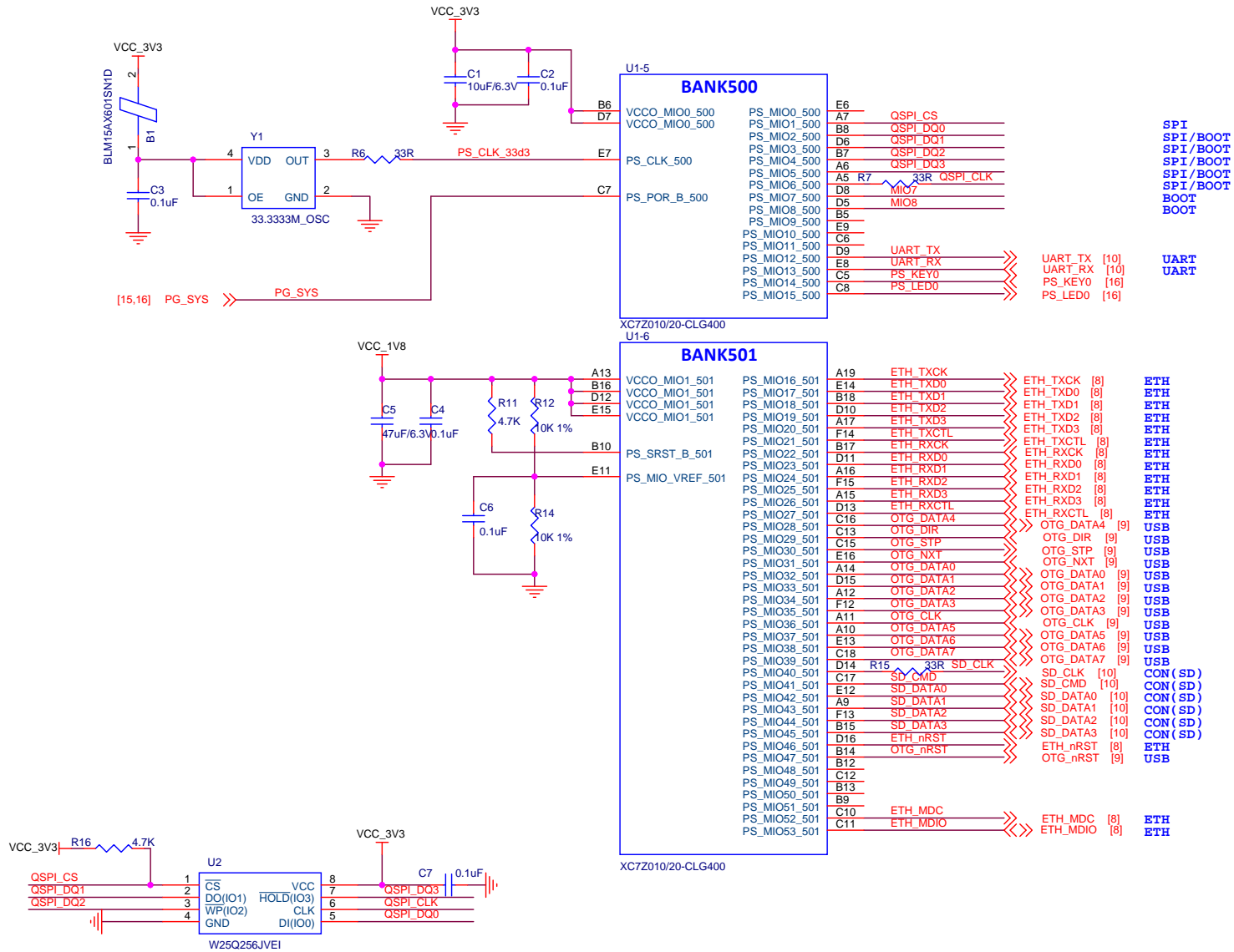
PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	PS BANK500&501
3	PS BANK502
4	PL BANK0&13
5	PL BANK34&35
6	ZYNQ Power
7	DDR3 RAM
8	PS ETH
9	PS USB
10	UART SD
11	AD936x
12	RF TX/RX
13	Clock & EX IO
14	USB JTAG
15	Power
16	Power
17	
18	
19	
20	
21	
22	
23	
24	
25	
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27	
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29	

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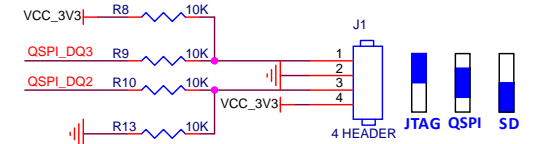
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 <i>MicroPhase Inc. www.microphase.cn</i>	
Title	
ANTSDR B220	
Size B	Document Number Block Diagram
	Rev 1.0
Date:	Tuesday, June 15, 2021
Sheet	1 of 16

PS B500 B501



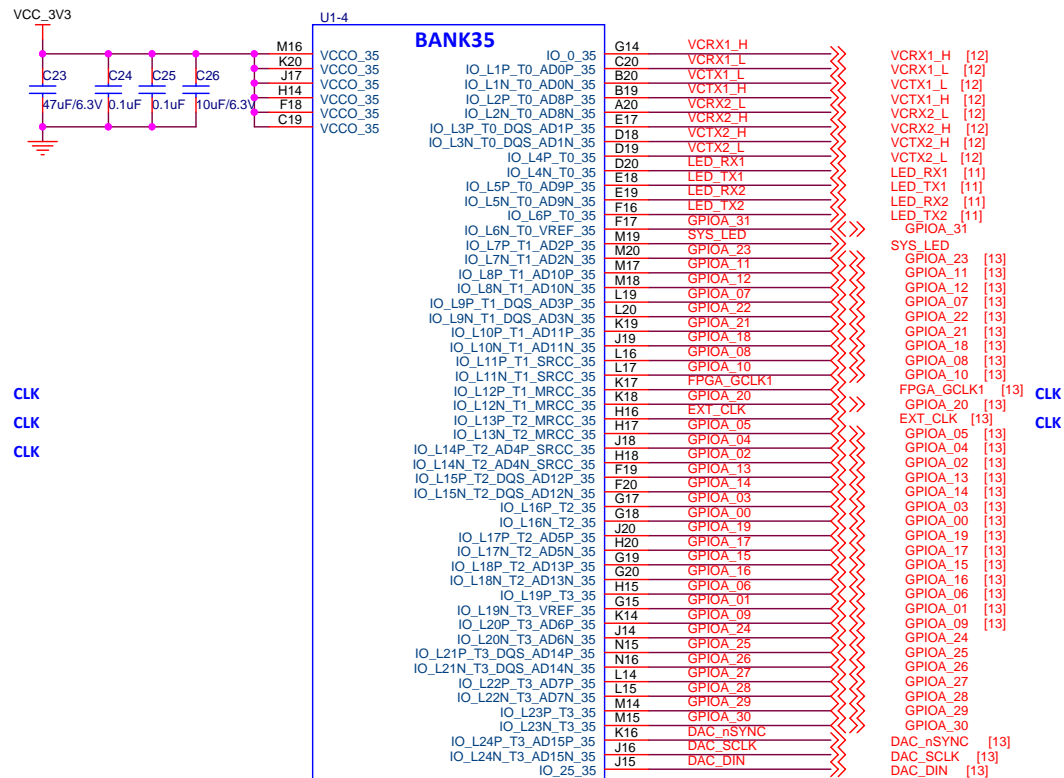
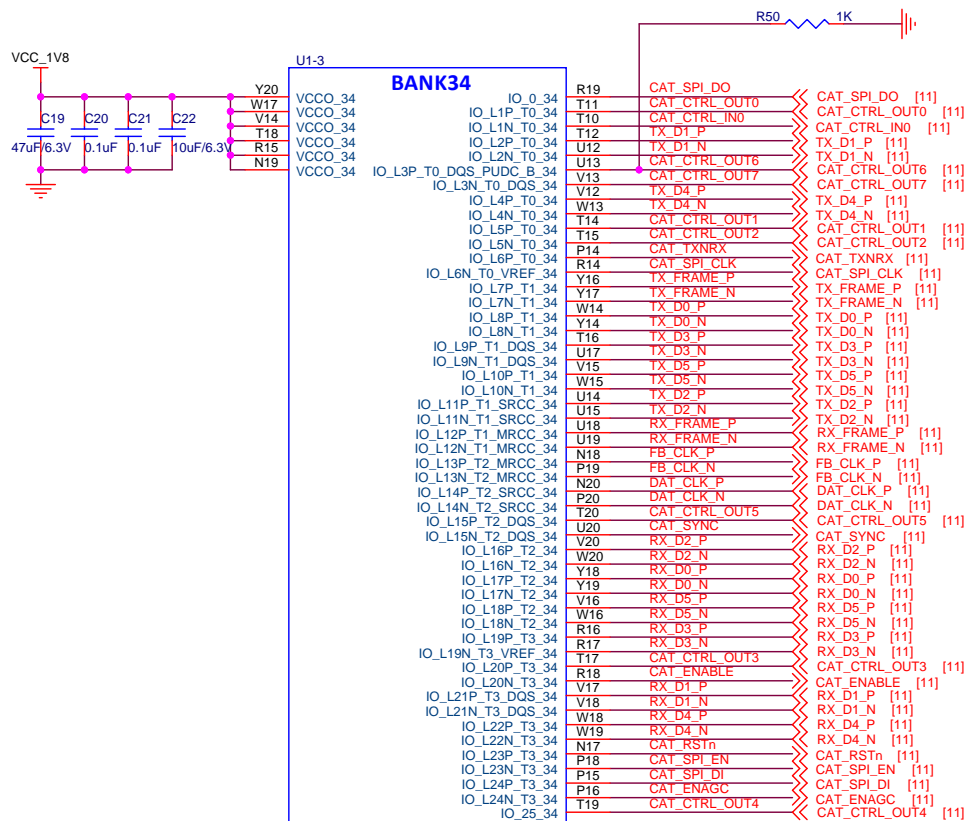
MIO[8] = 0 ---MIO bank1 voltage=3.3V
MIO[2] = 0 ---cascaded JTAG
MIO[3] = 0 ---JTAG/NAND/Quad-SPI/SD
MIO[6] = 0 ---PLL used
MIO[7] = 0 ---MIO bank0 voltage=3.3V



Boot Mode	MIO[5] (QSPI_DQ3)	MIO[4] (QSPI_DQ2)
JTAG	0	0
NAND	0	1
QSPI	1	0
SD Card	1	1

ZYNQ CONFIG

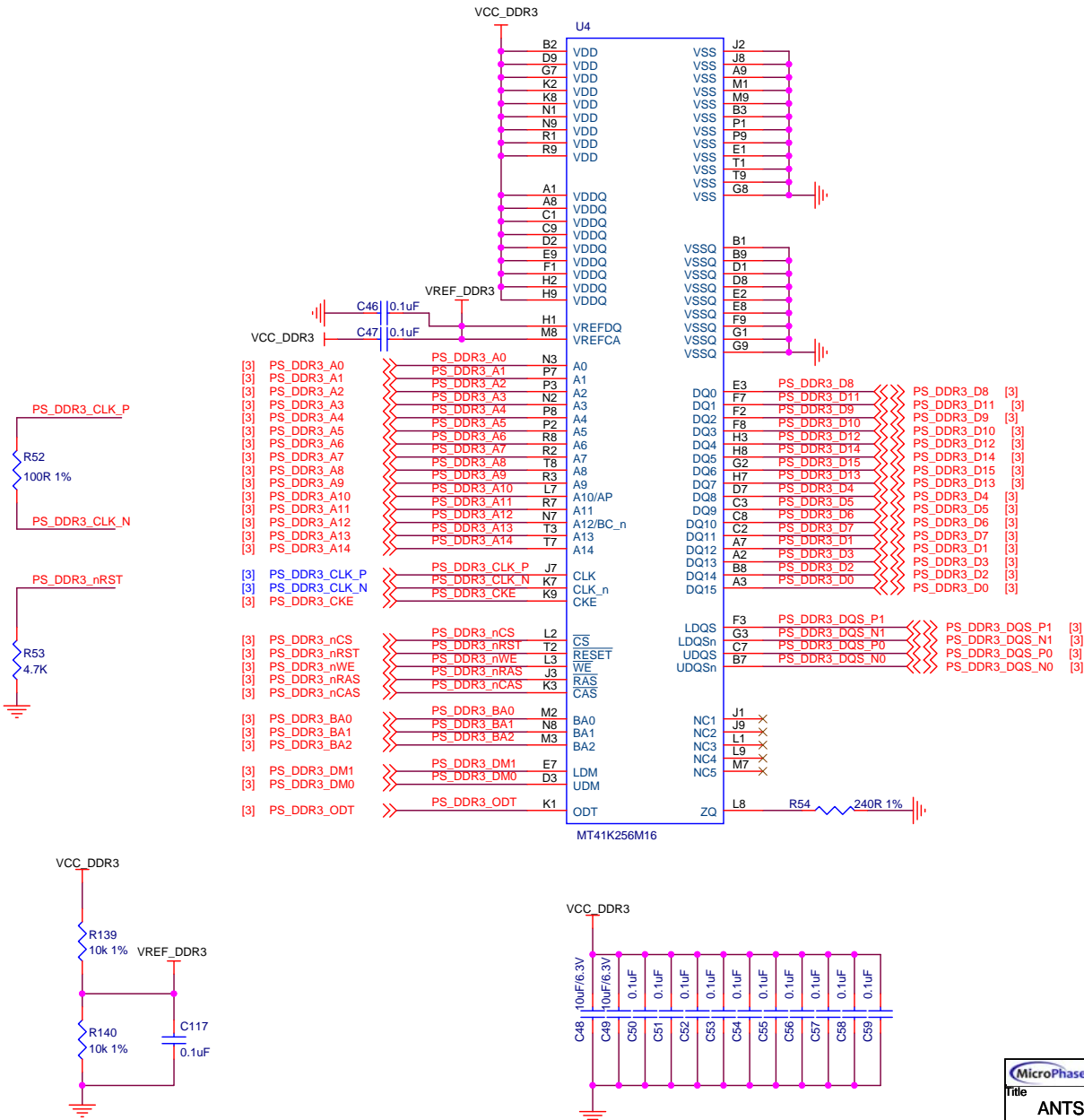
PL B34 B35



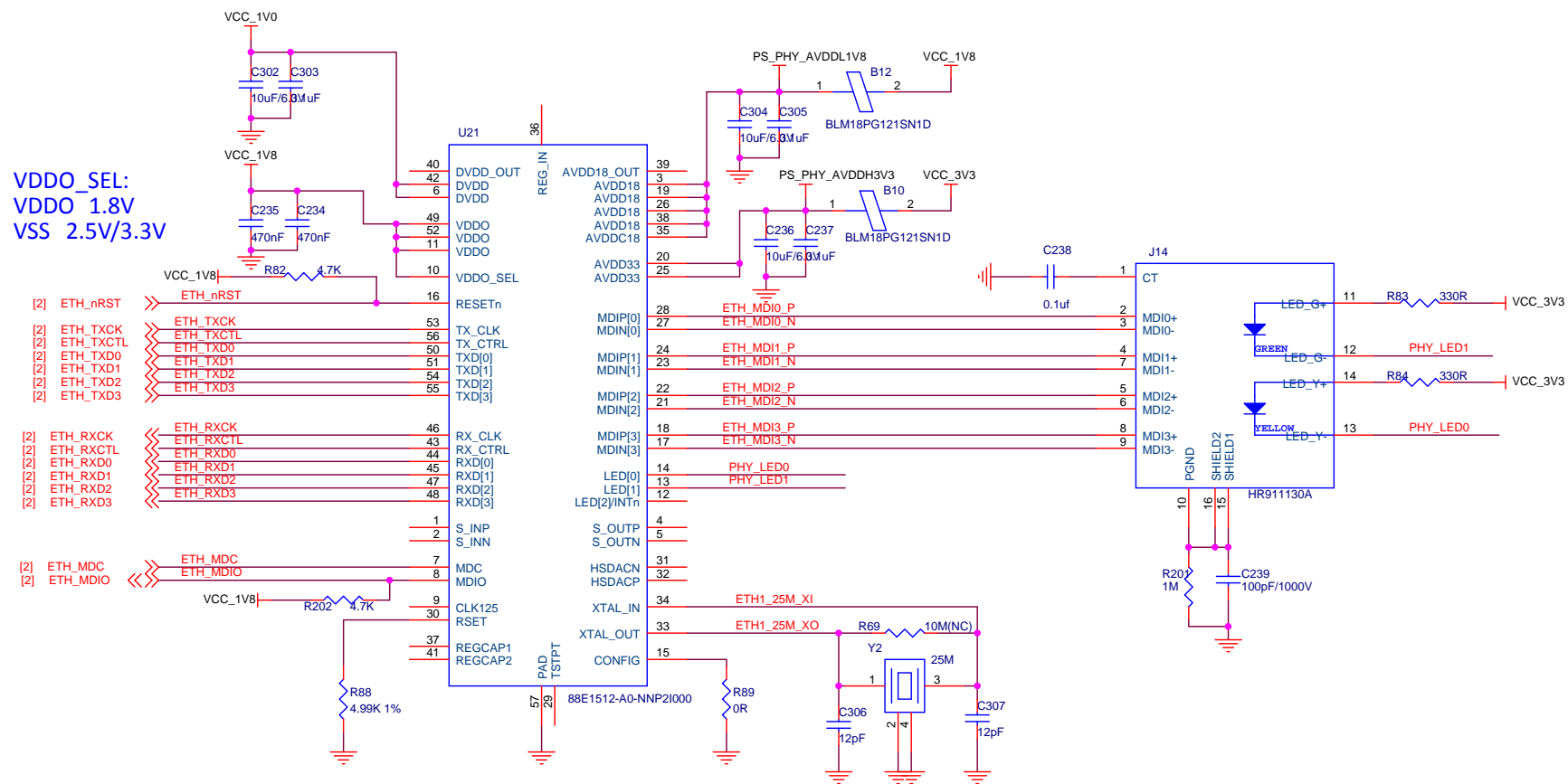
XC7Z010/20-CLG400

XC7Z010/20-CLG400

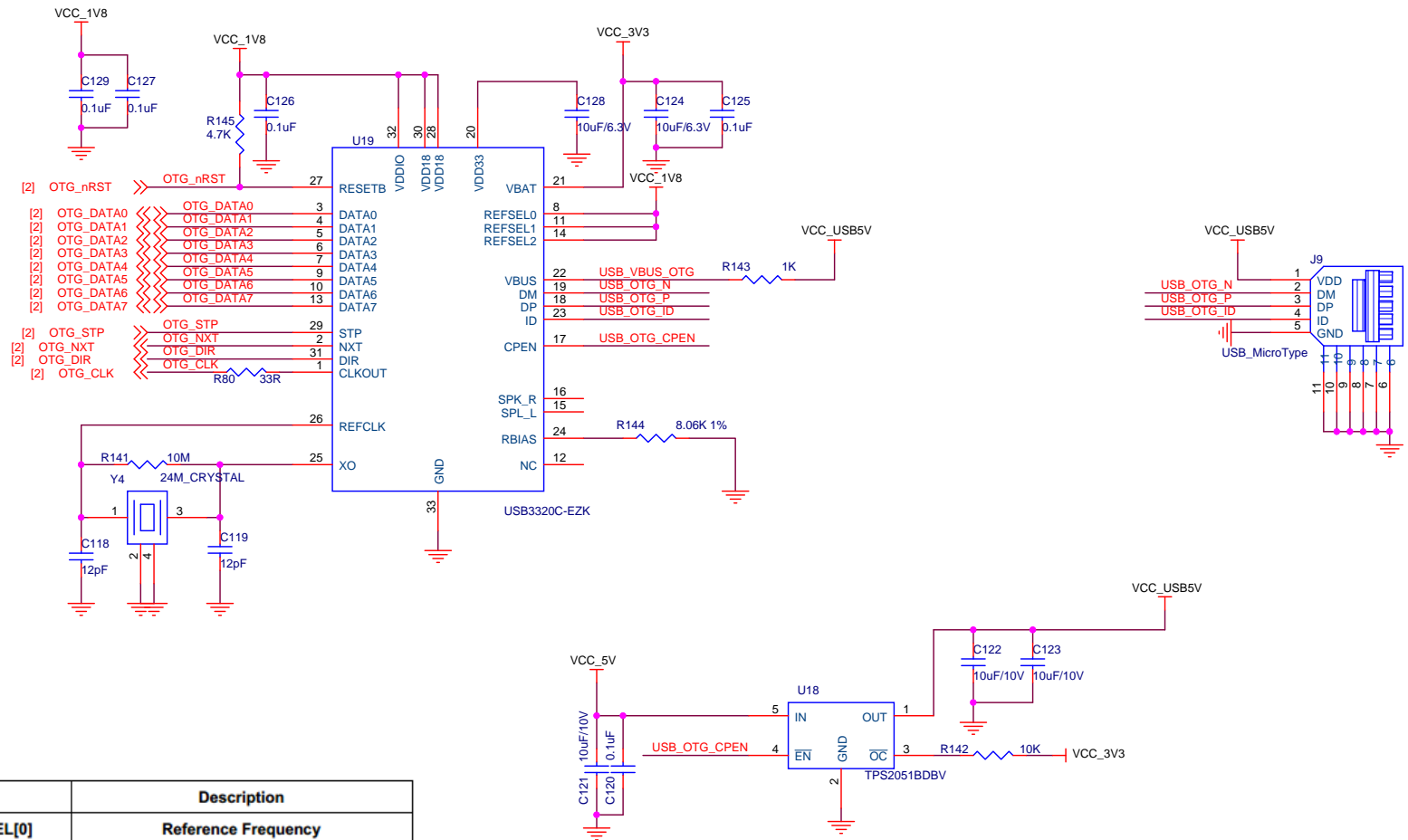
PS_DDR3



PS ETH

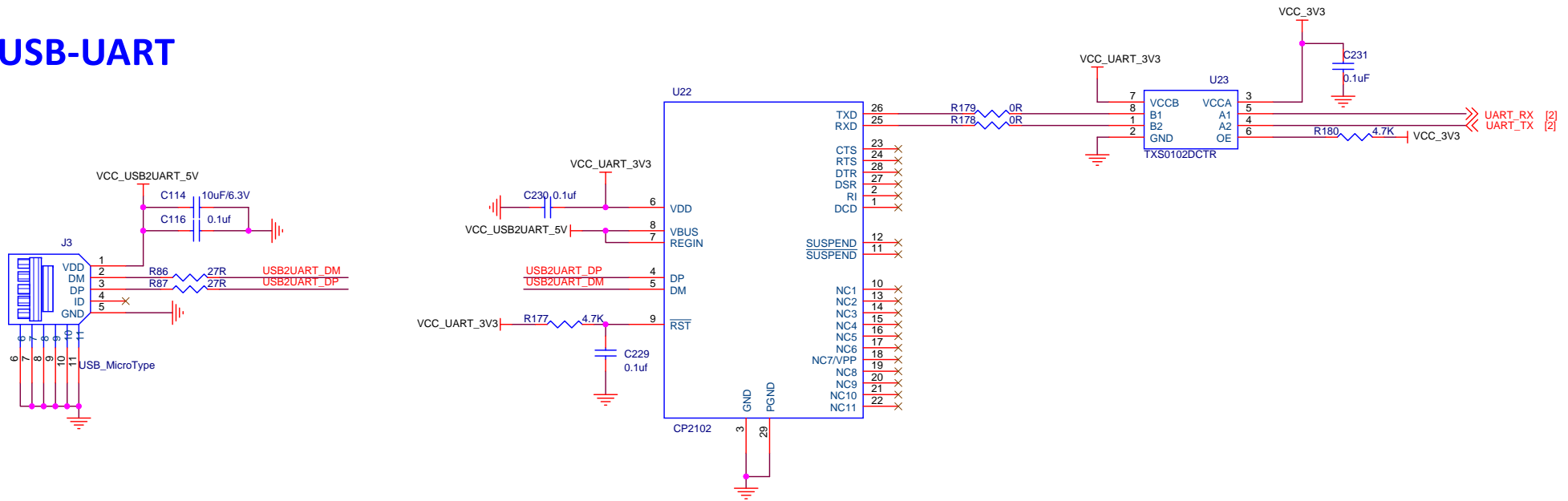


PS USB OTG

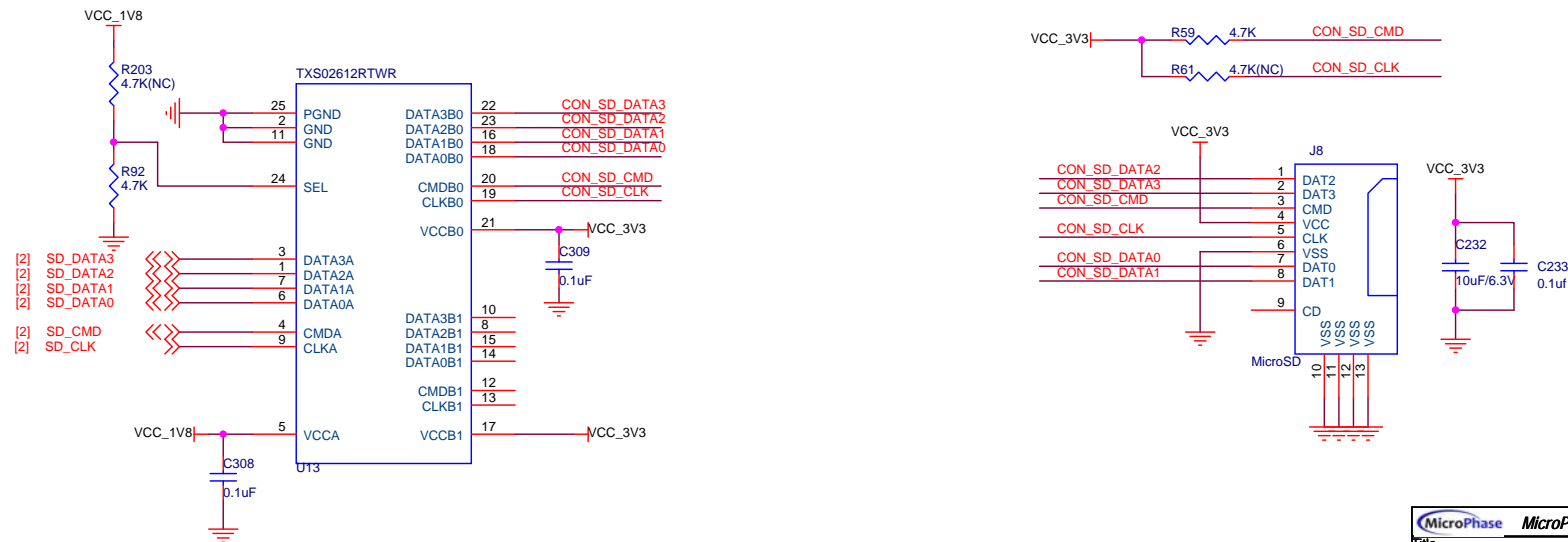


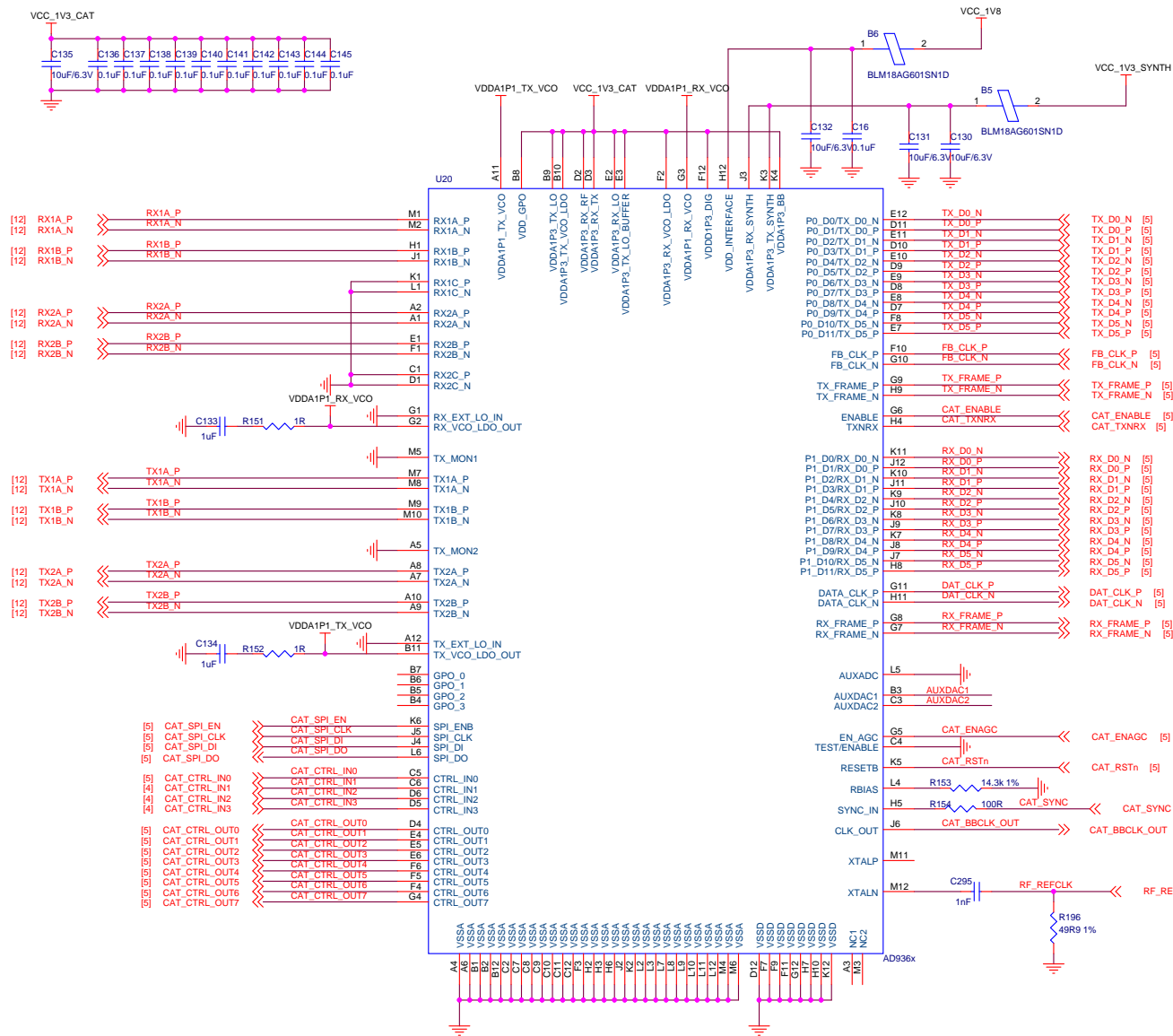
Configuration Pins			Description
REFSEL[2]	REFSEL[1]	REFSEL[0]	Reference Frequency
0	0	0	52 MHz
0	0	1	38.4 MHz
0	1	0	12 MHz
0	1	1	27 MHz
1	0	0	13 MHz
1	0	1	19.2 MHz
1	1	0	26 MHz
1	1	1	24 MHz

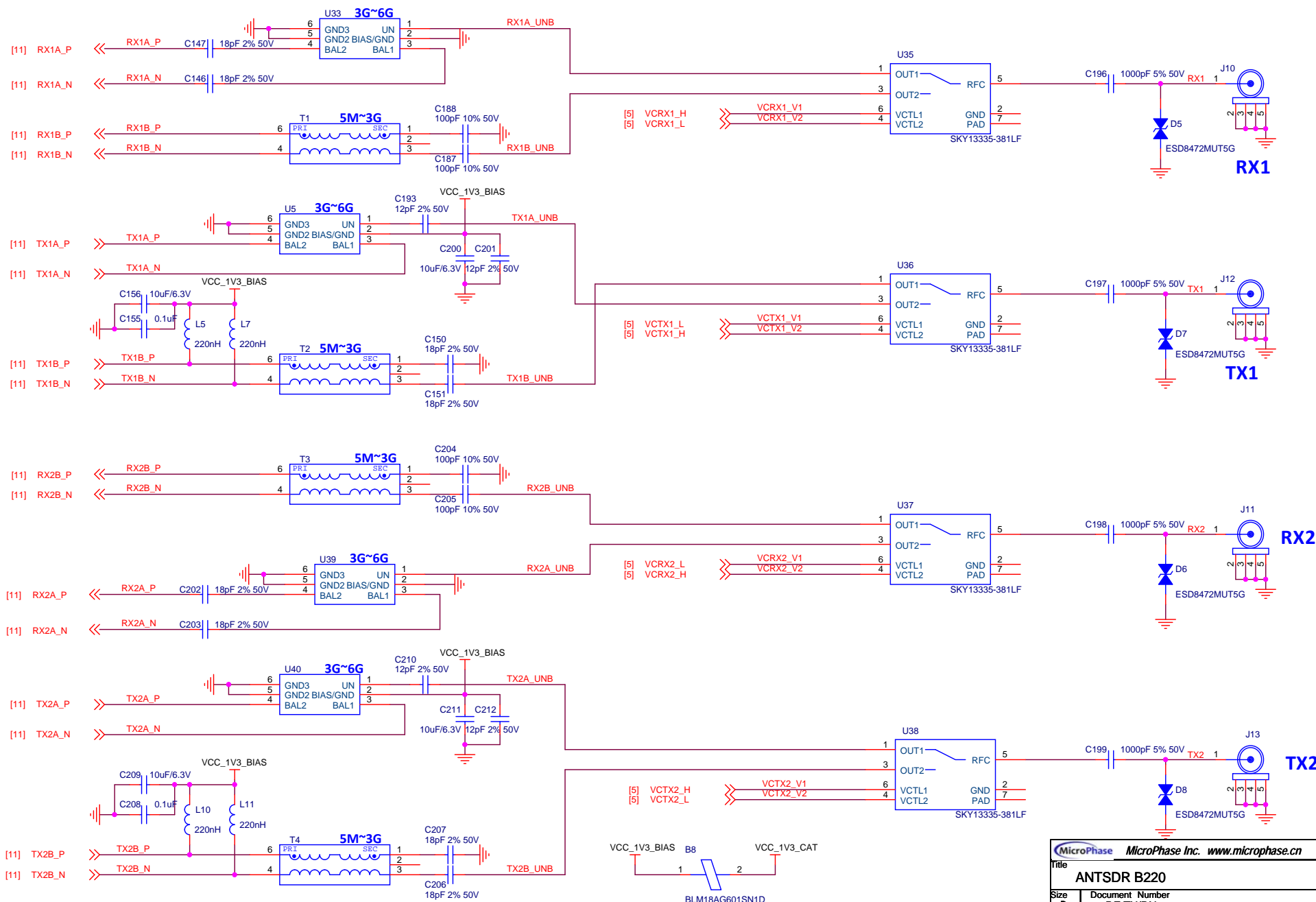
USB-UART

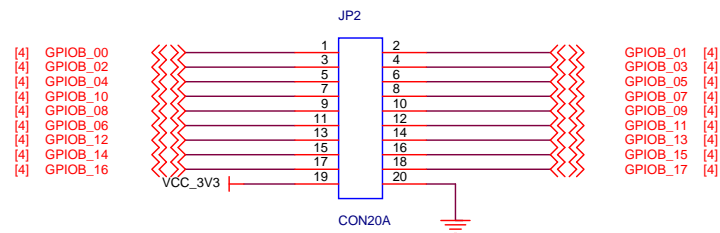
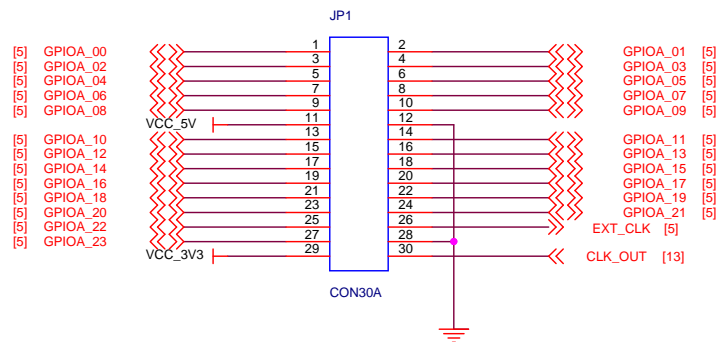
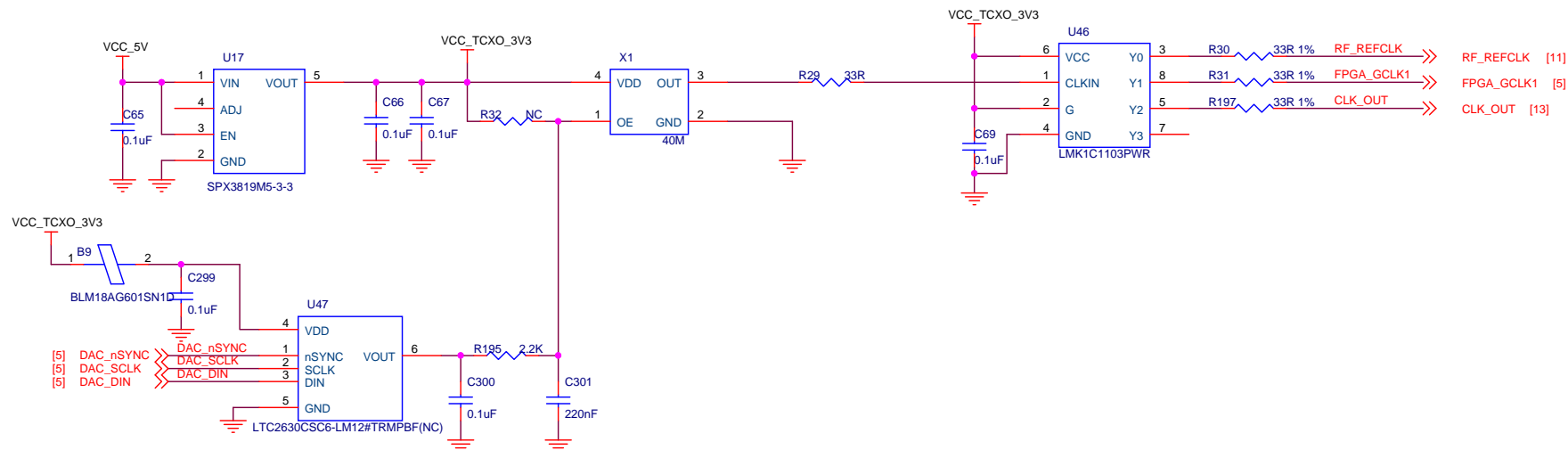


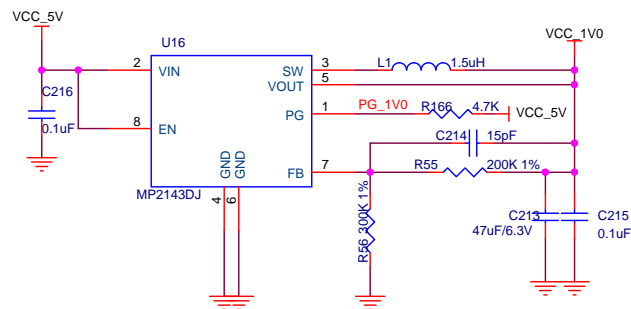
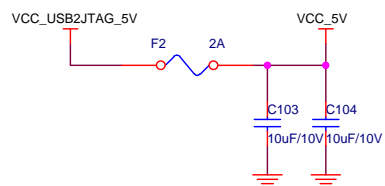
SD CARD



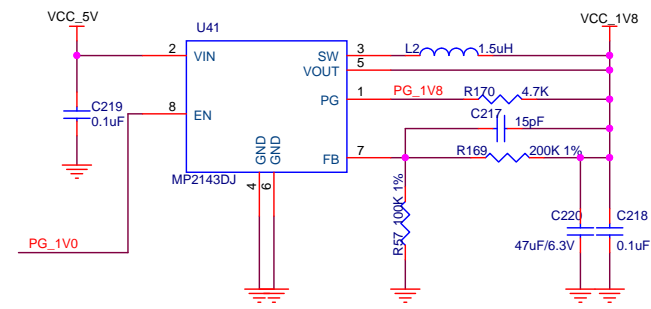




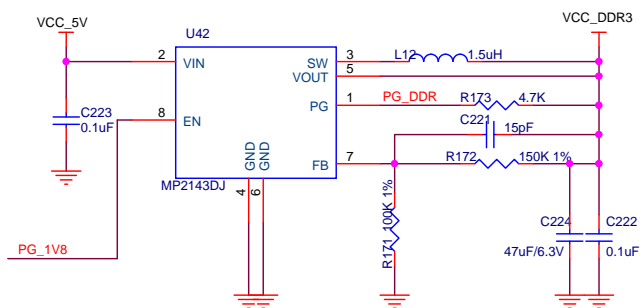




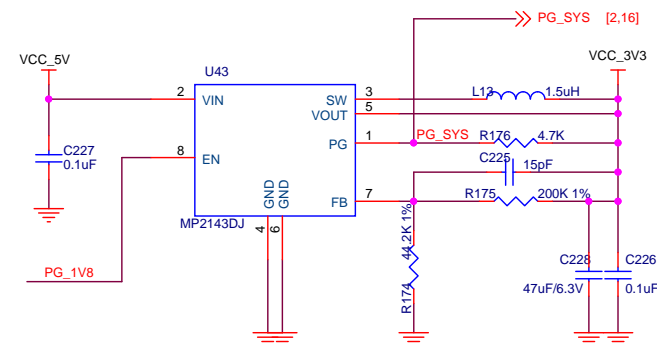
Vref = 0.6V VOUT = 1.0V



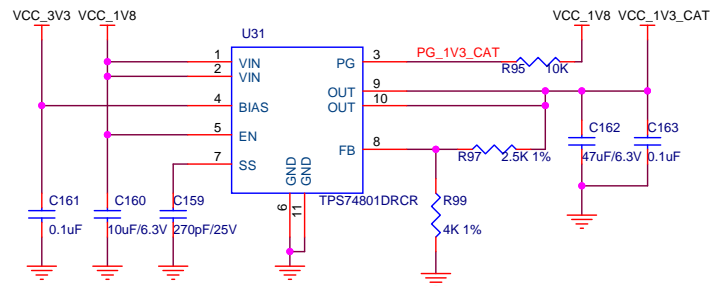
Vref = 0.6V VOUT = 1.8V



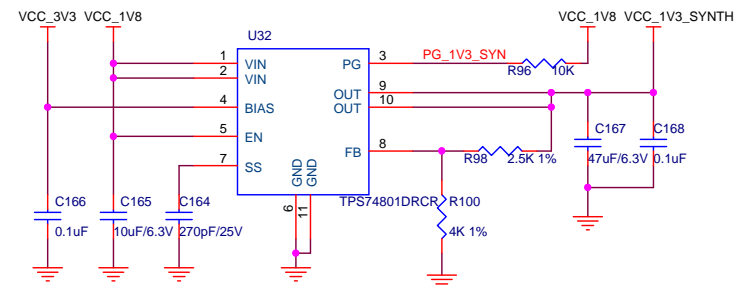
Vref = 0.6V VOUT = 1.5V



Vref = 0.6V VOUT = 3.3V



Vref = 0.8V, VOUT = 1.0V



Vref = 0.8V, VOUT = 1.0V

Panel RST

