Date: 2021/05/11

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~7

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Github updates since last meeting:

Issues discussed in meeting:

Discussed compliance simulations. Use macros to setup interrupts to abstract interrupt setup from test and would be platform responsibility to define the macros. Could also add a non-deterministic compliance sim that does a repeating sequence of instructions and a sanitized trap handler e.g., signature checks trap did happen and was right one but doesn't check epc or other values that could change based on implementation differences. Try to discuss more with Bill McSpadden next time.

#155 – Discussed triggers. Shelve for now until we can discuss with Tim from debug TG Questions like what is protocol of 16 bit interface to debug module.

Closed #154 – to avoid complicating critical code paths in privileged layer handling virtual memory, do not want to have to distinguish between CLIC vector table reads from other. updated spec in meeting.

Closed #141 based on previous spec update.

#91 - have linux group review example DTS entry.

Specification updates in meeting and since last meeting:

#154 – added text that clarifies behavior when inhv is set when returning from a ret instruction.

Open issue status:

Issues that can be closed?

#29 – Interrupt trigger in the trigger module – closed with pull #126?

#49 – clarification of memory map – closed with pull #129? Related to new issue #148

#77 – additional detail on CLIC M/S/U memory mapped regions – closed with pull #129?

#79 – supervisor/user mode alignment – closed with pull #129?

#48 – logic/state diagram for clicintip signals (related to #149?), closed with spec update clarifying behavior of the clicintip bit?

Need spec updates:

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG.

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #145 tries to close. need to clarify stvec.mode, utvec.mode register behavior when mtvec.mode switches?

#75 – move hw vectoring to separate section in spec

#107 – heritage of features

#142 – effect of MPRV and SUM on hardware vector table access. load has to obey MPRV and SUM bits. Add this clarification to the spec.

#149 – 32-bit writes to memory-mapped CLIC registers. need to add to spec: A 32-bit write is legal. However, there is no specified order in which the effects of the individual byte updates take effect.

Need more discussion:

#50 – xcause save privilege modification bits

#96 – proposed reformat of cliccfg

#97 – proposed reformat of xcause CSRs

#98 – name of CLIC (related to #109?)

#99, 100, 101, 102, 103, 106 – enhancements

#139 – shadow general purpose registers (GPR) for interrupts?

#140 – automated GPR save/restore?

#148 – Elaborate address map possibilities

Issues related to work in other TGs:

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too?

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – closed with pull #130? have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#155 – clarify inttrig details. discuss with Tim from debug group. Invite Tim to fast-interrupt TG meeting to discuss.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#108 – pushint/popint?