

Date: 2021/04/27

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~10

Current issues on github: <https://github.com/riscv/riscv-fast-interrupt/issues>

Previous meeting minutes: <https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes>

Fast Interrupt DoD (Definition of Done) Status:

<https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG>

Github updates since last meeting:

New file: test-plan-clic.adoc

New file: riscv-test-suite/rv32i_m/Ziclic_unratified/src/clic_priv.S

We will start with discussion of CLIC compatibility tests next meeting (5/11/2021)

Issues discussed in meeting:

#149 – (related to #48) normally setup attribute ahead of time. Comments: A 32-bit write is legal. However, there is no specified order in which the effects of the individual byte updates take effect. Need to update Spec.

#152 (2nd part of #149) - changing from edge to level, what happens to pending? Only the current values of clicintip affect the interrupt processing. Closed with spec update clarifying behavior of the clicintip bit.

#153 (based on 2nd part of #149 continued) - what happens to clicintip value when switching from edge to level and back to edge. The state in clicintip is undefined in this case. Closed with spec update.

At end of the meeting we had a minor discussion of CLIC test plan/ Definition of Done (DoD) compliance.

- Current proposed test-plan-clic.adoc does simple, minimal testing. E.g. Only does synchronous tests, tests if CLIC registers can be set, and checks if it vectors to the correct address.
- But async behavior and debug are extremely important and where the bugs are. Bugs mean incompatibility and fragmentation. Isn't it important that compliance covers items at highest risk of compatibility?
- Since every pipeline will take an interrupt in a different place, it can't be verified trivially. For actual verification to know CLIC is functioning correctly, need to have a

way of testing async behaviors. Should CLIC have a standalone test? Generic test harness? Unit testing of behavioral component called the CLIC?

- Should more pseudo-code be added directly to the CLIC spec so that the pseudo-code can be ported directly to SAIL?

Specification updates since last meeting:

Pull #150 - Updated adoc format to align with risc-v template, added revision history. clic.pdf updated

Pull #147 for issue #45 - for rev1.0 mtvec not xtvec controls enabling CLIC mode for all priv

Pull #146 for issue #141 - N-extension vs Bare S-mode note added.

Pull #138 for issue #107 - Added Bibliography section (#107 kept open. more heritage of features items still need to be added).

Pull #132 for issue #117, #125 fix - change text to match table in M/S/U system if nmbits==1

Clicintip clarifications (for issues #152, 153).

Open issue status:

Issues that can be closed?:

#29 – Interrupt trigger in the trigger module – closed with pull #126?

#49 – clarification of memory map – closed with pull #129? Related to new issue #148

#77 – additional detail on CLIC M/S/U memory mapped regions – closed with pull #129?

#79 – supervisor/user mode alignment – closed with pull #129?

#91 – DTS entry – closed with pull #130?

#141 – add commentary on bare-s mode – closed with pull #146?

#48 – logic/state diagram for clicintip signals (related to #149?), closed with spec update clarifying behavior of the clicintip bit?

Need spec updates:

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG.

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #145 tries to close. need to clarify stvec.mode, utvec.mode register behavior when mtvec.mode switches?

#75 – move hw vectoring to separate section in spec

#107 – heritage of features

#149 – 32-bit writes to memory-mapped CLIC registers. need to add to spec: A 32-bit write is legal. However, there is no specified order in which the effects of the individual byte updates take effect.

Need more discussion:

#50 – xcause save privilege modification bits

#96 – proposed reformat of cliccfg

#97 – proposed reformat of xcause CSRs

#98 – name of CLIC (related to #109?)

#99, 100, 101, 102, 103, 106 – enhancements

#139 – shadow general purpose registers (GPR) for interrupts?

#140 – automated GPR save/restore?

#142 – effect of MPRV and SUM on hardware vector table access

#148 – Elaborate address map possibilities

Issues related to work in other TGs:

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too?

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#108 – pushint/popint?