Date: 2021/05/25

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~8

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/TECH/Fast+Interrupts+TG

Next meeting agenda (6/8/21)

Imperas would like to share how they test ints in verilog testbenches and ISS.

Email question (move to priv group instead of fast-int group?) :

> Is there an update about the RNMI proposal? What is the status of it? Since end of January I don't see anything about it.

Moving from kickoff to plan? validation with SAIL, Zephyr OS? Hypervisor support?

Github updates since last meeting:

Issue #156 opened. priv/clic mem mapped registers clarification

Issues discussed in meeting:

#155 – clarify inttrig details. Entire meeting discussed CLIC trigger details with Tim from debug group. CLIC, trigger module, and hart need to be tightly integrated since these features need to be in the core to get sync behavior. discussion on where the details are written down. E.g. CLIC spec describes set of interrupts selected for interface to debug, debug specifies what happens on that event (enter debug mode, start trace, stop trace). For now, keeping abstract action in CLIC, debug takes concrete action. try do discuss more over email reflector.

Specification updates since last meeting:

#142 – added text that vector table load obeys MPRV and SUM.

#149 – added text that 32-bit writes to CLIC registers are legal but effects not defined.

Open issue status:

Issues that can be closed?

#29 – Interrupt trigger in the trigger module – closed with pull #126?

#49 – clarification of memory map – closed with pull #129? Related to new issue #148, #156

#77 – additional detail on CLIC M/S/U memory mapped regions – closed with pull #129?

#79 – supervisor/user mode alignment – closed with pull #129?

#48 – logic/state diagram for clicintip signals (related to #149?), closed with spec update clarifying behavior of the clicintip bit?

#142 – effect of MPRV and SUM on hardware vector table access. load has to obey MPRV and SUM bits. Add this clarification to the spec.

#149 – 32-bit writes to memory-mapped CLIC registers. need to add to spec: A 32-bit write is legal. However, there is no specified order in which the effects of the individual byte updates take effect.

Need spec updates:

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos. Pull #144 tries to fix typos and clarify text. Discuss in TG.

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select. Pull #145 tries to close. need to clarify stvec.mode, utvec.mode register behavior when mtvec.mode switches?

#75 – move hw vectoring to separate section in spec

#107 – heritage of features

Need more discussion:

#50 – xcause save privilege modification bits

#96 – proposed reformat of cliccfg

#97 – proposed reformat of xcause CSRs

#98 – name of CLIC (related to #109?)

#99, 100, 101, 102, 103, 106 – enhancements for future versions?

#139 – shadow general purpose registers (GPR) for interrupts?

#140 – automated GPR save/restore?

#148 – Elaborate address map possibilities

#156 – Clarify isolation mechanism over CLIC memory mapped registers

Issues related to work in other TGs:

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism? remove mclicbase too?

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#91 – DTS entry – closed with pull #130? have linux group review DTS example.

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

#155 – clarify inttrig details. discuss with Tim from debug group. Invite Tim to fast-interrupt TG meeting to discuss.

Issues waiting on ratification (encoding/opcode consistency review needed)

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#108 – pushint/popint?