Date: 2021/04/13

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Kevin Chen

Number of Attendees: ~6

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Next meeting 4/27/2021 we would like to discuss CLIC simulation and testing. (Allen Baum, Imperas please let me know if you can't attend so we can reschedule)

Specification updates since last meeting:

Pull 128 – for now all privilege modes must run in either CLIC or all in non-CLIC mode.

Pull 129 – removed clic m/s/u memory map recommendations and added commentary that it is a platform issue.

Pull 131 – Added on hardware vector traps, both tval and epc hold faulting address.

Pull 132 – made text match table: in M/S/U, when nmbits is 1 MSB selects between M and S.

Pull 133 – added text comparing CLIC to Advanced Interrupt Architecture (AIA)

Pull 134 - modified description of inhv to not define micro-architectural behavior of inhv.

Pull 136 – added example DTS entry to appendix

Pull 137 – added CLIC reset behavior section

Issues discussed in meeting:

Closed issue #117, #125 (text did not match table) based on pull #132

Closed issue #47 clic reset behavior based on pull #137

Closed issue #26 (xINHV) based on pull #134 and pull #131

Closed issue #87 (vector table page faults) based on pull #131

Closed issue #105 (inhv) based on pull #131

Closed issue #111 (vector table fault) based on pull #131

Closed issue #46 (vector table fault) based on pull #131. Created separate issue #142 to discuss MPRV and SUM.

Created issue #141 – add commentary on base-S mode vs. N-extension

Closed and reopened issue #45 – xtvec.mode - need to add text to state since all priv-modes need to be in either clic or all in non-clic, only m-mode can make selection.

Discussed pull #135 for WFI. text needs to fix typos and more clarification.

Open issue status:

Pulls created to try to close issues:

#29 – Interrupt trigger in the trigger module – try to close with pull #126

#49 – clarification of memory map – try to close with pull #129

#77 – additional detail on CLIC M/S/U memory mapped regions – try to close with pull #129

#79 – supervisor/user mode alignment – try to close with pull #129

#91 – DTS entry – try to close with pull #130

Need spec updates:

#31, #120 – WFI behavior – need to clarify text in pull #135. pull text has typos.

#45 – all priv modes in clic or all in clint. Need spec update that only m-mode can select.

#75 – move hw vectoring to separate section in spec

#107 – heritage of features

#141 – add commentary on bare-s mode

Need more discussion:

#48 – logic/state diagram for clicintip signals

#50 – xcause save privilege modification bits

#96 – proposed reformat of cliccfg

#97 – proposed reformat of xcause CSRs

#98 – name of CLIC

#99, 100, 101, 102, 103, 106 – enhancements

#139 – shadow general purpose registers (GPR) for interrupts?

#140 – automated GPR save/restore?

#142 – effect of MPRV and SUM on hardware vector table access

Issues related to work in other TGs:

#80 – version fields in clicinfo – remove clicinfo and make it a separate platform discovery mechanism?

#81 – programming clic in s and u modes – discussions in hypervisor group about a more general pattern of delegating configurable features

#92 – hypervisor compatibility – goal is not to virtualize CLIC but to allow virtualization of device interrupts. Follow up with hypervisor group.

#109 – add arch string for CLIC – need appropriate named and versioned sub-extensions of clic.

Issues waiting on ratification

#88 – CSR address mapping

Issues punted for rev1, keep open for future enhancements:

#82 – xcause register behavior with some modes in clic and some in clint.

#108 – pushint/popint?