**TILE\_SS\_RVC:  
The Tile building block of a  
Subset RISCV 32-bit Core**

HAS: High-Level Architecture Specifications

Revision HAS 0.1 – draft  
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Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| R*ev. No.* | Who | Description | Rev. Date |
| 0.1 | Amichai Ben-David | Initial TILE\_SS\_RVC HAS | 28 July 2021 |
|  |  |  |  |

**Table 1 - Revision History**

Related Documents

|  |  |  |
| --- | --- | --- |
| Name | Path | Description |
| riscv\_isa\_spec.pdf | TODO | The full RISCV Unprivileged Specification file.  Including the RV32I Baseline ISA |
| SS\_RVC\_HAS.pdf | TODO | The ss\_rvc HAS. Describes the core architecture. |

**Table 2 - Related Documents**

Glossary

|  |  |
| --- | --- |
| Term | Description |
| ISA | Instruction Set Architecture. (such as X86, ARM, RISC-V etc.) |
| IO | Input & output. |
| IP | Intellectual Property. In this case, RTL building block that can be consumed. |
| HAS | High Level Architecture Specifications. (This document) |
| MAS | Micro Architecture Specifications. Document with the microarchitecture details. |
| I\_MEM | Instruction memory – where the program is loaded and ready for execution. |
| D\_MEM | Data Memory – where the LOAD & STORE instructions read/write Data. |
| Pipeline | Common Way to parallel and utilize Hardware  <https://en.wikipedia.org/wiki/Instruction_pipelining> |
| RISC | Reduce Instruction Set Computer. (Unlike CISC -Complex Instruction Set Computer) <https://en.wikipedia.org/wiki/Reduced_instruction_set_computer> |
| Thread | A "hardware thread" is a physical CPU or core that ca run a program. |
| RISC-V | A relatively new open and free ISA. (comparable to intel X86, ARM)  <https://en.wikipedia.org/wiki/RISC-V> |
| RV32I | “RISC-V 32-bit Integer” The RISC-V baseline compatible ISA (no extensions M/A/F etc.) |
| Standard interface | Functional characteristics to allow the exchange of information between two systems |
| Word | 32-bits of data - 4 Bytes. The size of an integer in RV32I ISA. |
| Hazard | Potential source of harm. in this document when reading Outdated data, or wrongly executing Instruction. |
| Strap | Tie signals to constant value (1’b0 or 1’b1) |
| MSFF | Main & Secondary Flip Flop. (AKA Master Slave Flip Flop) |
| Clock Gating | Logic that allows to condition the MSFF clock. Functionality and power reasons. |
| Polling | Actively sampling the status of an external device. |

**Table 3 - Glossary**

# General Description

This HAS describes the High-Level-Architecture of the tile\_ss\_rvc module.  
The tile\_ss\_rvc is the main building block in the SOC.

Each tile contains 3 blocks:

1. **SS\_RVC**

The Core IP - Compatible with a subset of the RISCV RV32I ISA.

1. **MEM\_WRAP**

Contains the I\_MEM & D\_MEM (Instruction Memory & Data Memory)  
Each memory block is dual access – accessible from both CORE & IO\_CTRL.

Holds a the MMIO 1 bit register “PcResetQnnnH”.   
When this register is set the Cores Program Counter will point to Instruction address 0x0.

1. **IO\_CTRL**Controls the Interface with the SOC.  
   In case the input request address matches the local core, the request will be forwarded to the core.   
   In case an input request address misses local core, it lets the Requests to pass through to next tile\_ss\_rvc.

## Tile Block Diagram



Figure – TILE\_SS\_RVC Block Diagram

# 

# Top Level Interface

**Default Parameter Values:**

|  |  |  |
| --- | --- | --- |
| Name | Default Value | Description |
| XLEN | 32 | Integer Size - RV32I Spec |

**Table 4 – SS\_RVC Parameters**

**Interface signals:**

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Size | Direction | Description |
| ClkQH | 1 | Input | Q Clock – a single clock domain. 100Mhz - 2Ghz |
| ResetQnnnH | 1 | Input | Active High |
| TileIdStrapQnnnH | 10 | Input | The Tile ID – used to match Req Address to local Mem Connectivity by strap. |

**Table 5 - SSRV\_CORE general interface**

**Standard interface signals:**

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Size | Direction | Description |
| Input – Standard Interface | | | |
| ReqValidQ500H | 1 | input | Valid |
| ReqOpcodeQ500H | 2 | Input | 2’b00 – RD (Read)  2’b01 - WR (Write)  2’b10 - <reserved>  2’b11 - RD\_RSP(Read Response) |
| ReqAddressQ500H | XLEN | Input | Address[31:22] – indicates the target “Tile-ID”  Address[12] – indicates the Region I\_MEM vs D\_MEM Address[11:0] – Memory offset within 4KB I/D\_MEM |
| ReqDataQ500H | XLEN | Input | In case of WR Opcode – write data to memory In case of Rd Opcode – data should not be used.  In case of Rd\_RSP Opcode – Response Data to SA. |
| Output - Standard Interface | | | |
| RspValidQ504H | 1 | Output | Valid |
| RspOpcodeQ504H | 1 | Output | 2’b00 – RD (Read)  2’b01 - WR ( Write)  2’b10 - <reserved>  2’b11 - RD\_RSP(Read Response) |
| RspAddressQ504H | XLEN | Output | Address[31:22] – indicates the target “Tile-ID”  Address[12] – indicates the Region I\_MEM vs D\_MEM Address[11:0] – Memory offset within 4KB I/D\_MEM |
| RspDataQ504H | XLEN | Output | In case of WR Opcode – write data to memory In case of Rd Opcode – data should not be used.  In case of Rd\_RSP Opcode – Response Data to SA. |

**Table – TILE\_SS\_RVC standard interface**

# Internal interconnect

## IO\_CTRL

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Size | Direction | To/From | Description |
| IO\_CTRL<-> TILE\_SS\_RVC | | | | |
| ClkQH | 1 | Input | TILE\_SS\_RVC |  |
| ResetQnnnH | 1 | Input | TILE\_SS\_RVC |  |
| TileIdStrapQnnnH | 10 | Input | TILE\_SS\_RVC | Match Request address to TILE ID |
| IO\_CTRL<-> MEM\_WRAP | | | | |
| ReqValidQ501H | 1 | Input | MEM\_WRAP | Standard interface |
| ReqOpcodeQ501H | 2 | Input | MEM\_WRAP | Standard interface |
| ReqAddressQ501H | XLEN | Input | MEM\_WRAP | Standard interface |
| ReqDataQ501H | XLEN | Input | MEM\_WRAP | Standard interface |
| RspValidQ503H | 1 | Output | MEM\_WRAP | Standard interface |
| RspOpcodeQ503H | 2 | Output | MEM\_WRAP | Standard interface |
| RspAddressQ503H | XLEN | Output | MEM\_WRAP | Standard interface |
| RspDataQ503H | XLEN | Output | MEM\_WRAP | Standard interface |

## MEM\_WRAP

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Size | Direction | To/From | Description |
| MEM\_WRAP<-> TILE\_SS\_RVC | | | | |
| ClkQH | 1 | Input | TILE\_SS\_RVC |  |
| ResetQnnnH | 1 | Input | TILE\_SS\_RVC |  |
| MEM\_WRAP<->IO\_CTRL | | | | |
| ReqValidQ501H | 1 | Input | IO\_CTRL | Standard interface |
| ReqOpcodeQ501H | 2 | Input | IO\_CTRL | Standard interface |
| ReqAddressQ501H | XLEN | Input | IO\_CTRL | Standard interface |
| ReqDataQ501H | XLEN | Input | IO\_CTRL | Standard interface |
| RspValidQ503H | 1 | Output | IO\_CTRL | Standard interface |
| RspOpcodeQ503H | 2 | Output | IO\_CTRL | Standard interface |
| RspAddressQ503H | XLEN | Output | IO\_CTRL | Standard interface |
| RspDataQ503H | XLEN | Output | IO\_CTRL | Standard interface |
| MEM\_WRAP<->SS\_RVC | | | | |
| PcQ100H | XLEN | Input | SS\_RVC |  |
| InstructionQ101H | 32 | Output | SS\_RVC |  |
| AddressDmQ103H | XLEN | Input | SS\_RVC |  |
| WrDataDmQ103 | XLEN | Input | SS\_RVC |  |
| RdEnDmQ103H | 1 | Input | SS\_RVC |  |
| WrEnDmQ103H | 1 | Input | SS\_RVC |  |
| RdDataDmQ104H | XLEN | Output | SS\_RVC |  |
| PcResetQnnnH | 1 | output | SS\_RVC |  |

## SS\_RVC

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Size | Direction | To/From | Description |
| SS\_RVC <-> TILE\_SS\_RVC | | | | |
| ClkQH | 1 | Input | TILE\_SS\_RVC |  |
| ResetQnnnH | 1 | Input | TILE\_SS\_RVC |  |
| SS\_RVC<->MEM\_WRAP | | | | |
| PcQ100H | XLEN | Input | MEM\_WRAP | Ad-hoc |
| InstructionQ101H | 32 | Output | MEM\_WRAP | Ad-hoc |
| AddressDmQ103H | XLEN | Input | MEM\_WRAP | Ad-hoc |
| WrDataDmQ103 | XLEN | Input | MEM\_WRAP | Ad-hoc |
| RdEnDmQ103H | 1 | Input | MEM\_WRAP | Ad-hoc |
| WrEnDmQ103H | 1 | Input | MEM\_WRAP | Ad-hoc |
| RdDataDmQ104H | XLEN | Output | MEM\_WRAP | Ad-hoc |
| PcResetQnnnH | 1 | Input | MEM\_WRAP | Ad-hoc |

## Interface Block Diagram



Figure 2 - Interface Block Diagra

# **TILE\_SS\_RVC\_<#> in the SOC**

Many Tiles together can be connected to a “ring architecture”.  
Together they make a multi-core SOC.

* All the Tiles are “passive” and cannot generate ring traffic.
* The System Agent interacts with the Tiles memory by sending RD/WR requests on the ring.
* The latency is deterministic for all transaction.
  + The Tile latency of Request to Response. (Both for TILE\_ID hit & miss):
  + The System agent Latency Request to Response:

## SOC Block Diagram



Figure - SOC Block diagram

## SOC Execution Flow:

1. Reset stage – Reset the Control bits & Set the MMIO PcResetQnnnH register.

When exiting the RESET – all PC are stock at reset value pointing to 0x0 I\_MEM.

1. SA (System Agent) will load the program to I\_MEM & the Data set to D\_MEM.  
   This is done by sending the program & Data to the Tiles with the correct Address offset.
2. Start the program by writing to the “PcResetQnnnH” 1’b0.  
   This will allow the PC to exit the reset and start executing the program.