Type R-I

Format	Instruction	Operation	Cycles	Description
rd rd rd rd I I I I I I I I 0 0 0 1	LDI rd, I	rd <= I	1	Load Immediate
rd rd rd rd I I I I I I I I 0 0 1 1	ANI rd, I	rd <= rd & I	1	AND Immediate
rd rd rd rd I I I I I I I I 0 1 0 1	ORI rd, I	rd <= rd | I	1	OR Immediate
rd rd rd rd I I I I I I I I 0 1 1 1	XOI rd, I	rd <= rd ^ I	1	XOR Immediate
rd rd rd rd I I I I I I I I 1 0 0 1	ADI rd, I	rd <= rd + I	1	ADD Immediate
rd rd rd rd I I I I I I I I 1 0 1 1	ACI rd, I	rd <= rd + I + C	1	ADD Immediate With Carry
rd rd rd rd I I I I I I I I 1 1 0 1	CPI rd, I	See Note 1	1	Compare Immediate

Type R-L

Format	Instruction	Operation	Cycles	Description
rd rd rd rd L L L L L L L L 0 0 1 0	IN rd, L	rd <= *L	2	IO In
rs rs rs rs L L L L L L L L 0 1 0 0	OUT rs, L	*L <= rs	1	IO Out

Type R-R

Format	Instruction	Operation	Cycles	Description
rd rd rd rd rs rs rs rs 0 0 0 0 1 0 0 0	AND rd, rs	rd <= rd & rs	1	AND
rd rd rd rd rs rs rs rs 0 0 0 1 0 0 0 0	OR rd, rs	rd <= rd | rs	1	OR
rd rd rd rd rs rs rs rs 0 0 0 1 1 0 0 0	XOR rd, rs	rd <= rd ^ rs	1	XOR
rd rd rd rd rs rs rs rs 0 0 1 0 0 0 0 0	ADD rd, rs	rd <= rd + rs	1	ADD
rd rd rd rd rs rs rs rs 0 0 1 0 1 0 0 0	ADC rd, rs	rd <= rd + rs + C	1	ADD With Carry
rd rd rd rd rs rs rs rs 0 0 1 1 0 0 0 0	CMP rd, rs	See Note 1	1	Compare
rd rd rd rd rs rs rs rs 0 0 1 1 1 0 0 0	SUB rd, rs	rd <= rd - rs	1	Subtract
rd rd rd rd rs rs rs rs 0 1 0 0 0 0 0 0	SBB rd, rs	rd <= rd - rs - C	1	Subtract With Borrow
rd rd rd rd rs rs rs rs 0 1 0 0 1 0 0 0	MOV rd, rs	rd <= rs	1	Move

Type R

Format	Instruction	Operation	Cycles	Description
rd rd rd rd 0 0 0 0 0 1 0 1 0 0 0 0	NOT rd	rd <= !rd	1	NOT
rd rd rd rd 0 0 0 0 0 1 0 1 1 0 0 0	SLL rd	rd <= rd << 1	1	Shift Left Logical
rd rd rd rd 0 0 0 0 0 1 1 0 0 0 0 0	SRL rd	rd <= rd >> 1	1	Shift Right Logical
rd rd rd rd 0 0 0 0 0 1 1 0 1 0 0 0	SRA rd	rd <= rd >>> 1	1	Shift Right Arithmetic

Type R-RP

Format	Instruction	Operation	Cycles	Description
rs rs rs rs rp rp rp rp 0 1 1 1 0 0 0 0	STR rs, rp	*rp <= rs	1	Store
rs rs rs rs rp rp rp rp 0 1 1 1 1 0 0 0	SRI rs, rp	*rp <= rs, rp <= rp + 1	1	Store, Post Increment
rs rs rs rs rp rp rp rp 1 0 0 0 0 0 0 0	SRD rs, rp	*rp <= rs, rp <= rp - 1	1	Store, Post Decrement
rd rd rd rd rp rp rp rp 1 0 0 0 1 0 0 0	LDR rd, rp	rs <= *rp	2	Load
rd rd rd rd rp rp rp rp 1 0 0 1 0 0 0 0	LRI rd, rp	rs <= *rp, rp <= rp + 1	2	Load, Post Increment
rd rd rd rd rp rp rp rp 1 0 0 1 1 0 0 0	LRD rd, rp	rs <= *rp, rp <= rp - 1	2	Load, Post Decrement

Type RP

Format	Instruction	Operation	Cycles	Description
0 0 0 0 rp rp rp rp 1 0 1 0 0 0 0 0	IRP, rp	rp <= rp + 1	1	Increment Register Pair
0 0 0 0 rp rp rp rp 1 0 1 0 1 0 0 0	DRP, rp	rp <= rp - 1	1	Decrement Register Pair
0 0 0 0 rp rp rp rp 1 0 1 1 0 0 0 0	JMPI, rp	PC <= rp	2	Jump Indirect
0 0 1 0 rp rp rp rp 1 0 1 1 0 0 0 0	JCI, rp	PC <= rp, If C	1 or 2	Jump Carry Indirect
0 1 0 0 rp rp rp rp 1 0 1 1 0 0 0 0	JNCI, rp	PC <= rp, If !C	1 or 2	Jump Not Carry Indirect
0 0 1 0 rp rp rp rp 1 0 1 1 0 0 0 0	JZI, rp	PC <= rp, If Z	1 or 2	Jump Zero Indirect
1 0 0 0 rp rp rp rp 1 0 1 1 0 0 0 0	JNZI, rp	PC <= rp, If !Z	1 or 2	Jump Not Zero Indirect
1 0 1 0 rp rp rp rp 1 0 1 1 0 0 0 0	JNI, rp	PC <= rp, If N	1 or 2	Jump Negative Indirect
1 1 0 0 rp rp rp rp 1 0 1 1 0 0 0 0	JNNI, rp	PC <= rp, If !N	1 or 2	Jump Not Negative Indirect